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A high speed graphics DRAM with low power and low noise data bus inversion in 54 nm CMOS

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Abstract: This paper presents a high speed 1 Gb GDDR3 Graphics DRAM using data bus inversion (DBI) DC mode in order to achieve low power and low noise in DRAM. A DBI, digital majority voter (DMV) circuit and the Global I/O (GIO) control circuit on the DBI DC mode are newly proposed. In this DMV, The current of GIO toggle pattern is consumed less than 47% compared with the analog majority voter (AMV). The voltage fluctuation wave form of the data eye is also reduced in accordance with DBI on the operation mode. Using the proposed DBI scheme can produce almost stable signal integrity of the DQs against high speed operation. The DBI is fabricated using 54 nm technology.

Keywords: DMV, AMV, DBI, DBI DC

Classification: Integrated circuits

References

[1] M. R. Stan and W. P. Burleson, "Bus-invert coding for low-power I/O," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 3, no. 3, pp. 49–58, March 1995.

[2] S. J. Bae, K. I. Park, J. D. Ihm, H. Y. Song, W. J. Lee, H. J. Kim, K. H. Kim, Y. S. Park, M. S. Park, H. K. Lee, S. Y. Bang, G. S. Moon, S. W. Hwang, Y. C. Cho, S. J. Hwang, D. H. Kim, J. H. Lim, J. S. Kim, S. H. Kim, S. J. Jang, J. S. Choi, Y. H. Jun, K. Kim, and S. I. Cho, "An 80 nm 4 Gb/s/pin 32 bit 512 Mb GDDR4 Graphics DRAM With Low Power and Low Noise Data Bus Inversion," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 121–131, Jan. 2007.

[3] Y. S. Shon, J. H. Choi, I. Y. Chung, H. J. Chung, C. K. Kim, G. S. Byun, D. W. Kang, W. K. Park, I. S. Park, H. S. Hwang, C. H. Kim, and S. I. Cho, "A512 Mbit, 3.2 Gbps/pin Packet-based DRAM with cost-efficient clock generation and distribution scheme," *in Symp. VLSI Circuits Dig. Tech. Papers*, pp. 36–37, 2004.

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[4] K. Nakamura, K. Takeda, H. Toyoshima, K. Noda, H. Ohkubo, T. Uchida, T. Shimizu, T. Itani, K. Tokashiki, and K. Kishimoto, "A 500-MHz 4-Mb CMOS pipeline-burst cache SRAM with point-to-point noise reduction coding I/O," *IEEE J. Solid-State Circuit*, vol. 32, no. 11, pp. 1758–1765, Nov. 1997.

1 Introduction

In recent years, a trend on DRAM has been focusing on increasing speed and the efficiency of power consumption. In order to achieve both high speed and low-power, the graphics SDRAM extends the number of I/O lines up to 32 lines per DRAM and increases the data rate to several Gb/s/pin, while maintaining the single-ended signaling. However, the DRAM suffers from bottlenecks caused by the parallel single-ended signaling such as crosstalk, and power consumption of I/O. The more transitions between low and high data at I/O, the greater the power and noise of high speed memory interface are generated [1].

To overcome these bottlenecks of signal integrity (SI), we propose a data bus inversion (DBI) DC mode to improve data characteristic for high speed and low power same as Graphics DRAM. The DBI DC is used to reduce the power consumption of the data channels, resulting in a restriction in the total number of simultaneously driven-low DQ lines. However, this number should not exceed a half of the total number of DQ lines. In the case of the Graphics SDRAM, one DBI DC is allocated to one byte of DQs. Fig. 1 (a) shows the encoding algorithm of DBI DC. DBI DC checks the number of '0' among present byte data. If the number of '0' is more than or equal to 4, byte data are inverted and DBI flag is also set to high, which indicate that data are inverted. The outputs of DBI DC encoder have 5 case of the number of '0'. The minimum number of zeros is 0 and the maximum number of zeros is 4 [2].

2 The Proposed Write DBI (WDBI) Scheme

The write operation occurs when the data coming from outside of the DRAM are stored in the cells. Otherwise, when the data stored in the cells are to be transferred through DQ pins, the read operation occurs. In the case of the write operation, the WGIO (Write Global I/O) toggles inside of the DRAM right before the data come through DQ pins. No matter which DQ pins are selected as a data path, the WGIO signal toggles every time when the data comes in. As the X32 graphics DRAM reads or writes one byte data at a time, the 128 drivers operate at the same time. This leads to the power drop problem and the increase of the current, because the number of toggles increases when the GPU sends a large amount of data to the DRAM through DQ pins. Also, the performance can be lowered when the DRAM operates at high speed. To solve these problems, the WDBI is proposed in this paper.

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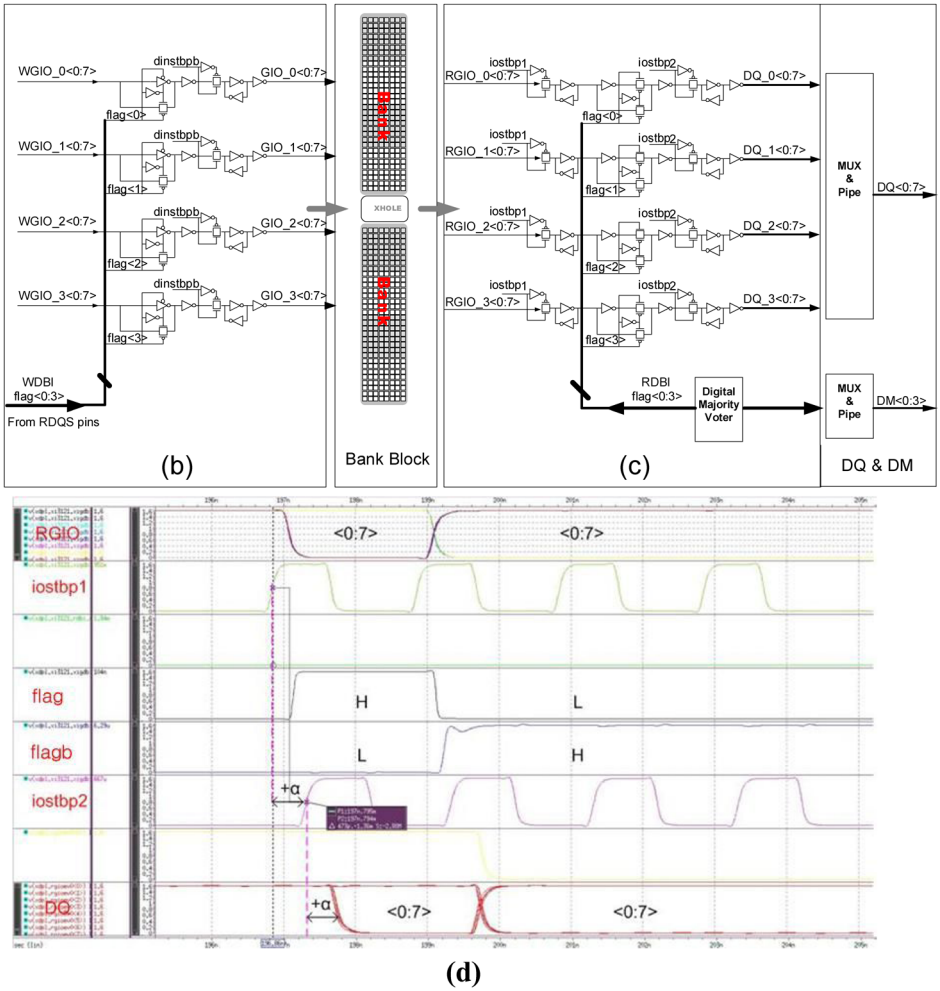
DBI DC

case	DQ<0:7>		case	DQ<0:7>	Num.of 0	Flag
1	00000000		1	11111111	0	1
2	00000001		2	11111110	1	1
3	00000011	Inversion	3	11111100	2	1
4	00000111		4	11111000	3	1
5	00001111		5	11110000	4	1
6	00011111		6	00011111	3	0
7	00111111	Non Inversion	7	00111111	2	0
8	01111111		8	01111111	1	0
9	11111111		9	11111111	0	0

(a)



(d)

Fig. 1. (a) Algorithm of data bus inversion of DBI DC mode (b) The WDBI GIO control scheme (c) The RDBI GIO control scheme (d) The operating wave of RDBI scheme

The WDBI helps to lower the number of toggles at the WGIO when the chip operates in the write mode.

The WDBI GIO control scheme shown in Fig. 1 (b) is controlled by the value of the EMRS (Extended Mode Register Set). When the WDBI mode is selected, the DRAM gets the WDBI flag signal from the GPU through the

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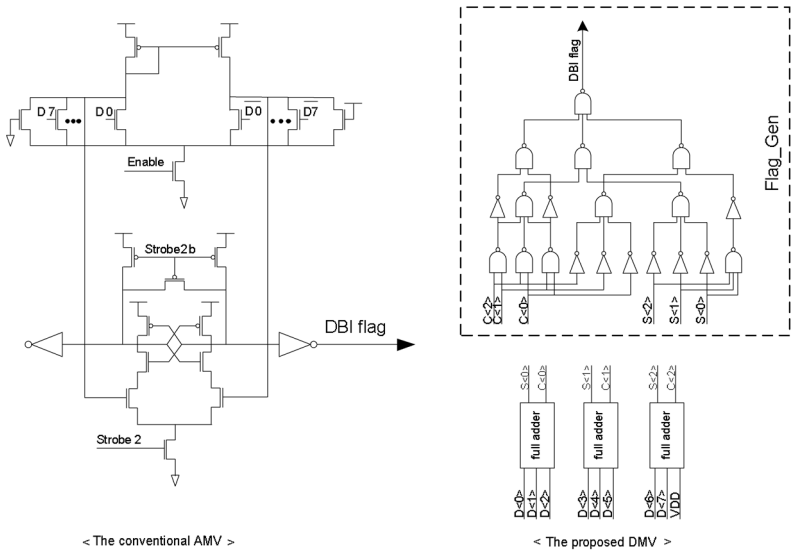
RDQS pin in the case of the write operation shown in Fig. 1 (b). The WDBI flag signal contains the information about whether the data of the GIO have more than four zeros or not.

The WDBI flag signal consists of four bits and is used at the WDBI GIO control block. The WGIO<0:7> data are latched by the 'dinstbpb' (internal Write) signal and stored in the cell after being controlled by the flag<0:3>. The proposed WDBI scheme controls the flag signal very easily and consists of simple logic so that the SI characteristic is enhanced at high speed.

3 The Proposed Read DBI Scheme

The proposed DBI control logic located at the X/Y cross area is used. This



Num of '1'	S	C
0	0	0
1	1	0
2	0	1
3	1	1

SUM(S) = A⊕B⊕C
Carry(C) = A·B + A·C + B·C

< Truth table >

(a)

Comparison	Analog		Digital	
Measure	avg	peak	avg	peak
Current (with GIO toggle)	10.4mA	45.2mA	5.56mA	20.2mA
Current (without GIO toggle)	8.79mA	38.2mA	2.85mA	13.7mA
Layout area	90x19.6μm^2		82.32x19.6μm^2	
Speed	729ps		471ps	

(b)

Fig. 2. (a) The comparison of the scheme of conventional majority voter and proposed majority voter (b) The comparison of conventional and proposed majority voter

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control logic determines whether present byte data is converted or not. The number of RGIO data '0' is directly reduced by the flag information of the DBI.

The DBI flag signal consists of four bits and is generated from the digital majority voter (DMV). As shown in Fig. 1 (c), it determines whether the present RGIO data is converted or not based on the number of '0'. The DBI flag signal is also obtained at the same time when the RGIO data, which are manipulated by eight bits, are latched according to the control signals. As shown in Fig. 1 (d), the 'iostbp1' signal is generated by a 'Read' command. The 'iostbp2' signal is a delayed signal from the 'iostbp1' signal. The RGIO<0:7> data, which consist of one byte, are latched at the rising edge of the 'iostbp1' signal.

The 'flag' signal is synchronized with the 'iostbp1' signal and determines whether the RGIO data should be inverted or not. The RGIO data are re-latched at the 'iostbp2' signal to obtain the margin.

Consequently, the amount of '0' toggling of the DQ data decreases. This improvement results in the decrease of the current and the power drop at the DQ pins.

4 The Proposed Digital Majority Voter

The conventional analog majority voter (AMV) has the overhead of die area and current, therefore, the DMV is newly proposed in this Graphics DRAM (1 Gb GDDR3). The proposed DMV solves the conventional analog type problem mentioned above. As shown in Fig. 2 (a), the proposed DMV consists of much simpler elements than the conventional one. The eight bits RGIO data (D<0:7>) are connected to the full adder input and the result is composed of Sum(S) and Carry(C) which consists of three bits for each. As shown in the truth table, these S and C are determined by the counter of '1'. The 'Fag_Gen' block determines the DBI flag to 'H' or 'L' in accordance with mixing of S<0:2> and C<0:2>. If the RGIO data have more than or equal to 4 '0's, the DMV generates such a signal that the DBI flag can be enabled. Otherwise, if the number of '0' is less than 4, the DBI flag signal is disabled to determine whether the values of the RGIO data are converted or not.

In the case of the analog type, the RGIO data outputs are sensitive to offset when data have equal number of '0' and '1'. The size of the AMV can be also large, which is dependent on the elements used. The DMV operates independently from the offset and current consumption is also decreased from 10.4 mA to 5.56 mA at the RGIO toggle pattern compared with the current of the analog type in Fig. 2 (b). In addition, Fig. 2 (b) shows the comparison of the operating speed and the layout area between the proposed DMV and the conventional analog one using actual data.

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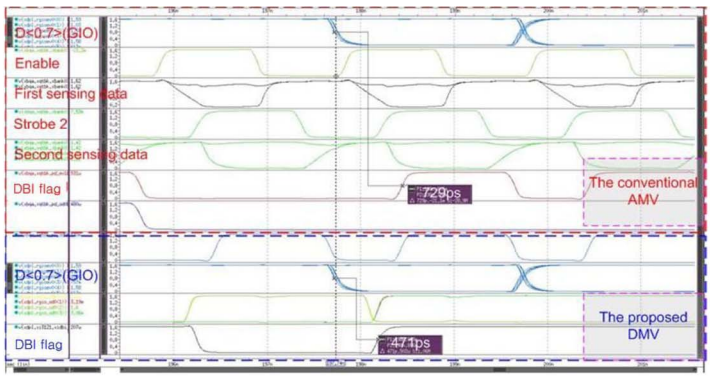
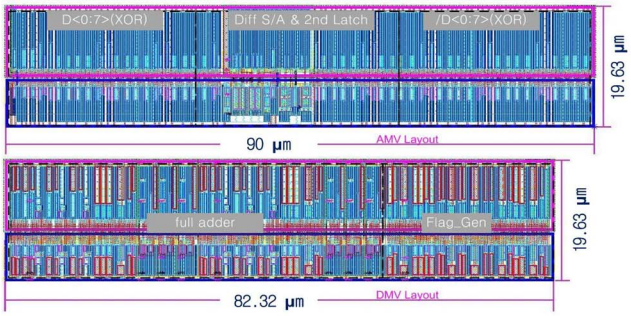
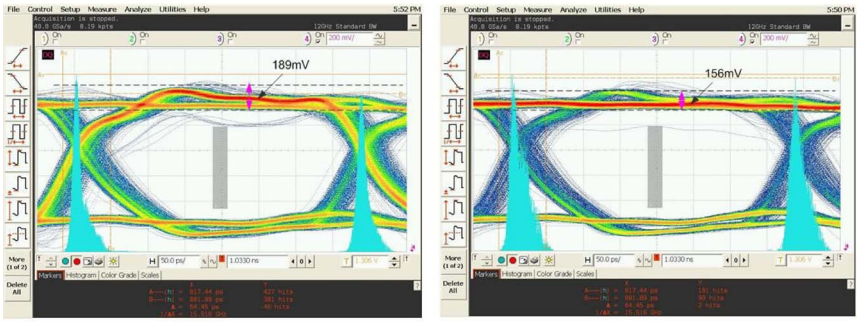


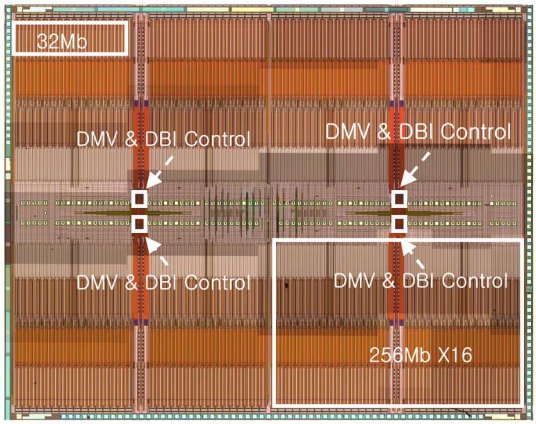
(a)



(b)



(c)



(d)

Fig. 3. (a) The operating speed wave form of conventional and proposed majority scheme (b) The comparison of layout area (c) Measurement results of the eye pattern at the data rate with DBI on/off mode (d) The microphotograph of the chip

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5 Experiment

This circuit is simulated using HSPICE with a CMOS process parameter of 54 nm. Fig. 3 (a) shows the post-layout simulation result of the DMV and AMV. The operating speed of the proposed DMV is improved from 729 ps to 471 ps, the layout area was compared with that of the conventional AMV as shown in Fig. 3 (b). Also, the average current consumption at read operation is reduced from 301 mA to 247 mA in 32 I/O at supply voltage of 2.0 V, and the peak current is reduced from 610 mA to 271 mA at DBI DC. This performance enhancement is achieved when these data are measured at supply voltage of 2.0 V, Vref=70%. Also, Fig. 3 (c) shows the measured eye pattern of read data. In order to measure the performance enhancement due to DBI DC mode, both turn-on and turn-off modes of DBI DC are measured using same data pattern. The microphotograph of 1 Gb Graphics SDRAM is shown in Fig. 3 (d) where four DMV and DBI controllers are indicated.

6 Conclusions

A 1 Gb GDDR3 SDRAM is implemented by using the DBI, the WDBI and the RDBI scheme. The proposed DBI DC is used to solve the problem of a parallel SI by reducing I/O power consumption and power supply noise. The conspicuous improvement is that the peak current is reduced about 339 mA at the DBI DC if it is compared with the average current. Measurement results on the read data with and without DBI DC operation show that the DBI operation reduced the voltage fluctuation from 189 mV to 156 mV at 1.2 GHz of AMD RV770 graphic application board. The 1 Gb GDDR3 SDRAM is fabricated by using 54 nm technology.

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