A broadband 5-bit CMOS step attenuator in small area with low insertion loss

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Abstract: A broadband 5-bit CMOS step attenuator in small area with low insertion loss is presented in this paper, which is implemented with three independent attenuation modules and two compact T-type attenuation networks. Two of the independent modules are switched π-type, and the other is bridged-T type. The compact T-type attenuation networks share the series branches with the adjacent modules to decrease the chip area and insertion loss. The proposed attenuator has a maximum attenuation range of $0-31\,\mathrm{dB}$ with $1\,\mathrm{dB}$-increase at the operational frequency range of $5-20\,\mathrm{GHz}$ and consumes a layout area cost of $0.44\,\mathrm{mm}^2$. The insertion loss is less than $8.7\,\mathrm{dB}$. The RMS insertion amplitude and phase error are less than $0.45\,\mathrm{dB}$ and $5.7°$, respectively.

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1 Introduction

CMOS digital step attenuators are widely used as modern gain controlled applications in communication systems, for their facility to design and extremely low power consumption [1]. Although variable gain amplifiers (VGAs) have been the traditional means to implement dB-linear gain controlling, their applications are limited for their poor linearity and narrow bandwidth [2, 3]. Thus, CMOS digital step attenuators make it possible to be a candidate for implementing dB-linear gain variation.

Conventional CMOS digital step attenuators are based on resistance networks with MOS switches. Those step attenuators can be switched among different attenuative states with independent attenuation modules [4, 5]. While, the long chain of cascaded attenuation modules may cost a large chip area, which can be as large as $0.5\,\text{mm}^2$ [4, 6]. Besides, the parasatric resisitance in the long module-chain introduces great insertion loss [1, 4]. In order to integrate the digital step attenuators into communication systems in a single chip, the area cost needs decreasing. Besides, the insertion loss should also be as low as possible.

This paper proposed a broadband 5-bit CMOS step attenuator in small area with low insertion loss. The attenuator is designed on switched bridged-T topology and π topology to implement larger attenuative amplitude. By sharing the series branches with the two adjacent attenuation modules, the compact T-type attenuation network is realized by a single shunt branch to achieve smaller amplitude of attenuation. With the compact structure, the attenuator can minimize both the chip area cost and insertion loss.

2 Design of proposed step attenuator

The topology of the proposed broadband 5-bit CMOS step attenuator is shown in Fig. 1. As shown, the attenuation amplitude of the five attenuation modules are chosen to be $1\,\text{dB}$, $2\,\text{dB}$, $4\,\text{dB}$, $8\,\text{dB}$ and $16\,\text{dB}$, respectively, to achieve an attenuation range of 0–$31\,\text{dB}$ by $1\,\text{dB}$-step with a 5-bit digital control signal.
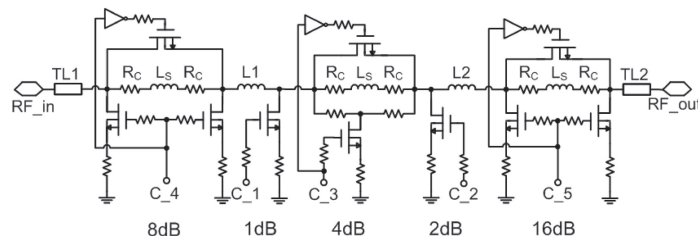

Fig. 1. Topology of proposed attenuator.

Due to the two shunt branches, the switched π-topology attenuator is used to implement the $8\,\text{dB}$- and $16\,\text{dB}$-attenuation modules. As the resistor on the series branch of a π-topology attenuator with $4\,\text{dB}$-attenuation is very small, as much as $24\,\text{Ohms}$, it will be quite sensitive to the parasitic resistance of the interconnection lines. Therefore, the $4\,\text{dB}$-attenuation module is based on bridged-T topology.

In general, the 1 dB- and 2 dB-attenuation modules in a step attenuator are based on bridged-T topology. While, the impedance of the MOS switches at on-state and off-state are different. At off-state, the impedance of the MOS switches performs more capacitive than that at on-state. The parasitic capacitance will provide a leakage path for signal in series branch, which will decrease the attenuation amplitude, especially in higher frequency. This may narrow the operational bandwidth of the attenuator. Additionally, the capacitance will also cause the phase leading of output signals at attenuation state to that at reference state. The phase difference, defined as insertion phase, may cause phase errors for blocks following with the attenuator. By inserting an inductor into the series branches of each attenuation module can compensate the insertion phase of the attenuator [4] and degrade the phase error induced as operating. In addition, the inductance can block part of the signal leakage and improve the operational bandwidth of each attenuation state.

The inserted inductors of each attenuation module will cost large chip area and involve much signal power loss. Therefore, the 1 dB- and 2 dB-attenuation modules are designed with compact structure to discard the chip area of the inserted inductors. Moreover, sharing the series branches with other modules can also decrease the insertion loss caused by the parasitic resistance on signal path and inserted inductors.

As Fig. 1 shows, the 4 dB-attenuation module is placed in the middle of the two π-topology modules, to have a good symmetric performance for the compact 1 dB- and 2 dB-attenuation modules. The 1 dB-attenuation module is between the 8 dB- and 4 dB-attenuation modules and shares the series branches with both of the two modules. The 2 dB-attenuation module is of same situation between the 4 dB- and 16 dB-attenuation modules. The mirror symmetric relationship of 1 dB and 2 dB attenuation modules has a complementary when the two modules are operating.
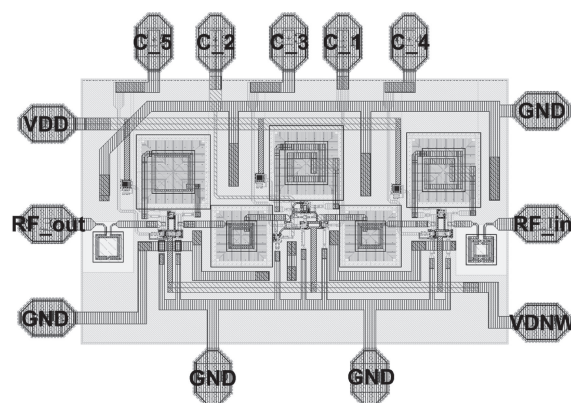

Fig. 2.   Layout of proposed attenuator.

The proposed attenuator is implemented in SBC18H2 0.18 μm BiCMOS process from Jazz Semiconductor, and its layout is shown in Fig. 2. Compared with the attenuators presented in [1] and [4], the proposed attenuator is 12%

smaller with a chip area of $840 \times 520\,\mu m^2$ ($0.44\,mm^2$) including PADs. Besides, the sharing of series resistance makes the insertion loss 20% lower.

As Fig. 1 and 2 show, the proposed attenuator is controlled by a 5-bit digital signal, C_1, C_2, C_3, C_4, C_5, which are used to control $1\,dB$, $2\,dB$, $4\,dB$, $8\,dB$ and $16\,dB$ attenuation modules, respectively. Each attenuation module is controlled by MOS switches, whose body terminals are connected to their source terminal with deep N-well technology. An inductor is inserted between two adjacent independent modules, i.e. L1 and L2, to satisfy the matching, and transmission lines are involved to match the input and output to $50\,\Omega$.

3 Experimental results and discussion

The layout simulation is performed using Cadence Virtuoso Tool and Agilent Advanced Design System 2009U1 version. The EM simulation is involved with Sonnet Software to determine the performance of parasitic effects on the signal line. The simulation results are shown in Fig. 3.
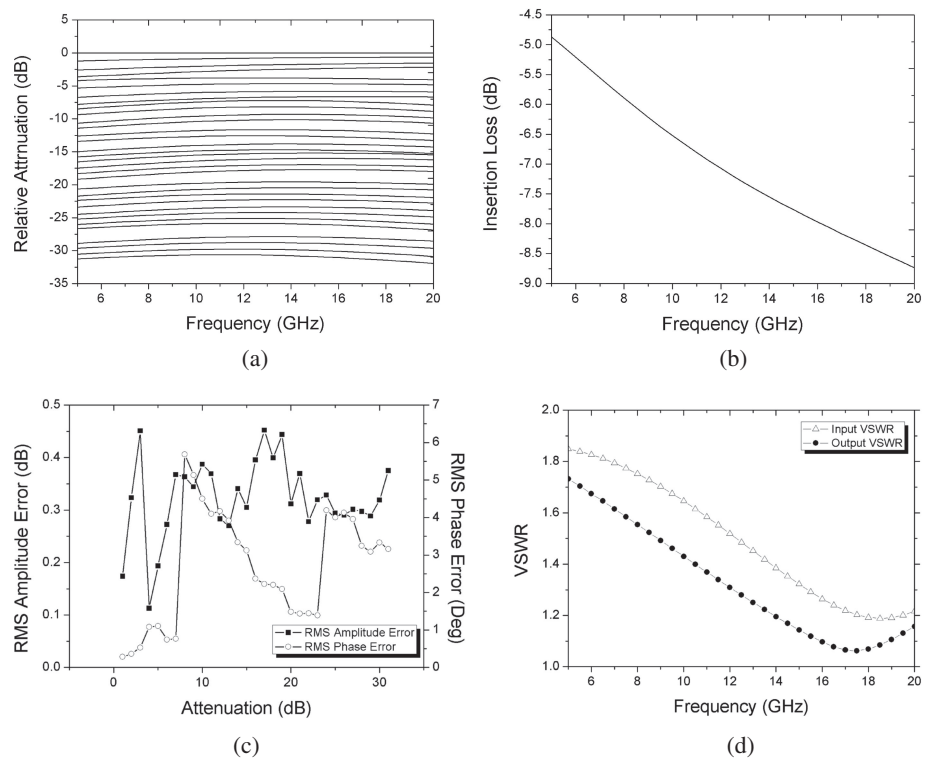
Fig. 3. Simulation results: (a) relative attenuation, (b) insertion loss, (c) RMS amplitude error and phase error, (d) input and output VSWR.

Fig. 3(a) shows the results of relative attenuation amplitude. The proposed attenuator has a maximum attenuation range of 0–$31\,dB$ with $1\,dB$-increase at frequency range of 5–$20\,GHz$. As shown, each of the attenuation state has no overlap. The insertion loss (IL), shown in Fig. 3(b), increases following with the frequency, due to the parasitic capacitance between metal

interconnection and silicon substrate. The maximum IL is 8.7 dB at 20 GHz, and 3.9 dB variation at 5–20 GHz.

Fig. 3(c) is the root mean square (RMS) amplitude error and phase error of each attenuation state. As shown, the amplitude error of the proposed attenuator is less than 0.45 dB, and the phase error is less than 5.7°. With small amplitude and small phase error, the proposed attenuator can operate accurately for amplitude controlling.

The voltage standing wave ratio (VSWR) is shown in Fig. 3(d). The VSWR simulation is performed with 50 Ω input and output impedance. As shown, the input VSWR is less than 1.85, and the output VSWR is less than 1.73. The results show that both the input and output of proposed attenuator are well matched to a characteristic impedance of 50 Ω.

In addition, the input 1-dB compression point P_{1dB} of the proposed attenuator is 15.63 dBm. Thus, the attenuator can well work with large signal power.

Table I gives the performance comparison of the proposed step attenuator with other presented ones. As shown, the proposed attenuator has a minimum chip area and insertion loss at a broad oprational frequency range.

Table I. Comparison of digital step attenuators

Ref.	This work	[1]	[4]	[6]
Tech (µm)	0.18	0.13	0.18	0.18
BW (GHz)	5–20	DC–20	DC–14	10–67
Attenuation rang (dB)	31	31	31.5	32–42
Min Attenuation (dB)	1	1	0.5	—
Insertion loss (dB)	<8.7	<11	<10	<11
Amplitude error (dB)	<0.45	<0.5	<0.5	<6.8
Chip area (mm^2)	0.44	0.5	0.5	0.77

4　Conclusion

A broadband 5-bit CMOS step attenuator in small area with low insertion loss is proposed and simulated with layout in this paper. The attenuator has a maximum attenuation range of 0–31 dB with 1 dB-increase at frequency range of 5–20 GHz. With the compact topology, the layout consumes an area of 0.44 mm^2 and the insertion loss is less than 8.7 dB, which performs better than attenuators presented in other works. As implemented in BiCMOS technology, the proposed attenuator can be used for integrated broadband communication systems with less chip area cost and smaller insertion loss.

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