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Sinusoidal-switched serial-coupled CMOS LC quadrature VCO

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Abstract: A new topology to design low-phase-noise low-power quadrature voltage-controlled-oscillator (QVCO) is proposed. The proposed topology is based on using a dynamic transistor biasing scheme in a typical voltage-controlled-oscillator (VCO). This method modifies the equivalent impulse-sensitivity-function (ISF) of oscillator to reduce the oscillator sensitivity to noise sources and as a result reducing the oscillator phase noise. A 1.8 GHz, 1.8v designed QVCO with 0.18u CMOS technology based on the proposed topology shows a phase noise of −134 dBc/Hz at 1 MHz offset frequency from the carrier.

Keywords: quadrature voltage-controlled-oscillator (QVCO), coupled-oscillators, phase noise, impulse-sensitivity-function (ISF)

Classification: Integrated circuits

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1 Introduction

Since introduction of the coupled VCO's method to design quadrature-VCO (QVCO), which was proposed by Rofougaran [1], coupled oscillators has be-

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come one of the most commonly used method for quadrature LO (Local Oscillator) signal generation [1, 2, 3]. The main issue in designing QVCO is to obtain lower phase noise with precise quadrature outputs. In [2], cascode-coupling method for lower phase noise with good quadrature accuracy is proposed. In [3], second order harmonics coupling topology is introduced to decrease phase noise of QVCO but phase accuracy is not guaranteed in this structure. This paper proposes a new QVCO topology with introducing a new low-phase-noise sinusoidal-switched VCO which is coupled with a similar VCO to make a low-phase-noise QVCO.

Section 2 introduces oscillator phase noise reduction through impulse-sensitivity-function (ISF) shaping and in the section 3, sinusoidal switched oscillator is presented. In section 4, the proposed QVCO is introduced. Sections 5 and 6 present the simulation results and conclusion.

2 Oscillator Phase Noise Reduction

In designing a QVCO, the oscillator phase noise and quadrature phase accuracy are two main design constraints [1, 2, 3]. First, it is needed to design a low-phase-noise VCO and then design a good coupling method to couple VCOs. Therefore, a new method to design a low-phase-noise VCO is initially introduced. From the general phase noise theory [4], the phase noise formula based on the root-mean-square ($\boldsymbol{rms}$) value of the impulse-sensitivity-function (ISF) of oscillator is:

$$L(\Delta\omega) = 10.\log_{10}\left[\frac{\frac{\overline{i_n^2}}{\Delta f}(ISF_{rms}^2)}{2q_{\max}^2.(\Delta\omega)^2}\right] \tag{1}$$

where $\overline{i_n^2}/\Delta f$ is the power spectrum density of the parallel current noise, $\mathrm{ISF}_{\mathrm{rms}}$ is the root-mean-square (rms) value of the impulse-sensitivity-function (ISF) associated with that noise source, $\boldsymbol{q_{max}}$ is the maximum charge displacement on the tank circuit and $\Delta\omega$ is the offset frequency from the carrier.

From (1), it is clear that the oscillator phase noise can be reduced by: a) reducing noise power spectrum density, b) reducing $\boldsymbol{rms}$ value of ISF, c) increasing the tank quality factor (Q) and d) increasing the oscillation amplitude. Items (c) and (d) increases $\boldsymbol{q_{max}}$ thereby reducing the oscillator phase noise. But the tank quality factor Q is limited to the on-chip low-Q inductors. For on-chip inductors, increasing Q has physical limitations. Increasing the oscillation amplitude is limited by the supply voltage which is not achievable in low voltage designs used in new short channel CMOS processes. Decreasing the noise power is also limited by the fabrication technology. On the other hand, lowering the $\boldsymbol{rms}$ value of the ISF is a straight forward solution for phase noise reduction.

As shown in [4], ISF is approximately equal to $\boldsymbol{f'(x)/[\max(f'(x))]^2}$, where $\boldsymbol{f(x)}$ is the oscillator output waveform. Of course there is one ISF for each noise source but in a symmetric structure of transistors, it can be assumed that ISF for all transistors' noise sources is approximately the same.

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For LC oscillators, ISF is approximately equal to $\cos(\omega_0 t)/V_{m.}$, where V_m is the oscillation amplitude and the oscillator output voltage is $V_{out}(t) = V_{m.}\sin(\omega_0 t)$. If transistor's current varies with time, then its generated noise will be a cyclostationary process controlled by the shape of its current. In this case as mentioned in [4], it is described an equivalent-ISF which is the product of the ISF and $a(t)$; which is the shape of the transistor's current waveform. The $a(t)$ is a scaled function with unity peak value proportional to the transistor's current and it is a periodic function. By changing the shape of $a(t)$, the shape of the equivalent-ISF can be can modified. Modification of the equivalent-ISF should be done in a manner that its rms value decreases to reduce the phase noise. Indeed, minimizing the rms value of the equivalent-ISF is an optimization problem and the problem is to find the unity function of $a(t)$ which minimize the rms value of the equivalent-ISF as:

$$\min(ISF_{rms}^2) = \min\left(\frac{1}{\pi}\int_0^{\pi}\left(a(t).\frac{\cos(\omega_0 t)}{v_m}\right)^2 d(\omega_0 t)\right) \tag{2}$$

where the oscillator output voltage is $V_{out}(t) = V_m \sin(\omega_0 t)$. As $a(t)$ is less than or equal to one, we can write:

$$\int_0^{\pi}\left(a(t).\frac{\cos(\omega_0 t)}{v_m}\right)^2 .d(\omega_0 t) \leq \int_0^{\pi}\left(\frac{\cos(\omega_0 t)}{v_m}\right)^2 d(\omega_0 t) \tag{3}$$

From (3), in constant oscillation amplitude (V_m), equivalent-ISF shaping can decrease its rms value in order to decrease the oscillator phase noise. Actually, it is not easy to find a closed form formula for $a(t)$ but we can consider that $a(t)$ should be zero in the maximum points of the ISF to decrease rms value of the equivalent-ISF. A good choice for $a(t)$ can be a squared sinusoidal waveform synchronously with the oscillator output sinusoidal voltage. As the ISF of a LC oscillator is maximum when the output voltage is in its zero-crossing points, with this choice for $a(t)$, the equivalent-ISF is zero when the output voltage is in the zero-crossing points. This proposes to have effective squared sine wave current for transistors synchronously with the oscillator output sinusoidal voltage.

3 Sinusoidal Switching VCO

As seen in the previous section, in the LC oscillators, a good choice for the transistors' current is a squared sinusoidal waveform in-phase with the oscillator output voltage. To implement the idea, the oscillator of [5] is used as the reference oscillator and the proposed method is applied on it. The proposed sinusoidal-switched VCO is shown in figure 1. In this figure, the NMOS transistors MB1 and MB2 are biased near the transistor threshold voltage (Vth) by using the MT1 and MT2 transistors. The feedback capacitors Cf1 and Cf2 bring synchronously sinusoidal voltage to the gate of MB1 and MB2. For 0.18u CMOS process with low supply voltage, transistors still follow the long channel equations and the MOS transistor's current is proportional to square of its gate-source voltage. With assumption that the MB1 and MB2 are biased near the NMOS threshold voltage (Vth) and the gate-source voltages

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of these transistors are driven with sinusoidal output voltages, the current of MB1 and the $\boldsymbol{a(t)}$ for normalized oscillation frequency will be:

$$I_D = \frac{\mu}{2} C_{ox} \frac{w}{l} (v_{gs} - v_{th})^2 = \begin{cases} \hat{I}_b . \sin^2(t) & : 0 < t < \pi \\ 0 & : \pi < t < 2\pi \end{cases} \tag{4}$$

$$a(t) = \sin^2(t) \tag{5}$$

where $\hat{I}_b$ is the peak current of the tail transistors. Now, by using $\boldsymbol{a(t)}$ function, the equivalent-ISF ($\mathrm{ISF_{eq}(t)}$) and its $\boldsymbol{rms}$ value ($\mathrm{ISF_{rms}}$) will be expressed as:

$$ISF_{eq}(t) = \frac{\cos(t)}{v_m} . a(t) = \frac{\cos(t)}{v_m} . \sin^2(t) \tag{6}$$

$$ISF^2_{rms} = \frac{1}{\pi} \int_0^{\pi} ISF^2_{eq}(t) . dt = \frac{1}{\pi} \int_0^{\pi} \left[\frac{\cos(t)}{v_m} . \sin^2(t) \right]^2 . dt = \frac{1}{16 v_m^2} \tag{7}$$

$\mathrm{ISF^2_{rms}}$ for traditional LC oscillator, for $\boldsymbol{a(t) = 1}$, is 8 times of the value of (7). So it is clear that the sinusoidal switching can decrease the phase noise based on (1).

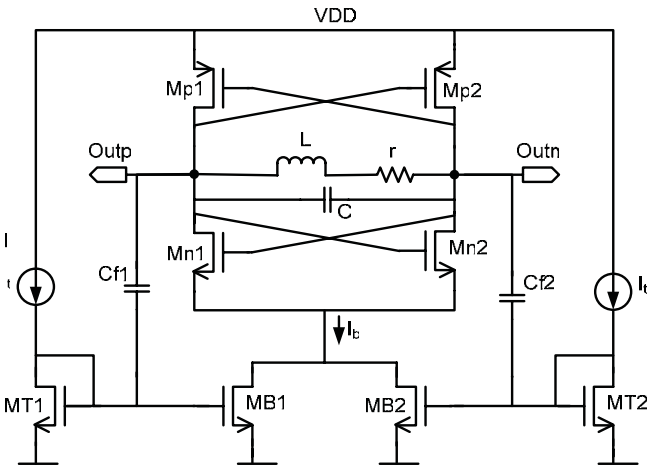

Fig. 1. The Proposed sinusoidal-switched VCO.

4 Proposed QVCO Topology

In the coupled-oscillators techniques to design QVCO, there is a trade off between the quadrature phase accuracy and the oscillator phase noise [1, 2, 3]. Indeed, the phase noise of QVCO's is not as good as the individual VCO's. The degraded phase noise performance of the coupling QVCO's in comparison to the individual VCO's is initially due to the noise coming from the additional coupling transistors and secondly due to shifting the oscillation frequency from the tank natural oscillation frequency to a frequency that causes phase shift between current and voltage of the tank circuit [2, 3]. The shifting of the oscillation frequency decreases the tank effective quality

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factor (Q) and as a result increasing the oscillator phase noise. The cascode-coupling QVCO of [2] uses an efficient coupling scheme for keeping the oscillation frequency near to the tank natural frequency. It reduces phase noise about 6 dB in comparison to the typical QVCO [1] but however, its phase noise is still high.

Another solution to keep the oscillator frequency in the tank natural frequency is to use second order harmonics coupling technique to design QVCO [3]. But coupling of two oscillators with second harmonics is not firm enough to force the oscillators to oscillate in a common frequency and any mismatch in their tank circuits can generate a beat frequency in the output.

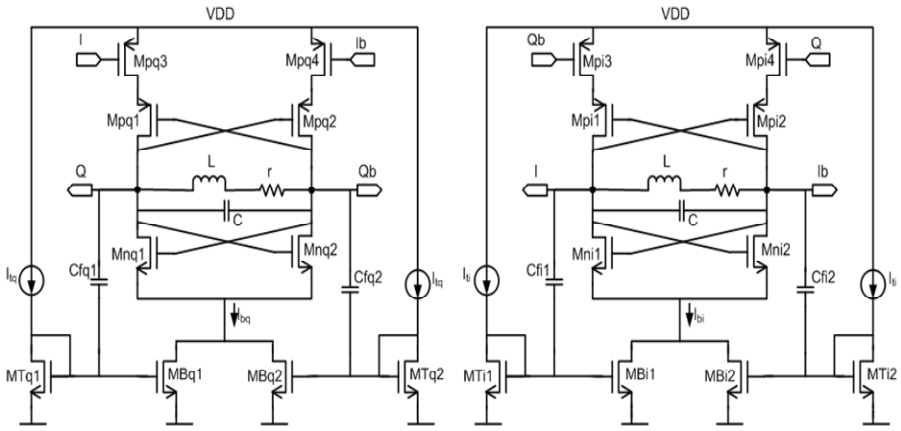

Fig. 2. Proposed QVCO based on sinusoidal-switched VCOs.

The sinusoidal-switched QVCO topology is proposed with combining the proposed sinusoidal-switched VCO and the cascode-coupling method of [2]. The sinusoidal-switched QVCO topology is shown in figure 2 in which transistors Mpi1-Mpi4 and Mpq1- Mpq4 couple two VCOs similar to [2] and transistors MBi1-MBi2 and MBq1-MBq2 make the sinusoidal-switched bias for the QVCO. As the simulation results will show, it gives better phase noise performance than [2] and [3] while it has good quadrature outputs phase accuracy like [2].

5 Simulation Results

Based on the proposed sinusoidal-switched QVCO topology of figure 2, a 1.8 GHz QVCO was designed by using 0.18u CMOS process and a supply voltage of 1.8v. It is assumed that the quality factor (Q) of the used inductor in 1.8 GHz is about 8. As mentioned before, in the oscillator of figure 1, capacitors Cf1 and Cf2 bring the output sinusoidal voltages to the gate of transistors MB1 and MB2 and the gate of these transistors are biased near $\boldsymbol{Vth}$ with high-impedance voltage sources. These high impedance voltage sources are established on two diode-connected NMOS transistors (MT1, MT2) with minimum W and L to have large equivalent resistances in the

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gate of MB1 and MB2. Equivalent resistance of these voltage sources together with Cf1 and Cf2 capacitors will cause phase difference between the oscillator output voltages and the gate voltages of MB1 and MB2. With biasing the gate-source of MB1 and MB2 near NMOS threshold voltage ($\boldsymbol{Vth}$), each of these transistors conducts for half of a sinusoidal period and as assumed in (4), the current of MB1 and MB2 will be square of sinusoidal. The dimension ratio of transistors Mni1-Mni2 and Mpi1-Mpi2 in figure 2 is taken 1 to 3 to have equal g_m for them and the PMOS coupling transistors' dimension is 5-6 times of Mpi1 dimension to have effective phase accuracy [2].

In addition to design a sinusoidal-switched QVCO, two QVCOs based on the SIPC (Source-Injection Parallel Coupling) [3] and the cascode-coupling [2] topologies were designed with the same tank circuit for 1.8 GHz oscillation frequency. The phase noise performance of these oscillators is compared with the same oscillation frequency and the same tank circuit. The phase noise simulation was done by using the SpectreRF advanced PSS and Pnoise analyses. The SpectreRF phase noise simulation result is shown in figure 3. As shown in this figure, the phase noise of the proposed Sinusoidal-switched QVCO is about −134 dBc/Hz at 1 MHz offset frequency thereby showing 3 dB and 5.3 dB phase noise reduction in comparison to the SIPC and cascode-coupling QVCO topologies respectively.

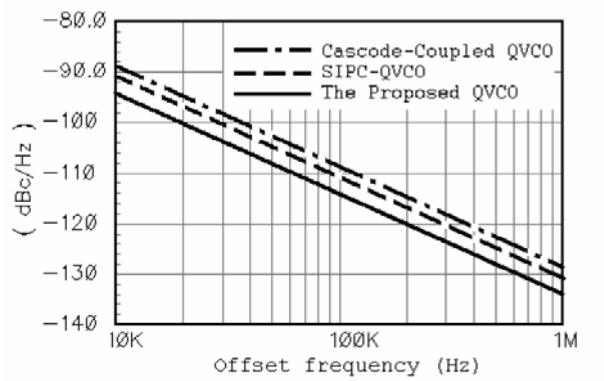

Fig. 3. SpectreRF phase noise simulation for three oscillators.

The power consumption of the proposed QVCO is about 12.6 mW while the power consumption of the designed SIPC and cascode-coupling QVCO is 28.8 mW and 11.2 mW respectively. In another simulation, for oscillation frequency variation from 1.7 GHz to 1.9 GHz, the phase noise of the sinusoidal-switched QVCO at 1 MHz offset frequency from the carrier changes less than ±1 dBc/Hz.

6 Conclusion

A new topology to design low-phase-noise low-power LC-QVCO was proposed. This topology uses oscillator equivalent-ISF shaping to reduce the sensitivity of the oscillator to the transistors' noise and as a result reducing

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the oscillator phase noise. In this QVCO topology, two sinusoidal-switched VCOs were coupled with cascode-coupling method. The 1.8 GHz, 1.8v designed sinusoidal-switched QVCO showed a phase noise of −134 dBc/Hz at 1 MHz offset frequency. This sinusoidal-switched QVCO gives 3 dB and 5.3 dB phase noise reduction in comparison to SIPC and cascode-coupling topologies respectively.

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