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A novel layout placement structure to mitigate the multi-bit-upset in 6T-SRAM cell

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Abstract: A novel layout structure for the typical 6T-SRAM cell is designed to mitigate the single-event induced MBU. And three-dimensional technology computer-aided design (TCAD) numerical simulation is used to evaluate the MBU hardening performance of this novel layout structure. Compared to other layout structures, our proposed layout can effectively attenuate the single-event induced MBU in typical 6T-SRAM with little area and power penalty.

Keywords: SRAM, single error correction, MBU, layout structure

Classification: Integrated circuits

References

[1] T. Heijmen, P. Roche, G. Gasiot, K. R. Forbes and D. Giot: IEEE Trans. Device Mater. Reliab. **7** (2007) 84. DOI:10.1109/TDMR.2007.897517

[2] T. Calin, M. Nicolaidis and R. Velazco: IEEE Trans. Nucl. Sci. **43** (1996) 2874. DOI:10.1109/23.556880

[3] S. M. Jahinuzzaman, D. J. Rennie and M. Sachdev: IEEE Trans. Nucl. Sci. **56** (2009) 3768. DOI:10.1109/TNS.2009.2032090

[4] P. Reviriego, J. A. Maestro, S. Baeg, S. Wen and R. Wong: IEEE Trans. Nucl. Sci. **57** (2010) 2124. DOI:10.1109/TNS.2010.2042818

[5] S. Yoshimoto, T. Amashita, S. Okumura, K. Yamaguchi, M. Yoshimoto and H. Kawaguchi: IRPS (2011) 876. DOI:10.1109/IRPS.2011.5784596

[6] T. Uemura, R. Tanabe and H. Matusyama: IRPS (2012) 5B.4.1. DOI:10.1109/IRPS.2012.6241846

[7] S. Yoshimoto, T. Amashita, S. Okumura, K. Nii, H. Kawaguchi and M. Yoshimoto: IRPS (2012) 5B.5.1. DOI:10.1109/IRPS.2012.6241847

[8] O. A. Amusan, A. L. Witulski, L. W. Massengill, B. L. Bhuva, R. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black and R. D. Schrimpf: IEEE Trans. Nucl. Sci. **53** (2006) 3253. DOI:10.1109/TNS.2006.884788

[9] P. Reviriego, J. A. Maestro and C. Cervantes: IEEE Trans. Device Mater. Reliab. **7** (2007) 592. DOI:10.1109/TDMR.2007.910443

[10] N. Mahatme and B. Bhuva: IRPS (2011) 891.

[11] B. D. Olson, O. A. Amusan, S. Dasgupta, L. W. Massengill, A. F. Witulski, B. L. Bhuva, M. L. Alles, K. M. Warren and D. R. Ball: IEEE Trans. Nucl. Sci. **54** (2007) 894. DOI:10.1109/TNS.2007.895243

[12] B. Narasimham, J. W. Gambles, R. L. Shuler, B. L. Bhuva and L. W. Massengill: IEEE Trans. Nucl. Sci. **55** (2008) 3456. DOI:10.1109/TNS.2008.2007119

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[13] S. Chen, Y. Du, B. Liu and J. Qin: IEEE Trans. Nucl. Sci. **61** (2014) 646. DOI:10.1109/TNS.2014.2298889

1 Introduction

As the feature size of integrate circuits (ICs) scales, the space radiation induced soft errors are becoming one of the major issues for the circuit reliability. When the energy particles existing in space travel through semiconductor materials, created minority carriers may be collected by the drain. This will perturb the voltage and create a voltage transient. If the data in the storage element changes due to the voltage transient, this is referred to a single event upset (SEU). Previous research has illustrated that the vulnerability of stored elements to SEU is increasing with technology scaling [1].

Static random access memory (SRAM) is a key component in modern ICs. Once the data stored in the SRAM is changed, this might result in system failure. Thus, lots of approaches at different levels have been designed to harden the SRAM against SEU [2, 3, 4, 5, 6, 7]. Of these hardening methods, single error correction (SEC) is an effective approach to mitigate the SEU in SRAM. However, due to the scaled technologies, charge sharing is becoming more and more prominent [8]. This has increased the ratio of multiple cell upsets (MCU) and multiple bit upsets (MBU) in SRAM. The SEC technique cannot deal with MBU [9].

In this paper, we propose a novel layout structure to mitigate the MBU in 6T-SRAM. This technique can be applied to both the twin-well and deep N-well process with little performance penalty. Three-dimensional technology computer-aided design (TCAD) numerical simulation is conducted to evaluate the hardening performance of this novel layout structure.

2 Related works

Fig. 1(a) presents the typical 6T-SRAM cell structure, and Fig. 1(b) shows the corresponding layout structure. In this structure, the NMOS transistors are placed in two separate P-wells, and the PMOS transistors are placed in one N-well. This layout structure is widely studied by the researchers [10].

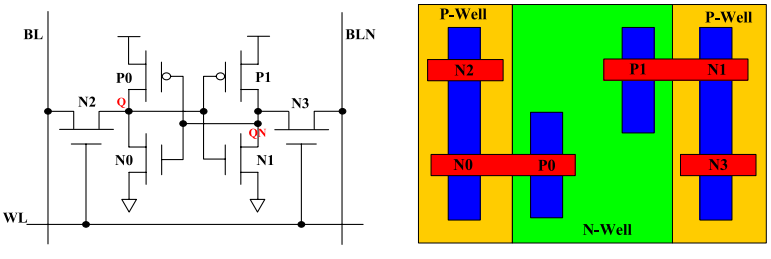

Fig. 1. Circuit and layout structure of the typical 6T-SRAM, (a) circuit structure, (b) layout structure.

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Fig. 2 presents the layout placement of two SRAM cells. *Cell1* and *Cell2* are in the same word. These two cells are adjacent to each other in the layout. The transistor N1 and N3 in *Cell1* are in the same well with the transistor N2 and N0 in *Cell2*. As charge sharing is more likely to occur in the same well, the transistor N0 and transistor N1 might be simultaneously affected when the ions strike on the region marked in Fig. 2. This might make both the *Cell1* and *Cell2* upset. Under this situation, the SEC technique becomes invalid.

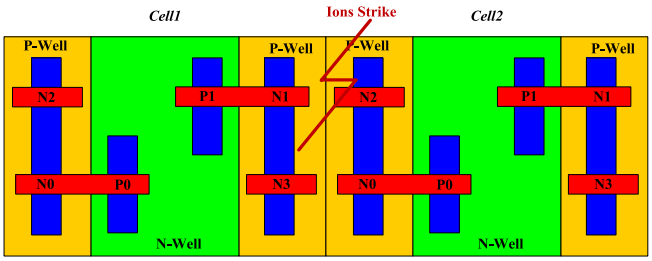

Fig. 2. Two adjacent cells in the same word.

To mitigate the upset of *Cell1* and *Cell2*, several techniques are designed. The technique with using bit-line alternation and narrow deep N-well can effectively mitigate MBU [6]. However, this technique is related to the process hardening. It is difficult to be implemented in the typical twin-well and deep N-well process. A layout structure that makes the NMOS transistors in the same well is designed in [7] as presented in Fig. 3. This layout structure can also achieve well performance to mitigate MBU. But this technique is applied to the deep N-well process. For the typical twin-well process, the bipolar amplification effect is more pronounced in PMOS transistors [11, 12]. This will increase the charge collected by the adjacent PMOS transistors in the two adjacent SRAM cells. And the hardening performance is decreased.

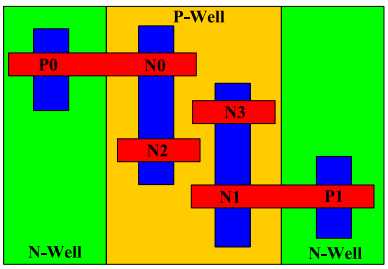

Fig. 3. NMOS-inside layout structure.

3 Layout structure with separate PMOS transistors

To efficiently mitigate MBU both in the twin-well and deep N-well process, we propose a novel layout structure as presented in Fig. 4. Fig. 4(a) is the circuit structure, and Fig. 4(b) is the layout structure. This layout structure combines two techniques to mitigate MBU. The first technique is to make the NMOS transistors in one N-well as proposed in [7], and the other technique is to split the transistor P0 into two transistors and to place these two transistors into two separate well.

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As the size of PMOS transistors is smaller than the size of NMOS transistors in the commercial 6T-SRAM, the read/write time of this SRAM cell will be little affected by adopting this structure. Another benefit of this layout structure is that the area for this layout presented in Fig. 4(b) is almost the same as the one shown in Fig. 1(b).

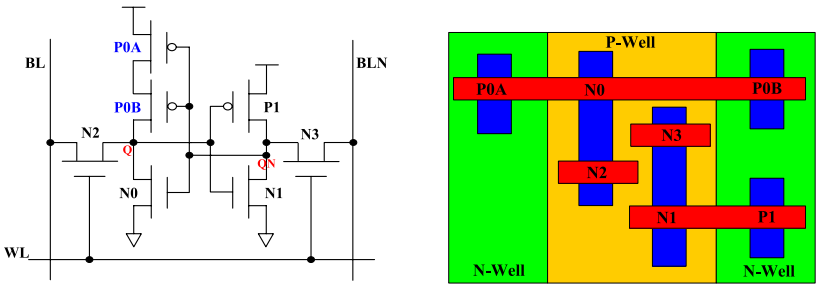

Fig. 4. SRAM structure with separate PMOS transistors, (a) circuit structure, (b) layout structure.

The principle of this structure to mitigate the MBU can be expressed below. Fig. 5 presents the two SRAM cells that using the proposed layout structure. These two cells are assumed to be in the same word. The state of transistor P1 in *Cell1* and transistor P0A is *Cell2* are in the off-state. As the state of P0B in *Cell2* is the same with the one of P0A in *Cell2*, the state of P0B in *Cell2* is also in off-state. Thus, when ions strike on the N-well shown in Fig. 5, no matter what the drain value of transistor P0A in *Cell2* is, the drain value of transistor P0A in *Cell2* cannot propagate to the drain of transistor P0B in *Cell2*. Anyway, the strike on the N-well shown in Fig. 5 cannot upset *Cell2* due to the off-state transistor P0B. And no MBU will appear under this situation.

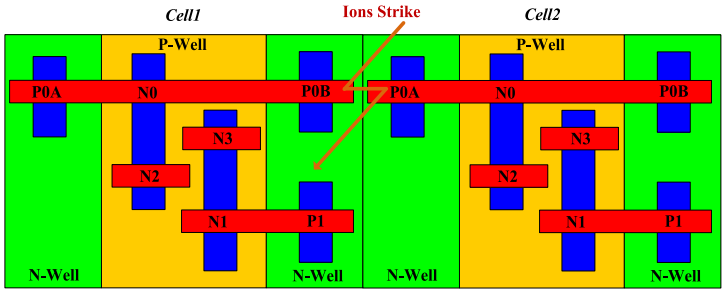

Fig. 5. Two adjacent SRAM cells with separate PMOS transistors in the same word.

4 Simulation and discussion

4.1 Simulation setup

Due to the good look-inside capability, the three-dimensional TCAD numerical simulation is widely used for investigating the mechanism of single-event

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charge collection [13]. In this section, the three-dimensional TCAD simulation is adopted to investigate the MBU hardening performance of our proposed SRAM structure. To have a comparison, the normal layout in Fig. 1(b), the NMOS-inside layout in Fig. 3 and our proposed layout structure in Fig. 4(b) are all simulated. And the typical twin-well process is considered.

These three SRAM layout structures are implemented by using the commercial 65 nm CMOS process. For the layout in Fig. 1(b), the width of P-well is 0.7 µm and the width of N-well is 0.8 µm. For the layout in Fig. 3 and Fig. 4(b), the width of P-well is 1.2 µm and the width of N-well is 0.5 µm. The size of the PMOS transistors in these three structures is all W : L = 200 nm : 60 nm. The size of the NMOS transistors in these three structures is all W : L = 400 nm : 60 nm. The PMOS and NMOS three-dimensional TCAD models are calibrated to match the electrical characteristics based on the commercial 65 nm CMOS PDK.

To simulate the MBU hardening performance, the simulated structure is constructed by two adjacent SRAM cells. Fig. 6(a) shows the simulated structure for the normal layout in Fig. 1(b). As the transistor N1 in *Cell1* and the transistor N0 in *Cell2* are in the same well, these two cells are modeled as the three-dimensional TCAD numerical models and the other transistors are modeled as the corresponding SPICE models. Fig. 6(b) shows the simulated structure for the NMOS-inside layout in Fig. 3. As the transistor P1 in *Cell1* and the transistor P0 in *Cell2* are in the same well, these two cells are modeled as the three-dimensional numerical model and the other transistors are modeled as the corresponding SPICE models. Fig. 6(c) shows the simulated structure for our proposed layout in Fig. 4(b). The transistor P0B in *Cell1*, transistor P1 in *Cell1* and the transistor P0A in *Cell2* in the same P-well are modeled as the three-dimensional numerical model. The other transistors are modeled as the corresponding SPICE models.

To extensively study the MBU hardening performance of these three layouts, several incident locations are chosen as presented in Fig. 7. For all the three layout structures, twenty points are selected. And the space between the adjacent points is 0.2 µm. During the simulation, the incident ions will strike each point normally. For the structure in Fig. 6(a), the value of Q in *Cell1* is set as LOW, and the value of Q in *Cell2* is set HIGH. For Fig. 6(b) and Fig. 6(c), the value of Q in *Cell1* is set as HIGH, and the value of Q in *Cell2* is set as LOW. During the simulation, the supply voltage is set as 1.0 V.

During the simulation, the following physical models are used: 1) Fermi-Dirac statistics; 2) band-gap narrowing effect; 3) doping-dependent SRH recombination and Auger recombination; 4) temperature, doping, electric field, and carrier-carrier-scattering impact on mobility; 5) incident heavy ions are modeled using a Gaussian radial profile with a characteristic 1/e radius of 50 nm and a Gaussian temporal profile with a characteristic decay time of 0.25 ps; and 6) a hydrodynamic model is used for carrier transportation. Unless otherwise specified, the default models and parameters provided by Sentaurus TCAD vE-2010.12 are used.

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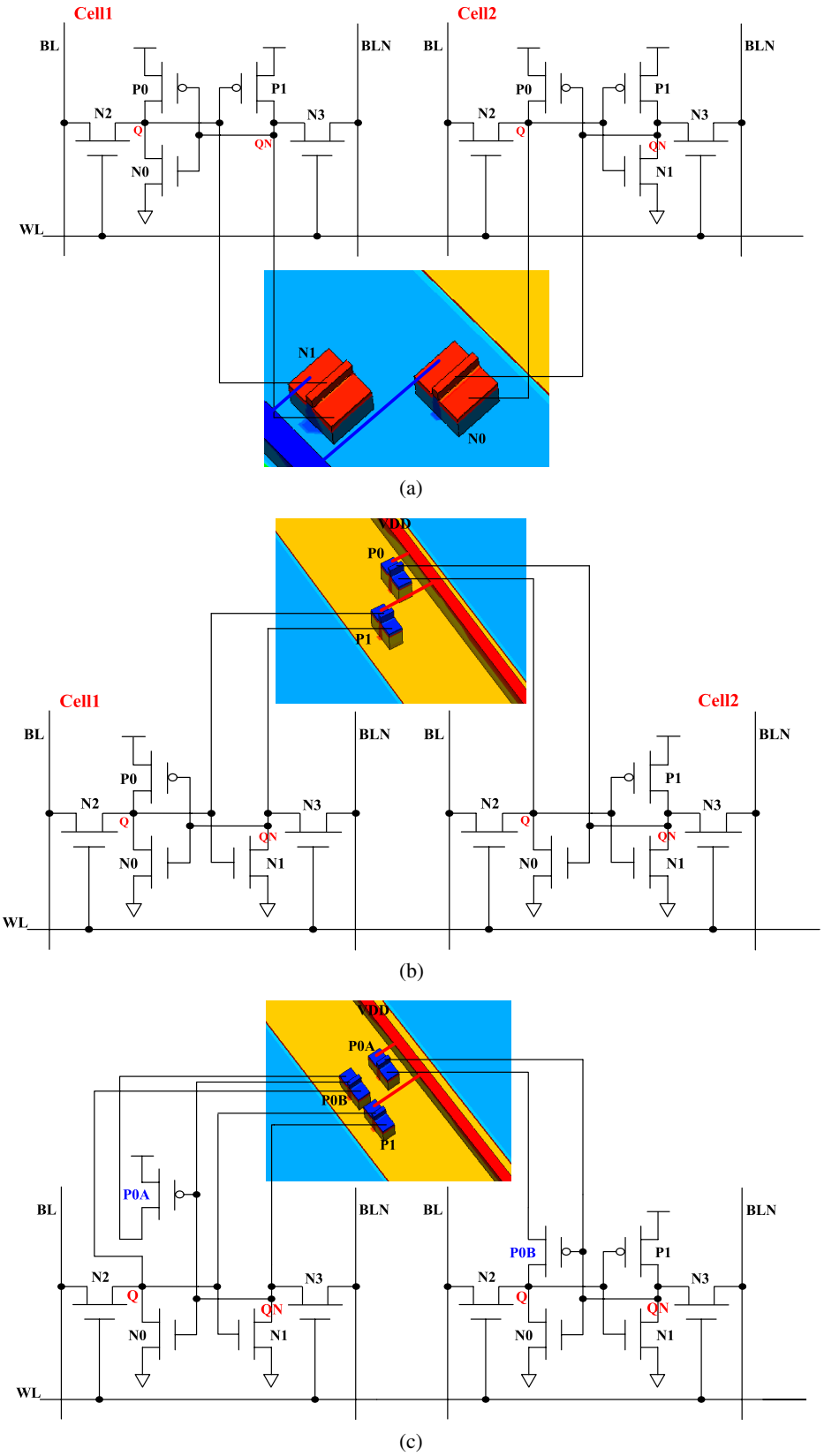

Fig. 6. Simulated structure to evaluate the MBU hardening performance, (a) the normal layout in Fig. 1(b), (b) the NMOS-inside layout in Fig. 3, (c) our proposed layout in Fig. 4(b).

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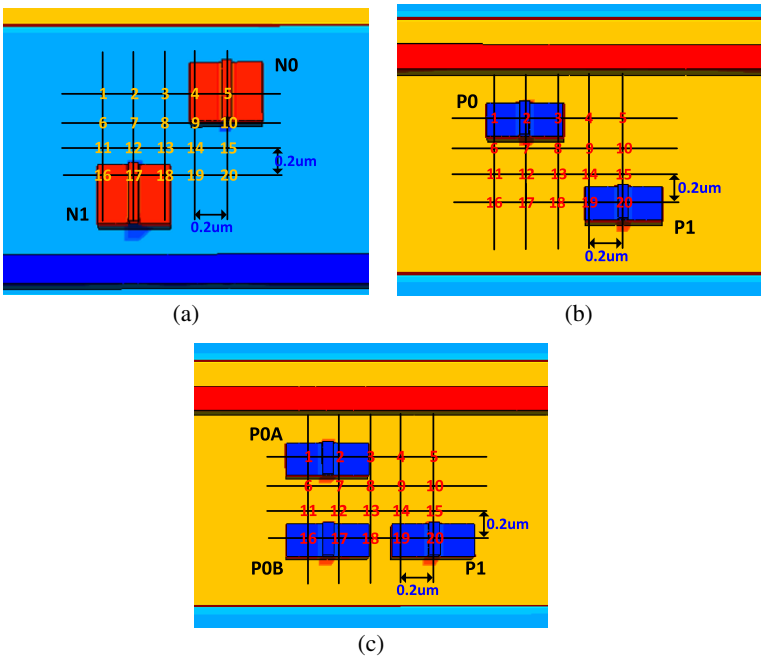

Fig. 7. Simulated ions incident location for the three layout structures. (a) the normal layout in Fig. 1(b), (b) the NMOS-inside layout in Fig. 3, (c) our proposed layout in Fig. 4(b).

4.2 Simulation results and discussion

Table I presents the number of occurred MBU for these three layout structures when ions with different LETs strike the twenty points in Fig. 7.

Table I. Simulation results for the number of occurred MBU for these three layout structures

Process	LET (MeV·cm^2/mg)	Number of MBU		
		Normal Layout	NMOS-Inside Layout	Our Proposed Layout
Typical twin-well process	30	1	8	0
	40	3	11	0
	50	4	16	0

From this table, it can be seen that no MBU occurs for our proposed layout structure when ions strike these twenty points. For the other two layout structures, the single-ion strike will induce MBU. For the normal layout structure in Fig. 1(b), as the bipolar amplification effect is not evident in NMOS transistors, charge sharing between the transistor N0 and transistor N1 in Fig. 7(a) is weak. The number of MBU is not much. However, for the deep N-well process, bipolar amplification effect is more serious in NMOS transistors, this will increase the MBU ratio [7, 11]. For the NMOS-inside layout structure in Fig. 1(c), the reason of the high number of MBU is that the bipolar amplification effect is more evident in PMOS transistors in typical

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twin-well process [11, 12]. This layout structure is mainly applied to the deep N-well process.

Fig. 8 presents the circuit response for our proposed layout structure in Fig. 6(c) when ions with LET of 50 MeV·cm^2/mg strike point 8 in Fig. 7(c). The ions strike time is at 500 ps. It can be seen that the *Cell1* is upset. For *Cell2*, although the voltage at the drain of transistor P0A is Cell2 in Fig. 6(c) is HIGH, the voltage cannot propagate to the drain of transistor P0B due to the off-state transistor P0B. The Cell2 is not upset.

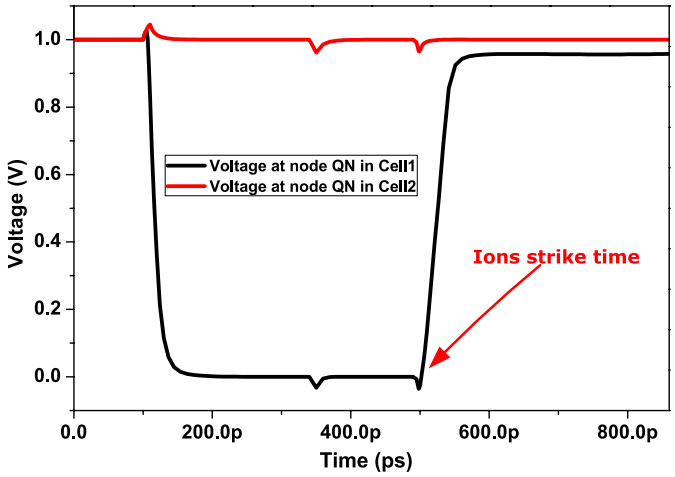

Fig. 8. Circuit response for our proposed layout structure in Fig. 6(c) when ion with LET of 50 MeV·cm^2/mg strikes point 8 in Fig. 7.

5 Conclusion

In this paper, we propose a novel layout structure to mitigate the MBU in typical 6T-SRAM. Two techniques are adopted in this layout structure. The first technique is to place the NMOS transistors in one N-well, and the other is to split the PMOS transistor into two transistors and to place these two transistors into two separate well. Three-dimensional TCAD numerical simulation shows that this layout structure can effectively attenuate MBU.

With the technology scales, the single-event induced multi-node charge collection will be more and more serious. This will increase the occurrence of MBU in 6T-SRAM. This will present a challenge for the SEC technique. The new layout and circuit structures of SRAM cells that can effectively mitigate MBU are expected in the future design.

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