

# Modeling and analysis of inter-symbol interference (ISI) jitter

Kyung Ki Kim<sup>a)</sup>

Department of Electrical and Computer Engineering,  
Northeastern University, Boston, MA 02115, USA

a) [kkkim@ece.neu.edu](mailto:kkkim@ece.neu.edu)

**Abstract:** This paper presents a novel modeling and analysis of inter-symbol interference (ISI) jitter in serial data channels either between chips or on chip. The simulation results show that ISI jitter is dependent on pole location, settling time, and damping ratio of the data serial channel. Based on the proposed ISI jitter model, the effect of the ISI jitter on other jitter components is illustrated along with realistic simulation results.

**Keywords:** ISI jitter, timing jitter, serial data channel

**Classification:** Integrated circuits

## References

- [1] Wavecrest Corp., *Understanding Jitter*, application note, 2001.
- [2] J. Buckwalter, B. Analui, and A. Hajimiri, "Predicting Data-Dependent Jitter," *IEEE Trans. Circuits Syst. II*, vol. 51, no. 9, pp. 453–457, Sept. 2004.
- [3] J. Buckwalter, B. Analui, and A. Hajimiri, "Data-Dependent Jitter and Crosstalk-Induced Bounded Uncorrelated Jitter in Copper Interconnects," *IEEE Int. Microwave Symp.*, vol. 3, pp. 1627–1630, June 2004.
- [4] T. J. Yamaguchi, M. Soma, M. Ishidal, M. Kurosawa, and H. Musha, "Effects of Deterministic Jitter in a Cable on Jitter Tolerance Measurements," *IEEE International Test Conference (ITC)*, vol. 1, pp. 58–66, Sept. 2003.
- [5] R. C. Drof and R. H. Bishop, *Modern Control System*, Prentice-Hall, 2000.
- [6] R. Sun and M. Li, "A Generic Test Path and DUT Model for DataCom ATE," *IEEE International Test Conference (ITC)*, vol. 1, pp. 528–536, Sept. 2003.
- [7] M. Shimanouchi, "New Paradigm for Signal Paths in ATE Pin Electronics are Needed for Serialcom Device Testing," *IEEE International Test Conference (ITC)*, pp. 903–912, 2002.

## 1 Introduction

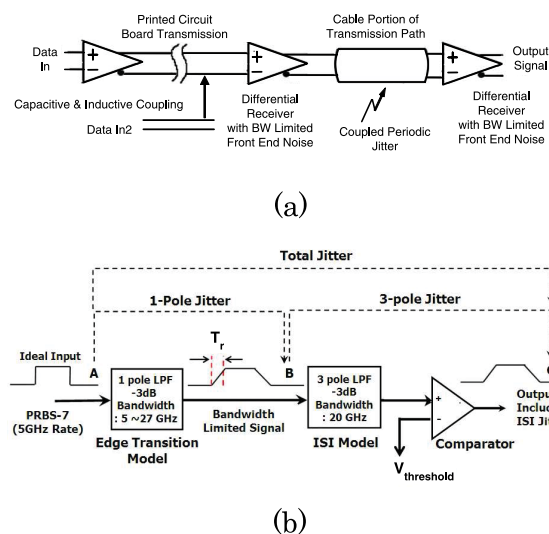
As the data rate of VLSI system increases, serial data channels either between chips and even on chip become more significant in the system for timing accuracy. Digital serial data have to be transmitted at high speed in the channels, and the typical data rate is 5 Gbits/sec. Transmission paths of the digital

data are different; Some of the lines are incorporated in printed circuit board etch, and some of the lines are differential cables. Typical transmission path lengths are around 4 nsec in term of delay. The transmission path is fairly lossy at the data rate specified. Usually, the transmission path is fairly lossy at the specified data rate and is shown in block diagram in Fig. 1 (a). Due to the stubs and impedance mismatches, the transmission paths have significantly long step response what introduces inter-symbol interference (ISI) jitter. Other interfering signals may be present near the transmission path and may inject normal-mode signal into the differential driver inputs [1].

Therefore, modeling ISI jitter is required to analyze the high-speed serial data channel. The motivation of the paper is to investigate how the increase in the ISI jitter can be predicted as a function of pole location, settling time, and damping ratio. Although some papers have been published on this ISI jitter model for the serial data channel, they usually focused on mathematical jitter model [2, 3]. In this paper, a new ISI jitter analysis for serial data channel is proposed along with Matlab results, and the effect of the ISI jitter on other jitter components is illustrated.

## 2 ISI Jitter Model

ISI jitter is dependent on many features, such as high and low lengths of data pattern, data rate, settling time of the LPF step response, and the frequency bandwidth (or edge transition time) of the data. T. J. Yamaguchi, et al. [4] has shown that the edge transition time of data is a function of its patterns and the high and low lengths of each pattern. In [6], a 2-pole test path model and a 1-pole device under test (DUT) model were suggested; however, no analysis has been pursued on the pole location of the LPF and the settling time and the damping ratio of the LPF step response. Therefore, the relationships between the settling time and the ISI jitter, the damping



**Fig. 1.** Data path model: (a) Block diagram of data path, (b) Block diagram of ISI jitter model

ratio and the ISI jitter, and the pole location and ISI jitter have not been addressed. The proposed ISI jitter model has a LPF with bandwidth limiting effects and ringing. Figure 1 (b) shows the block diagram of the proposed ISI jitter model. The input signal is an ideal square wave (with no transition time). The 1-pole LPF corresponds to the edge transition model that is used to generate the finite transition time in the input signal. The natural frequency of this LPF is chosen to be sufficiently high such that no ISI jitter is generated. The 3-pole LPF is used to generate the ISI jitter. This LPF is the concatenation of a 1-pole LPF (representing the limited-bandwidth effect of the DUT) and a 2-pole LPF (representing the ringing effect of the transmission media, such as connectors and cables) [6]. The second order system is the simplest model for the connectors and transmission media. The second order model is required to include under-damped response that results in ringing effect. The edge transition time ( $T_r$ ) of the bandwidth limited data is inversely proportional to the pole location, or the  $-3$  dB bandwidth of the path model [7]; this is expressed by

$$f_{-3dB} = \frac{0.35}{T_r} \quad (1)$$

where  $f_{-3dB}$  is the  $-3$  dB bandwidth frequency, and  $T_r$  is the edge transition time (10 – 90% of the transition time).

In the proposed model, the input is a pseudo-random binary sequence (PRBS)-7 with 5 Gbits/sec. To change the edge transition time of the input data, the pole location ( $-3$  dB bandwidth) of the edge transition model is changed from 5 GHz to 27 GHz as shown in Fig. 1 (b). The  $-3$  dB bandwidth of the 3-pole LPF is 20 GHz and this 3-pole system is a concatenation of a 1-pole system (a real pole, at 16 GHz) and a 2-pole system that has imaginary poles at  $(-7.85 \pm 18i)$  GHz and a damping ratio of 0.4 for under-damped response and ringing. In this model, three peak-to-peak jitter measurements are taken, i.e. between A and (1-pole Jitter), B and C (3-pole Jitter), and A and C (Total Jitter), as indicated on Fig. 1 (b).

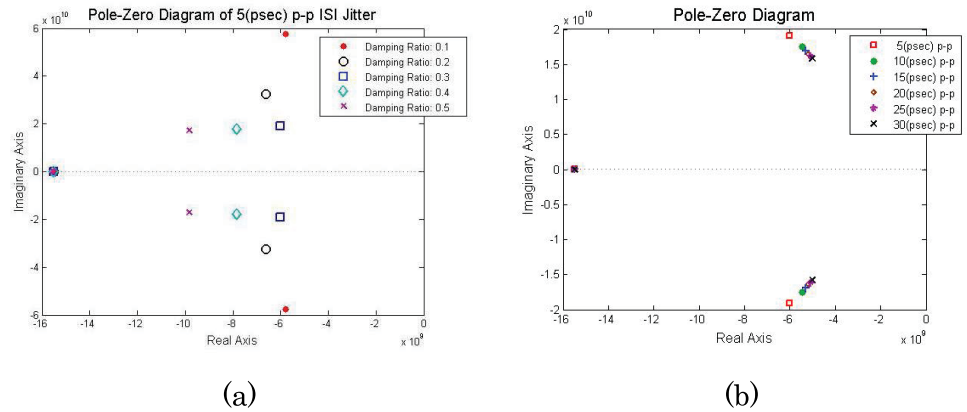
### 3 Pole Location of ISI Jitter Model

Figure 2 shows the effect of the pole location on the ISI jitter. The peak-to-peak value of the jitter has been used; even though the peak-to-peak jitter (5 psec) is the same, the pole locations of the three-pole LPF are different; the damping ratio is also changed as shown in Fig. 2 (a). The damping ratio is related to the settling time of the LPF step response. Assuming that the settling time for the second order model is the time it takes to fall within 5% of the steady state value for a step input, this relationship is given by [5]

$$T_{set} = \frac{3}{\xi\omega_n} \quad (2)$$

where  $T_{set}$  is the settling time of the LPF step response,  $\xi$  is the damping ratio of the LPF, and  $\omega_n$  is the natural frequency of the LPF.

This analysis shows that the settling time can change the ISI jitter as predicted in [6]. Moreover, Fig. 2 (b) shows that if the damping ratio is fixed



**Fig. 2.** Pole-Zero diagram of the ISI jitter model, (a) Pole-Zero diagram of ISI jitter with different damping ratio, (b) Pole-Zero diagram of different ISI jitters with same damping ratio(0.4)

to 0.4, the ISI jitter increases as the imaginary and real pole locations shift to the lower frequency, i.e. the slow decay and small ringing of the LPF step response cause an increase in ISI jitter.

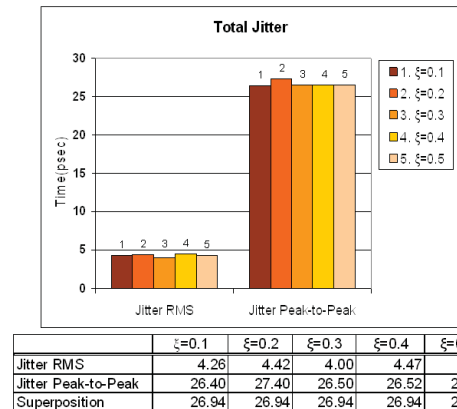
Physical media can induce jitter through two possible sources. The first source is due to the reflection by impedance mismatching at the termination, thus causing signal distortion. Reflection is dominated by the characteristic impedance and the reflection coefficient of the transmission line. In the simulations, signal distortion is significant when the reflection coefficient is negative at both the input and the output of the transmission. Therefore, the amount of jitter increases. High-frequency losses caused by the skin effect and the dielectric loss also affect ISI jitter. They are related to frequency; the skin effect is proportional to the square root of the frequency, while the dielectric loss is linearly proportional to frequency. Therefore, the skin effect dominates data loss at a lower frequency, whereas the dielectric loss dominates at a higher frequency. These effects have not yet been simulated thoroughly.

#### 4 Settling Time and Damping Ratio of ISI Jitter Model

As analyzed in [6], the settling time of the step response of the LPF is defined as the system memory length; the length should be greater than 2 unit intervals (UIs) to observe the ISI jitter caused by the high/low run length beyond two UIs. Figure 3 shows the effects of the settling time on total jitter (TJ) by using the five pole locations as in Fig. 2. As shown in Fig. 3(a), the peak-to-peak jitter value of all five cases is 5 psec, but the damping ratio (that primarily determines the settling time of the LPF) is changed from 0.1 to 0.5. The settling time and RMS value of the ISI jitter in the 3-pole ISI jitter model are changed depending on the damping ratio of the 2-pole LPF. The largest settling time for the five cases occurs not at a damping ratio of 0.1, but at 0.3 due to the effect of the 1-pole LPF. Figure 3(b) shows the magnitude of the peak-to-peak value and RMS value of TJ for different values of  $\xi$  (the

Settling Time (psec)	Damping Ratio	ISI <sub>rms</sub> (psec)
0.332	0.5	1.99
0.467	0.4	2.13
0.590	0.3	1.46
0.454	0.2	2.28
0.416	0.1	2.19

(a)



(b)

**Fig. 3.** Jitter vs. Settling time of ISI jitter, (a) Effect of damping ratio, (b) TJ for each damping ratio of LPF

damping ratio of the 2-pole LPF). Despite the different settling times and pole locations, the peak-to-peak value is almost the same (within a 2% difference). Hence, for this experiment superposition holds for TJ with different values of settling time provided the same peak-to-peak value is encountered.

When the damping ratio is 0.2, then the measured peak-to-peak value of TJ has the largest value (albeit, a damping ratio of 0.3 results in a larger settling time than for 0.1). This implies that a large settling time does not always guarantee a TJ of large value when the 3-pole LPF is utilized. Throughout this experiment, a rising time of less than 1 UI, and a settling time greater than 2UIs have been used; they generate a larger than expected value for the jitter. In Fig. 3(b), the measured peak-to-peak value of TJ is modestly greater than the value obtained by superposition of the jitter components. This seems to suggest that as the sum of all jitter components accounts for the worst timing error, the measured peak-to-peak value of TJ is always less than this sum. Also, a large settling time and a small rising time can cause the jitter to have a larger value than the injected one.

## 5 Experimental Results

In this experiment, the input data is given by an ideal square wave of pseudo-random data, in this case PRBS-7 signal pattern is used; it has a length of  $2^7 - 1 = 127$  bits. This pattern is repeated 40 times such that a total of  $127 \times 40 = 5080$  bits are simulated. The bit rate of the data pattern generator is 5G bits/sec, and the sampling rate of the simulator is 1,000 samples/bit cell. The ISI jitter model consists of a 2-pole LPF (poles at  $(-10 \pm 17.3i)$  GHz) concatenated with a 1-pole LPF (pole at 17 GHz). For real modeling for the serial data channel, other jitter components are injected: random jitter(RJ), periodic jitter(PJ), and duty cycle distortion(DCD) jitter. The jitters has been measured using its eye-diagram and histogram.

In the first experiment, the RJ is fixed to 2.44 psec rms and 34.33 psec

peak-to-peak whereas the ISI jitter is changed from 5 psec to 25 psec peak-to-peak to show the effect of ISI jitter on RJ. The results presents that the measured TJ is almost the same as the superposition of the RJ and the ISI jitter. However, the measured RJ is a little greater than the injected RJ, while the measured ISI jitter is a little smaller than the injected ISI jitter. To be exact, the ISI jitter has a little effect on the RJ within 10% difference i.e. The RJ is increased and the ISI jitter is decreased when the RJ and the ISI jitter are combined. Therefore, the measured TJ is almost the same as the superposition of the RJ and the ISI jitter.

In the next experiment, the ISI jitter is changed from 5 psec to 30 psec peak-to-peak where as the PJ is fixed to 15 psec peak-to-peak to show the effect of ISI jitter on PJ. The experiment result presents that the ISI jitter have no effect on the PJ, i.e. the amount of measured TJ is the same as the superposition of the PJ and the ISI jitter. Also the TJ is the same as the summation of the PJ and the ISI jitter although the PJ varies and the ISI jitter is fixed.

Finally, ISI and DCD jitters are combined. These two jitter components are included in the data dependent jitter, therefore the dependency between the two might be expected. Two different experiments are performed to look into the relationship between the TJ and the superposition of the ISI and the DCD jitter. The first experiment for the ISI jitter and the DCD jitter is for a fixed DCD jitter (15 psec peak-to-peak) and a varying ISI jitter (from 5 psec to 30 psec peak-to-peak). In this case, the TJ is about 2 psec peak-to-peak smaller than the superposition of the ISI jitter and the DCD jitter, and the value (2 psec) changes very little even though the injected ISI jitter changes. The difference between the measured TJ and the superposition of the RJ and the ISI jitter is within 5%. Therefore, the effect of the ISI jitter on the DCD jitter can be ignored. The second experimentation for the ISI jitter and the DCD jitter is for a fixed ISI jitter (20 psec peak-to-peak) and a varying DCD jitter (from 5 psec peak-to-peak to 30 psec peak-to-peak). In this experiment, the difference between the measured TJ and the superposition of the ISI jitter and the DCD jitter is increased as the DCD jitter increases. Especially, when the DCD jitter is 50 psec, the difference is over 10%, which means the ISI jitter is impacted by the DCD jitter. However, since the typical DCD jitter is smaller than the ISI jitter, it can be claimed that the superposition applies to the combining of the ISI jitter and the DCD jitter.

## 6 Conclusion

This paper has developed the ISI jitter model with a 3-pole LPF, and analyzed it using Matlab. The experiments show that the ISI jitter is dependent on pole location, settling time, and damping ratio of the data serial channel. Also, the dependence of the ISI jitter on other jitter components is illustrated. This paper will be very useful in characterizing data dependent jitter, and be a cornerstone in standardization of jitter measurement.