

Experimental demonstration of a ferroelectric FET using paper substrate

Changhwan Shin¹, Gwang-Geun Lee², Dae-Hee Han^{1,2},
Seung-Pil Han³, Eisuke Tokumitsu², Shun-Ichiro Ohmi²,
Dong-Joo Kim⁴, Hiroshi Ishiwara^{2,5}, Minseo Park⁶,
Seung-Hyun Kim⁷, Wan-Gyu Lee⁸, Yun Jeong Hwang⁹,
and Byung-Eun Park^{1,2,4a})

¹ School of Electrical and Computer Engineering, University of Seoul,
163 Seoulsiripdae-ro, Dongdaemun-gu, Seoul 130–743, Korea

² Interdisciplinary Graduate School of Science and Engineering,
Tokyo Institute of Technology, Yokohama 226–8503, Japan

³ Department of Biomolecular Engineering, Tokyo Institute of Technology, Japan

⁴ Materials Research and Education Center, Auburn University, AL 36849, U.S.A.

⁵ Department of Physics, Konkuk University, Seoul 143–701, Korea

⁶ Department of Physics, Auburn University, Auburn, AL 36849, U.S.A.

⁷ School of Engineering, Brown University, Providence, RI 02912, U.S.A.

⁸ Department of Nano CMOS, National NanoFab Center, Daejeon 305–806, Korea

⁹ Clean Energy Research Center, Korea Institute of Science and Technology, Korea
a) pbe@uos.ac.kr

Abstract: A ferroelectric field-effect transistor on a cellulose paper for nonvolatile memory application is fabricated by a low-cost solution-based-only fabrication process. A ferroelectric material, poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)), is used to obtain a wide threshold voltage (V_{TH}) window of ~ 20 V for the transistor on paper. An on/off current ratio of $\sim 10^2$ is also obtained with a semiconducting channel material, Poly(3-hexylthiophene) (P3HT).

Keywords: ferroelectric transistor, paper substrate, P(VDF-TrFE), P3HT

Classification: Electron devices, circuits, and systems

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1 Introduction

The original concept of single-transistor-type (1T-type) ferroelectric gate field-effect transistor (FeFET) was proposed in 1957 [1]. The interface characteristics of the metal-ferroelectric-semiconductor (MFS) structure were poor, due primarily to the inter-diffusion of the constituent elements. This led to various technical challenges such as high leakage current and fatigue issues. The MFS structure with an insulation buffer layer in between the ferroelectric layer and semiconductor would suppress the leakage current.

Organic electronics have recently been attractive for display, radio-frequency identification (RFID), and thin-film transistor (TFT) applications. Particularly, organic field-effect transistors (OFETs) in the field of organic electronics have received considerable attention due to their low-cost fabrication. Poly(vinylidene fluoride), or PVDF, and its copolymer Poly(vinylidene fluoride-trifluoroethylene), or P(VDF-TrFE), have also received much attention, due to their solution process, low-temperature process, and ferroelectric properties. Various applications using these materials have been studied, such as OFETs, piezoelectric and pyroelectric devices. Some of the researchers have reported on nonvolatile memory applications of thin polymer films. S. S. Möller et al. [2] demonstrated the polymer/semiconductor write-once read-many-times memory (WORM) with poly(3,4-ethylenedioxythiophene), or PEDOT. And, R. C. G. Naber et al. [3] demonstrated a nonvolatile memory device with P(VDF-TrFE) and poly[2-methoxy, 5-(2-ethyl-hexyloxy)-p-phenylene-vinylene], or MEH-PPV. However, most of the devices for nonvolatile memory applications were fabricated on plastic and glass substrates [4, 5]. In this study, for the first time, an organic nonvolatile ferroelectric random access memory device is fabricated on a cellulose paper substrate by all-solution processing steps.

2 Solution-based fabrication

On a cellulose paper substrate ($\sim 200\text{-}\mu\text{m}$ thick) with a 150-nm-thick aluminium film deposited by thermal evaporation, a polymer film of ferroelectric P(VDF-TrFE) [i.e., $\text{P}(\text{VDF}_{0.7}\text{--TrFE}_{0.3})$, $\text{VDF}:\text{TrFE} = 7\text{ mol}:\text{3 mol}$] is spin-coated at 3000 rpm for 25 seconds. $\text{P}(\text{VDF}_{0.7}\text{--TrFE}_{0.3})$ of varying wt %, diluted in 2-butanol, is used to control the film thickness. It is noted that the typical thickness of the 4-wt % $\text{P}(\text{VDF}_{0.7}\text{--TrFE}_{0.3})$ film is $\sim 180\text{-nm}$. The spin-coated film on the paper substrate is annealed at 140°C for 1 hour in ambient air for better crystallization. Further, a semiconducting n-type channel material comprised of 0.7-wt % regioregular Poly(3-hexylthiophene) (P3HT) solution dissolved in CHCl_3 is spin-coated at 2500 rpm for 25 seconds ($\sim 130\text{-nm}$ thick), followed by an annealing process at 140°C for 1 hour in ambient air to remove residual solvent. Finally, Au is deposited by thermal evaporation with a shadow mask, to form the source/drain electrodes. The physical gate length/width of the paper transistor is $5\text{-}/100\text{-}\mu\text{m}$. The cross-sectional field-emission scanning electron microscopy (FE-SEM) image of the paper transistor is shown in Fig. 1.

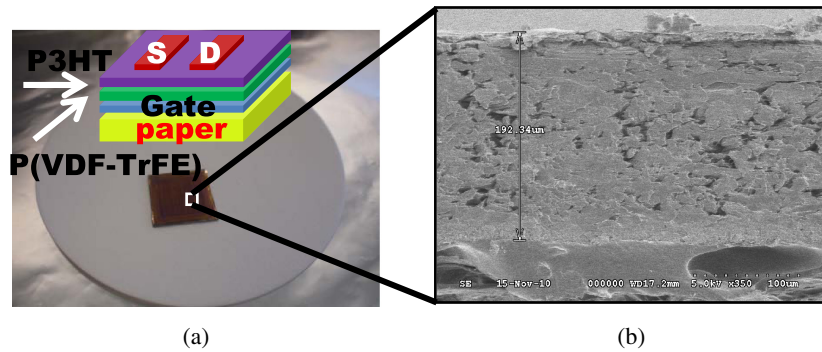


Fig. 1. (a) Chip fabricated on the cellulose paper substrate, with the three-dimensional bird's eye-view of the transistor on the paper, (b) the cross-sectional FE-SEM image

3 Results and discussion

The polarization versus electric-field (P-E) characteristics of the paper transistor without the P3HT channel layer are measured (Fig. (2)) to confirm the basic properties of the ferroelectric material [i.e., P(VDF-TrFE)]. It is observed that the ferroelectricity of the P(VDF_{0.7}-TrFE_{0.3}) triggers a hysteresis loop in the P-E curve. In the P-E characteristics of the capacitor consisting of a Au/P(VDF-TrFE)/Al/paper stack, the remanent polarization (P_r) and coercive field (E_c) are $\sim 8 \mu\text{C}/\text{cm}^2$ and $\sim 0.8 \text{ MV}/\text{cm}$, respectively, at 100 Hz.

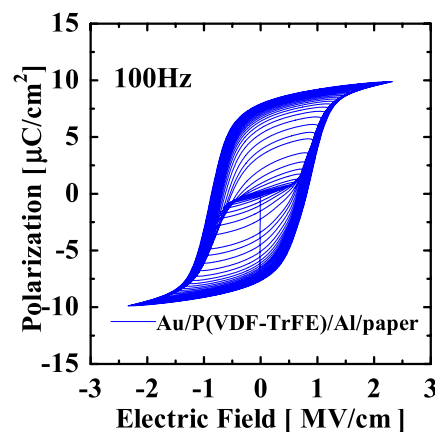


Fig. 2. The polarization versus electric-field (P-E) characteristic of the transistor on paper without the P3HT layer, under the frequency of 100 Hz. Note that the typical remanent polarization and coercive electric field in metal-ferroelectric-metal structure was $\sim 8 \mu\text{C}/\text{cm}^2$ and $\sim 0.8 \text{ MV}/\text{cm}$ at 100 Hz.

As shown in Fig. 3, the remanent polarization decreases with increasing frequency, whereas the coercive electric field increases with increasing frequency. This implies that the polarization reversal speed in the organic P(VDF-TrFE) is lower than that in the typical inorganic ferroelectric materi-

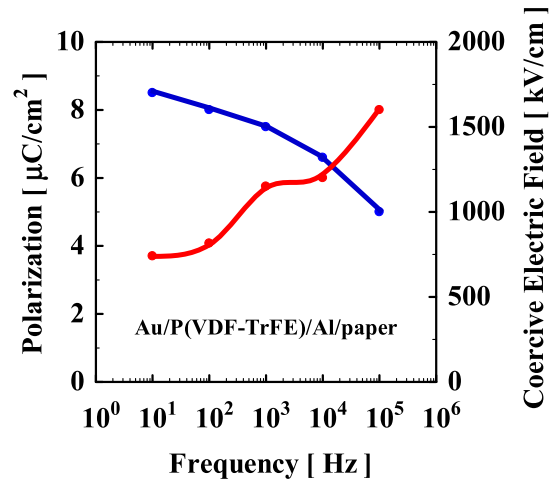


Fig. 3. Remanent polarization and the coercive electric field values as a function of frequency.

al, because of its slow molecular ordering. The basic properties of the ferroelectric material, P(VDF_{0.7}-TrFE_{0.3}), are experimentally verified as above.

Next, FeFETs with a semiconducting 0.7 wt-% P3HT channel are fabricated on a cellulose paper substrate. The current versus voltage characteristic of this device is measured, as shown in Fig. 4(a). Typical thicknesses of the 4-wt % P(VDF_{0.7}-TrFE_{0.3}) film and 0.7-wt % P3HT film are ~180-nm and 130-nm, respectively. The drain current (I_D) of the transistor on paper exhibits a clear hysteresis curve, which indicates that there exists a threshold voltage (V_{TH}) window of ~20 V for nonvolatile memory application. This V_{TH} window is obtained due to the shift of the turn-on voltage of the FeFET by the nature of the ferroelectric material [i.e., P(VDF-TrFE)]. In addition, an on-/off-current ratio of ~ 10^2 is also demonstrated with a gate voltage in the range from -30 V to +30 V. Fig. 4(b) shows the focused Ion Beam Scanning

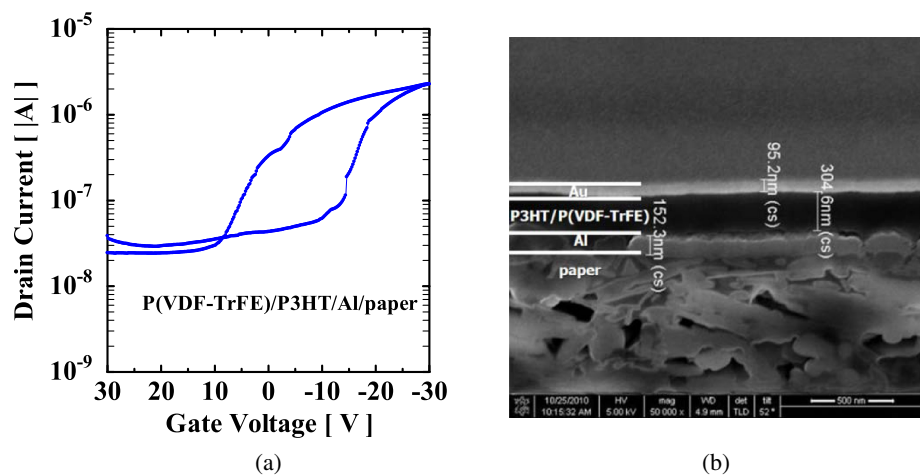


Fig. 4. (a) Typical drain current (I_D) vs. gate voltage (V_G) curve of the bottom-gated FeFET with Au/P3HT/P(VDF-TrFE)/Al/paper structure. (b) Focused Ion Beam Scanning Electron Microscopy (FIB-SEM) image

Electron Microscopy (FIB-SEM) image of the paper transistor. Al, P(VDF_{0.7}-TrFE_{0.3}), P3HT, and Au films are uniformly formed on the paper substrate with good adhesive property between them. This image was taken at 50,000× magnification in the secondary electron imaging mode.

4 Conclusion

A FeFET for nonvolatile memory application has been fabricated on a paper substrate by a low-cost solution-based-only fabrication process for the first time. The basic properties of the P(VDF-TrFE) ferroelectric material have been experimentally verified. The material has been used to demonstrate a wide V_{TH} window of ~ 20 V and an on-/off-current ratio of 10^2 in an organic FeFET on the paper. The V_{TH} window and performance of the device on the paper substrate are quite comparable with those of the device on the conventional silicon substrate. It was also confirmed that the wt-% of the P3HT semiconducting channel material can easily control the on-/off-current level of the transistor on the paper.

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