

# A low power low supply sensitivity current-mode relaxation oscillator

Jun Sun, Yan Han<sup>a)</sup>, and Yuji Qian

*Institute of Microelectronics and Optoelectronics, Zhejiang University,  
Hangzhou 310027, China*

*a) hany@zju.edu.cn*

**Abstract:** This paper presents a design of a 100 kHz 0.54  $\mu$ W fully integrated current-mode relaxation oscillator. The transistors in the sub-threshold region, the current-mode comparator, the current-starving RS flip-flop are used to reduce the power consumption. Meanwhile, the employing of the current-starving RS flip-flop significantly reduces the sensitivity of the frequency to supply voltage fluctuation. The temperature coefficient is 51 ppm/ $^{\circ}$ C from  $-40$  to  $85^{\circ}$ C, and the line regulation is  $-0.40\%/V$  over a supply voltage range from 1.0 to 2.0 V. This oscillator is designed in SMIC 0.18  $\mu$ m CMOS technology and operates at minimum supply voltage of 1.0 V with drawn current of 540 nA at room temperature.

**Keywords:** relaxation oscillator, low power, low supply sensitivity

**Classification:** Integrated circuits

## References

- [1] C. Ying, P. Leroux, W. De Cock and M. Steyaert: IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (2013) 186. DOI:10.1109/ISSCC.2013.6487693
- [2] F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts and B. Nauta: IEEE J. Solid-State Circuits **46** (2011) 1544. DOI:10.1109/JSSC.2011.2143630
- [3] Y. H. Chiang and S. I. Liu: IEEE Trans. Circuits Syst. II, Exp. Briefs **60** (2013) 837. DOI:10.1109/TCSII.2013.2281920
- [4] M. McCorquodale, B. Gupta, W. Armstrong, R. Beaudouin, G. Carichner, P. Chaudhari, N. Fayyaz, N. Gaskin, J. Kuhn, D. Linebarger, E. Marsman, J. O'Day, S. Pernia and D. Senderowicz: IEEE Int. Frequency Control Symp. (2010) 103. DOI:10.1109/FREQ.2010.5556366
- [5] X. J. Xia, X. C. Ji, Y. F. Guo, B. Zhu and L. Wang: IEICE Electron. Express **10** (2013) 5.
- [6] T. Tokairin, K. Nose, K. Takeda, K. Noguchi, T. Maeda, K. Kawai and M. Mizuno: Dig. Symp. VLSI Circuits (2012) 16. DOI:10.1109/VLSIC.2012.6243767
- [7] A. Paidimarri, D. Griffith, A. Wang, A. P. Chandrakasan and G. Burra: IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (2013) 184. DOI:10.1109/ISSCC.2013.6487692
- [8] K. Choe, O. D. Bernal, D. Nuttman and M. Je: IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (2009) 402. DOI:10.1109/ISSCC.2009.4977478
- [9] Y. C. Ni and M. Onabajo: Analog Integr. Circuits Signal Process. **79** (2014) 309. DOI:10.1007/s10470-014-0261-9

- [10] K. Ueno, T. Hirose, T. Asai and Y. Amemiya: IEEE J. Solid-State Circuits **44** (2009) 2047. DOI:10.1109/JSSC.2009.2021922

## 1 Introduction

Recently, there has been an increasing demand for SoCs in small-size, low-power and low-cost applications, such as battery-operated biomedical devices [1] and wireless sensor networks [2]. As an important component, on-chip oscillators are widely employed in those SoCs for timing reference. For a portable device, the volume and battery life are two of the critical issues [3]. For most batteries, the output voltage will drop over the operating time, a low-power on-chip oscillator with low supply sensitivity can not only extend the battery life but also reduce the circuitry volume.

Much work has been involved in the researches of fully integrated oscillator. LC oscillators [4] provide good frequency stability but consume a large power, which are not suitable for low power low frequency applications. Ring oscillators [5] are considerably accurate, but consume several hundred microwatts. Relaxation oscillators [3, 6, 7, 8, 9] can achieve good temperature performance while operate at lower power, which is extremely suitable for low power applications.

In this paper, a current-mode relaxation oscillator is presented with a sub-threshold current reference, two current-mode comparators and a current-starving RS flip-flop. The designed oscillator is focused on reducing the power dissipation while providing a wide supply voltage range and sufficient accuracy. The proposed oscillator is capable of operating over a wide supply voltage range with low sensitivity to supply voltage and doesn't need any external components.

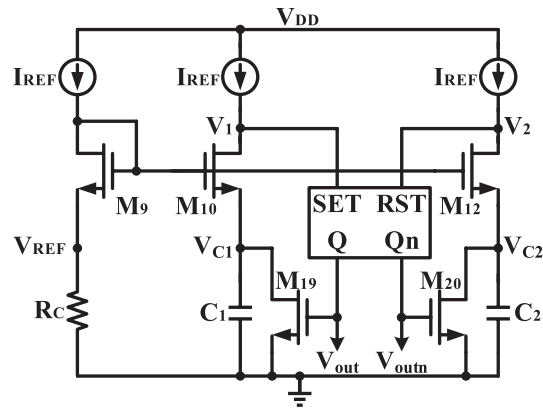
This paper is organized as follows. Section II presents the design and analysis of the proposed oscillator. Section III shows the simulation results and performance comparison with the art-of-state and Section IV concludes the paper.

## 2 Oscillator architecture

### 2.1 Overview of the approach

The proposed current-mode relaxation oscillator is shown in Fig. 1. The reference current  $I_{REF}$  passes through the resistor  $R_C$  and generates a reference voltage  $V_{REF}$ . The reference current  $I_{REF}$  charges metal-insulator-metal (MIM) capacitor  $C_1$  ( $C_2$ ) and when  $V_{C1}$  ( $V_{C2}$ ) exceeds  $V_{REF}$ ,  $M_{10}$  ( $M_{12}$ ) turns off, then the drain voltage of  $M_{10}$  ( $M_{12}$ ) goes high. The two capacitors  $C_1$  and  $C_2$  are alternately charged to  $V_{REF}$  by  $I_{REF}$  and discharged to ground depending on the state of RS flip-flop. To understand how this circuit operates, assume initially  $Q$  is low and its complement  $Q_n$  is high. The NMOS switch  $M_{20}$  is on,  $C_2$  is discharged to ground via  $M_{20}$ , and  $C_1$  is connected to the current source  $I_{REF}$ . Assume the voltage of  $C_1$  is initially zero, the process can be described as follows:

- 1)  $C_1$  continues to be charged by  $I_{REF}$  until its voltage  $V_{C1}$  exceeds  $V_{REF}$ .
- 2) When  $V_{C1}$  exceeds  $V_{REF}$ ,  $V_1$  goes high setting the RS flip-flop, reversing the state of  $Q$  and  $Q_n$ . Now  $C_2$  is charged by its charging current reference  $I_{REF}$ , and  $C_1$  is rapidly discharged to ground through  $M_{19}$ .



**Fig. 1.** System diagram of the proposed oscillator.

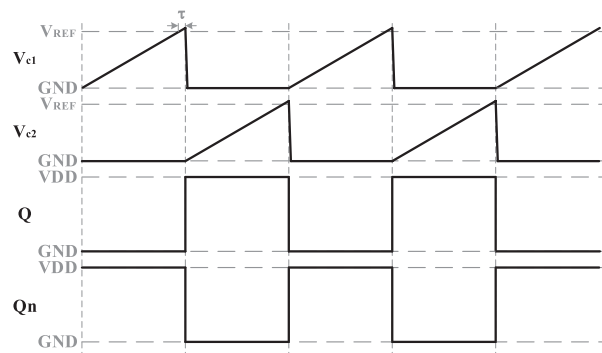
3)  $C_2$  continues to be charged until its voltage  $V_{C2}$  exceeds  $V_{REF}$ . When this happens, the state of the RS flip-flop changes again and a whole oscillation period is completed.

The simplified timing diagram of this process is shown in Fig. 2. Considering the delay of current-mode comparator and the RS flip-flop, the oscillation period of the relaxation oscillation can be given as

$$T = 2 * \left( \frac{V_{REF}C}{I_{REF}} + \tau \right) \quad (1)$$

where  $\tau$  is the delay of the comparator and RS flip-flop, for a typical 50% ratio output clock, here  $C_1$  and  $C_2$  is set to  $C_1 = C_2 = C$ . Because  $V_{REF} = I_{REF} * R_C$ , Eq. (1) can be rewritten as

$$T = 2 * (R_C C + \tau) \quad (2)$$



**Fig. 2.** Simplified timing diagram showing the operation of oscillator.

## 2.2 Oscillator

The detailed circuit of the proposed relaxation oscillator is shown in Fig. 3. A PTAT current reference generator is used as the bias circuit. When  $V_{DS}$  is more than 100 mV, the drain current  $I_D$  of an NMOS working in the sub-threshold region can be approximated as [10]

$$I_D = \mu(\zeta - 1)C_{OX} \frac{W}{L} V_T^2 \left( \exp \frac{V_{GS} - V_{TH}}{\zeta V_T} \right) \quad (3)$$

where  $\mu$  is the electron mobility,  $\zeta$  is the sub-threshold slope factor,  $C_{OX}$  is the gate-oxide capacitance,  $V_T$  is the thermal voltage, and  $V_{TH}$  is the threshold voltage.

In Fig. 3, both of  $M_5$  and  $M_6$  operate in the sub-threshold region. The PTAT current  $I_P$  can be derived as

$$I_P = \frac{V_{GS5} - V_{GS6}}{R} = \zeta \frac{V_T}{R} \ln\left(\frac{W_6/L_6}{W_5/L_5}\right) \quad (4)$$

Eq. (2) shows that the oscillation frequency is related to the reference voltage generating resistor  $R_C$ , the charging storing capacitor  $C$  and the delay  $\tau$  induced by the comparator and the RS flip-flop. In this paper, the delay  $\tau$  is designed to be much smaller than the oscillation period. Meanwhile, the temperature variation of the MIM capacitor can be negligible, so the temperature stability is dominant by the resistor  $R_C$ . Small temperature coefficient is achieved by cancelling the temperature dependence of the capacitance and the delay  $\tau$  using a diffused resistor  $R_P$  and a polysilicon resistor  $R_N$  with an opposite temperature coefficient.

According to the operation of the oscillator, when  $V_{C1}$  or  $V_{C2}$  is varying slowly from 0 to  $V_{REF}$ , the input voltage of RS flip-flop  $V_1$  or  $V_2$  is varying from 0 to the threshold voltage, thus a conventional RS flip-flop composed of NAND gates or NOR gates will consume a large short-circuit power. A current-starving RS flip-flop is used instead in this paper to solve this problem. Meanwhile, since the currents in  $M_{13}$  and  $M_{14}$  are copied from the current in  $M_3$  ( $M_4$ ) which is a supply-insensitive current reference, the input voltage to convert the state of the RS flip-flop will not change with the supply voltage, this makes the oscillation frequency less sensitive to the supply voltage.

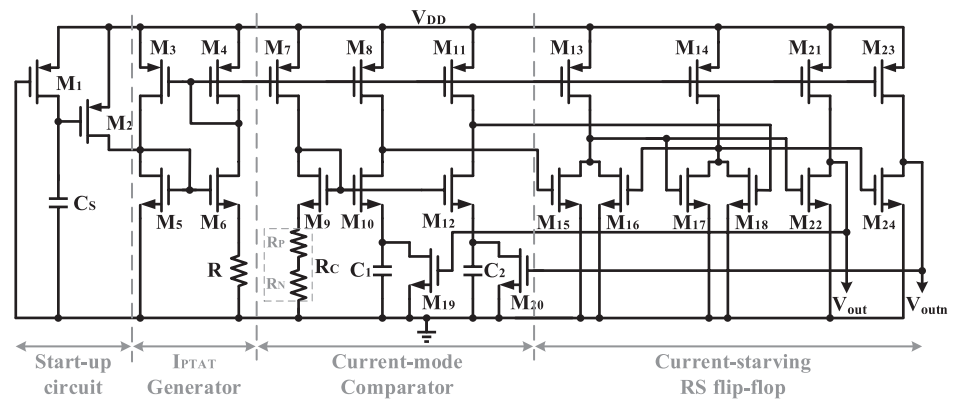


Fig. 3. Schematic of the proposed oscillator.

### 2.3 Sensitivity to supply fluctuation

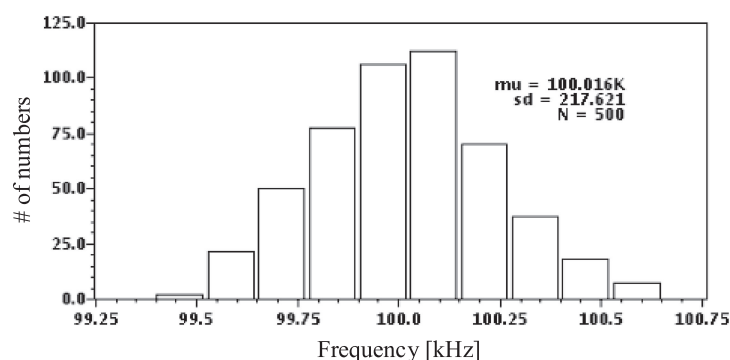
Several mechanisms affect the supply sensitivity. First, due to the channel length modulation effect, the current reference is positively correlated with the supply voltage, thus when the supply voltage increases, the delay of the current-mode comparator will decrease. Second, for a slow-varying input signal, the delay of the current-starving RS flip-flop is inversely proportional to supply voltage. Lastly,  $C_1$  ( $C_2$ ) is discharged to a value  $V_L$  which is not zero due to the finite on resistance of  $M_{19}$  ( $M_{20}$ ). The on resistance is supply dependent, a higher supply voltage will lead to a smaller  $V_L$ , which means a smaller oscillation frequency. However, this will

not be a serious problem since the smallest channel length can be used for  $M_{19}$  ( $M_{20}$ ), a relatively large  $W/L$  will not introduce large delay. Over all, due to the existence of the opposite effects to the oscillation frequency, a small supply sensitivity is achieved.

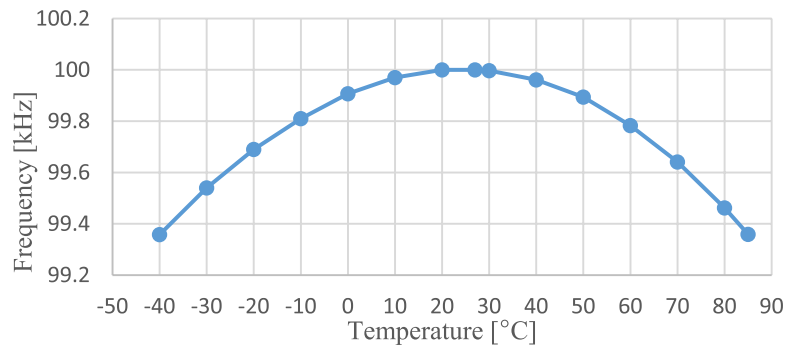
In [3], a low-power current-mode relaxation oscillator has also been proposed, since the delay is inversely proportional to supply voltage, the output frequency shows a positive variation when supply voltage increases. Moreover, the duty cycle of the oscillator signal is not 50%, an additional clock divider is needed to generate a proper 50% duty cycle signal. On the other hand, for our oscillator, the duty cycle can be designed to nearly any desired value simply by setting the ratio of  $C_1$  and  $C_2$  which provides more flexibility.

### 3 Simulation results and performance summary

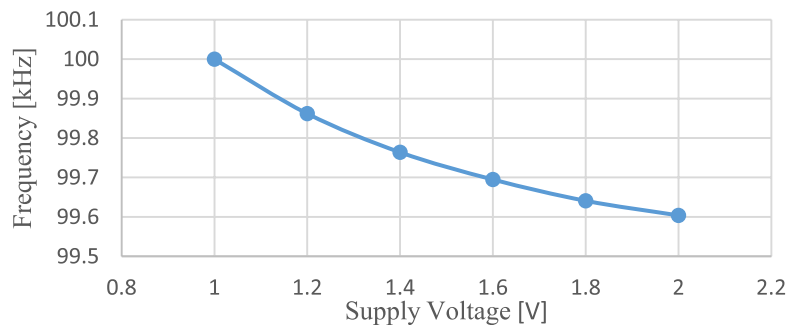
The proposed relaxation oscillator has been implemented in SMIC 0.18  $\mu\text{m}$  CMOS process. Monte Carlo simulation result of the relaxation oscillator is presented in Fig. 4. Since the statistical models of the resistors and MIM capacitor are not given in the simulation models, only the process variation of the MOSFETS is considered in this simulation. The simulation result shows a mean value of the output frequency of 100.0 kHz and a standard deviation (sd) of 217.6 Hz. Fig. 5 shows the oscillation frequency variation as function of temperature for a supply voltage of 1.0 V. From the results we can derive that the proposed oscillator has a temperature coefficient of about 51 ppm/ $^{\circ}\text{C}$  over a temperature range from  $-40$  to  $85^{\circ}\text{C}$  at a 1.0 V supply. Fig. 6 shows the simulated output frequency as function of supply voltage at room temperature, when the supply voltage varies from 1.0 to 2.0 V, the oscillation frequency varies from 100 kHz to 99.60 kHz, leading to a line sensitivity of  $-0.40\%/V$ . The oscillator consumes 540 nA from a 1.0-V supply at room temperature, tt corner. Performance comparison with the art-of-state is summarized in Table I. Compared to the current-mode relaxation oscillator in [3], thanks to the employing of the current-starving RS flip-flop, our oscillator achieves a much lower sensitivity to supply fluctuation. Although the oscillator in [6] consumes a lower power, the supply voltage sensitivity is extremely high. Overall, our oscillator exhibits a competitive performance in power consumption and supply voltage sensitivity.



**Fig. 4.** Histogram of the oscillation frequency for 500 Monte Carlo runs.



**Fig. 5.** Simulated output frequency variation as function of temperature.



**Fig. 6.** Simulated output frequency variation as function of supply voltage.

**Table I.** Performance summary.

Ref.	[3] TCSII'13	[5] ELEX'13	[6] VLSI'12	[8] ISSCC'09	[9]* AICSP'14	<b>This Work*</b>
Process	0.18 $\mu\text{m}$	0.5 $\mu\text{m}$	90 nm	0.13 $\mu\text{m}$	0.11 $\mu\text{m}$	<b>0.18 <math>\mu\text{m}</math></b>
Frequency [kHz]	1100	1200	100	3200	20	<b>100</b>
Supply V [V]	1.8	4	0.8	1.5	1.2	<b>1.0</b>
Power [ $\mu\text{W}$ ]	0.859	180	0.28	38.4	4.9	<b>0.54</b>
Variation with Temp. [%]	$\pm 0.32$ @ -20~80°C	$\pm 1.75$ @ -20~100°C	$\pm 0.68$ @ -40~90°C	$\pm 0.25$ @ 20~60°C	$\pm 1.57$ @ -20~80°C	<b><math>\pm 0.32</math> @ -40~85°C</b>
Variation with $V_{\text{DD}}$ [%/V]	3 @ 1.2~2.4 V	N/A	9.37 @ 0.725~0.9 V	4 @ 1.4~1.6 V	N/A	<b>-0.40 @ 1.0~2.0 V</b>

\*Simulation results.

#### 4 Conclusion

A new fully integrated relaxation oscillator is presented that combines extremely low power with low supply voltage sensitivity. The new structure of the current-mode oscillator provides more flexibility in the design of the duty cycle. Meanwhile, the application of the current-starving RS flip-flop significantly reduces the supply voltage sensitivity of the oscillator. Simulation results show that its frequency inaccuracy, due to temperature and supply voltage variations, respectively, is 0.64% from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  and 0.40% with a supply voltage variation of 1.0 V. The proposed oscillator is capable of operating with a minimum supply of 1.0 V while consuming only 540 nA. The performance comparison with recent works confirms that our work provides advantages in power consumption and sensitivity with supply voltage and temperature.