

Electrical characteristics of novel SCR - based ESD protection for power clamp

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Abstract: In this paper, we proposed a new structural protective device based on a silicon controlled rectifier (SCR) to protect ESD (Electrostatic Discharge) of an integrated circuit. The proposed device features latch-up immunity in a normal operation state by the low holding voltage of the existing SCR - based PSD protective device. The proposed device was analyzed to figure out electrical characteristics and tolerance robustness in terms of individual design variables (D1, D2, D3). As a result of the measurement, we were able to increase the holding voltage from 15.75 V to 19.35 V to the maximum depending on the length adjustment of design variables and checked the high robustness of the secondary breakdown current more than 4.6 A with tolerance robustness. The proposed ESD protective device was made using 0.18 μm Bipolar-CMOS-DMOS processing.

Keywords: ESD, Electrostatic Discharge, trigger voltage, holding voltage, SCR

Classification: Electron devices, circuits, and systems

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1 Introduction

The development of semi-conductor processing brought the increase of circuit speed in miniaturization and high-integration of integrated circuits. However, the malfunction and breakdown of circuits is being gradually acknowledged as a serious problem. The damage caused by ESD/EOS accounts for more than 70% of the destruction of the entire semiconductor integrated circuits [1]. For this reason, ESD is one of the most important items in terms of integrated circuits in safety issues and reliability issues [2]. The general device to solve general devices includes GGNMOS (Gate Grounded NMOS) and SCR (Silicon Controlled Rectifier). GGNMOS is easy to design and is perfectly compatible with CMOS processing. However, the current density is high at the surface, and vulnerable to degradation around oxide films. Thus, the amount of current area of ESD current discharge is few mA/ μm , which is so low compared to the area that it is not appropriate to the power clamp phase requiring high robustness [3]. On the contrary, SCR forms a current path inside silicon substrate, so it has high robustness suitable for power clamp phase. However, SCR has trigger voltage more than 20 V by avalanche breakdown voltage between n-well/p-well and holding voltage less than 2 V as NPN/PNP bipolar turn-on voltage [4]. When latch-up occurs by such low holding voltage, the operation of the inner circuit stops and the high current may cause the breakdown of integrated circuits.

In this paper, we proposed SCR – based ESD protection circuits with high holding voltage to prevent unexpected protection circuits by overshoot voltage and noises in normal operation area of inner circuits, and verified electrical characteristics and robustness of protective devices of ESD manufactured based on 0.18 μm BCD processing.

2 Advanced SCR based ESD protection circuit

Figure 1 shows the cross section of the proposed SCR – based ESD protective device. In the proposed device, the existing SCR structure was transformed and the floating n+ expansion area inserted in n-well area was added. Then, p+ cathode (p-drift) was expanded into the p-well area and the base width of the NPN/PNP bi-pole parasitically generated in SCR was expanded to reduce the current gain (Beta) and thus raise holding voltage. In addition, a resistant role on a discharge path was designed by covering the cathode phase with n-well and inserting a well-resistor, and the emitter injection efficiency of the parasitic NPN bipolar was reduced to raise the holding voltage.

The operation principle of the proposed device is as follows: When ESD phenomenon occurs from the Anode phase, the junction of the n-well and the p-well is a reverse direction bias. At this moment, avalanche breakdown occurs due to high electric field between the two junctions. And EHP (Electron-Hole Pair) is generated by avalanche breakdown, when hall current flows to p-drift junction through parasitic PNP bipolar Q2, and the p-well electric potential increases. The emitter-base junction of parasitic NPN bipolar Q3 becomes forward-bias due the raised electric potential of the p-well,

and NPN bipolar Q3 turns on. When Q3 turns on, Q3 current causes a voltage drop in R_{n1} , and PNP bipolar Q1 also turns on. Q1 current also results in a voltage drop at R_p , which helps Q3 turn on. In this process there is no need to supply bias to Q3 any longer due to Q3 current. The holding voltage of the ESD protective device relies on the space charge neutralization in the base area between NPN and PNP due to the carrier inflowing from the NPN/PNP bipolar emitter area. Thus, the bipolar base width and the p-drift area width are very important. To analyze holding voltage properties associated with this, design variables D1, D2, D3 have been set. Individual design variables include floating n+ area (D1) associated with PNP/NPN bipolar base width, p-drift junction (D2) length, n-well distance in floating n+ area, and p-well length (D3) in p-drift area.

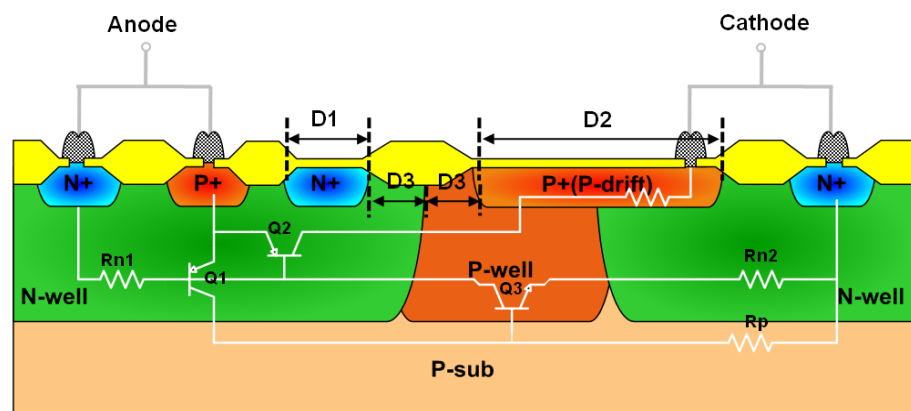


Fig. 1. Section of the proposed SCR-based ESD protection devices

3 Experimental results

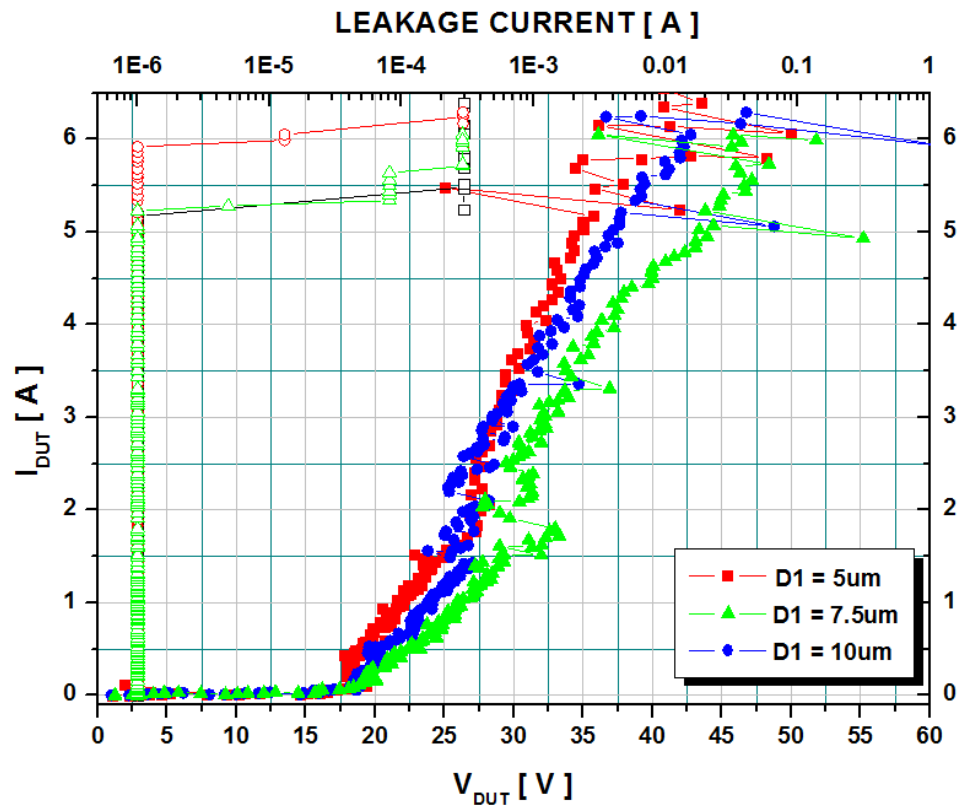
3.1 TLP and leakage measurements

A TLP (Transmission Line Pulse) measuring method, where we can obtain a rectangular current pulse with 10 ns-rising time and 100 ns-pulse width, is widely used to analyze electrical characteristics and robustness of ESD protective devices [5]. The proposed device was manufactured through 0.18 μm BCD processing, and the width was designed in 75 μm .

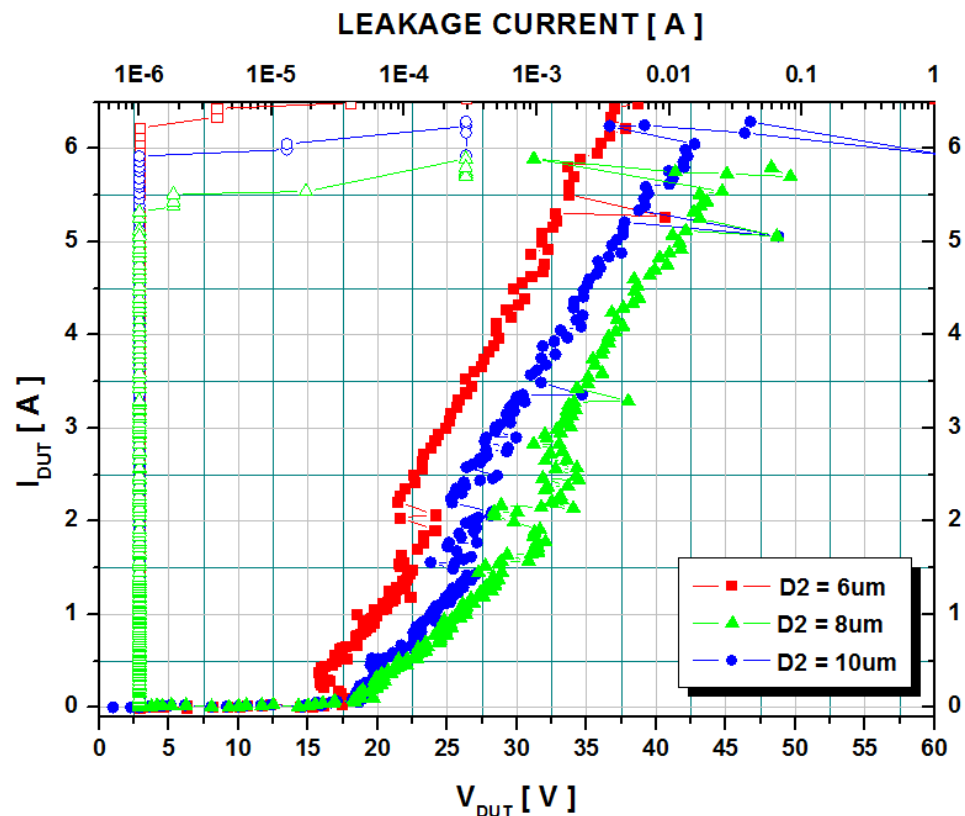
Figure 2 shows a curve of TLP I-V characteristics by design variable of the manufactured, proposed device. The graph in Figure 2 (a) indicates length changes in the graph design variable D1: 5 μm , 7.5 μm , 10 μm . The more the design variable D1 increases, the less the trigger voltage changes; however, holding voltages increased up to 17 V, 18 V, and 19 V, respectively, as current gains decreases with the increases in the PNP bipolar base width. Figure 2 (b) shows a graph when the design variable D2 changes in length: 5 μm , 7.5 μm , 10 μm . As the design variable D2 gradually increases, the holding voltage increases from 15 V to 18 V with the decrease in current gain. On the contrary, the second destruction current gradually decreases up to 6.2 A,

5.9 A, 5.3 A. It is because the entire resistance of SCR increased to raise the holding voltage, so the current driving capability decreases.

Figure 2(c) is a graph showing length changes in design variable D3:



(a)



(b)

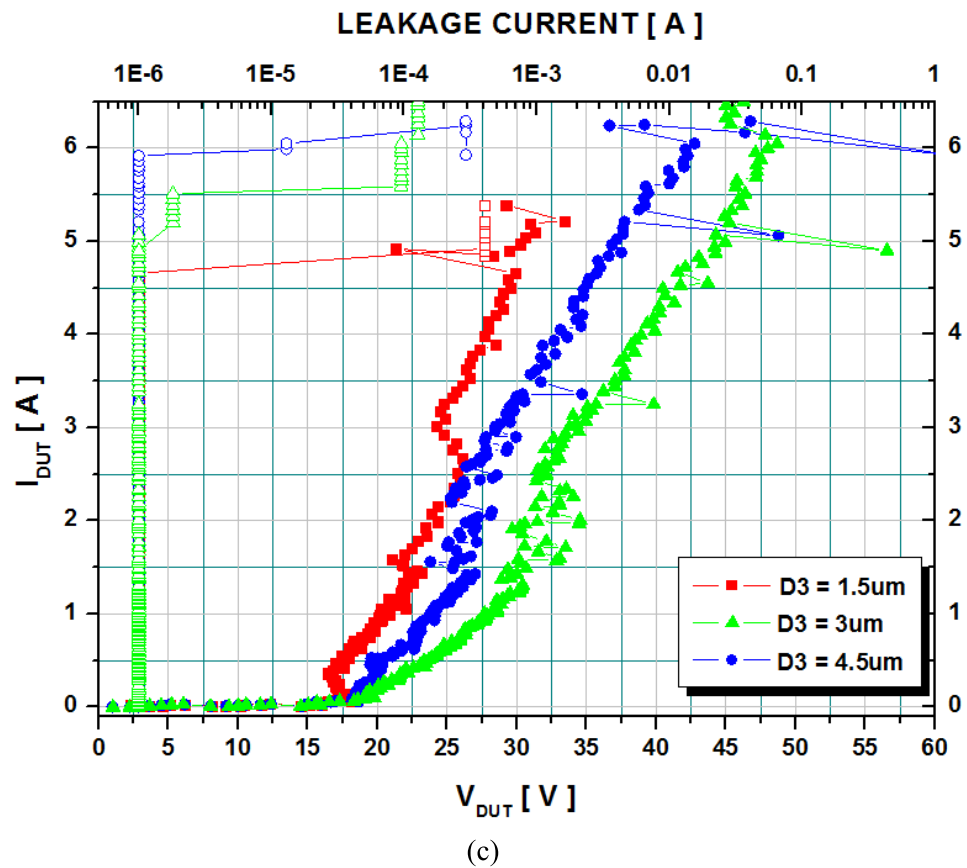


Fig. 2. The proposed device (a) D1 changes, (b) D2 changes, (c) TLP I-V characteristics curve according to D3 changes

Table I. Various electrical characteristics by each design variable of the proposed ESD protection device

| | Design parameter | | Electrical char | | |
|----|------------------|---------|-----------------|-----------|--------------|
| | Width [um] | D1 [um] | V_T [V] | V_H [V] | I_{t2} [A] |
| D1 | 75 | 5 | 19.38 | 17.8 | 5.17 |
| | 75 | 7.5 | 18.95 | 18.48 | 5.92 |
| | 75 | 10 | 20.1 | 19.35 | 5.23 |
| D2 | 75 | 6 | 18.77 | 15.75 | 6.22 |
| | 75 | 8 | 18.95 | 18.48 | 5.92 |
| | 75 | 10 | 19.67 | 18.67 | 5.32 |
| D3 | 75 | 1.5 | 18.36 | 16.47 | 4.66 |
| | 75 | 3 | 18.95 | 18.48 | 5.92 |
| | 75 | 4.5 | 19.25 | 19.25 | 5.07 |

1.5 μm , 3 μm , 4.5 μm . As the design variable D3 gradually increases, the holding voltage increases from 16 V to 19 V with the increase in NPN/PNP bipolar base width and in emitter resistance. Trigger voltage according to

each design parameter, holding voltage, and measurement results for the second breakdown current were attached to Table I.

4 Conclusion

In this paper, we improved latch-up problems by devising an excellent current driving capability - providing SCR-based ESD protective device in the power clamp requiring high robustness and raising the low holding voltage which is a problem with the existing SCR. The proposed ESD protective device was manufactured using 0.18 μm BCD processing. The holding voltage of the proposed protective device has higher holding voltage from 15.75 V to 19.35 V, compared with the existing SCR, depending on design variables. In addition, the devices with basic design variables of the proposed device have the very high robustness of 5.9 A of the second breakdown current, and all of the rest devices depending on design variables have the very high robustness more than 4.6 A of the second breakdown current. Thus, the proposed ESD protective device has latch-up immunity characteristics due to the high holding voltage, and the high robustness is expected to improve reliability of integrated circuits more.

Acknowledgments

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