ELectronics EXpress

IEICE Electronics Express, Vol.3, No.10, 216–220

A 10.0 Gb/s all-active LVDS receiver in 0.18 μm CMOS technology

Panduka Wijetunga[a)]

Rockwell Scientific

5212 Verdugo Way, Camarillo, CA 93012

a) *pwijetunga@yahoo.com*

Abstract: Results for a 10.0 Gb/s all-active LVDS receiver, designed using active bandwidth improvement strategies, are presented. The generalized model generated for the active peak load shows that the transfer characteristic of the load is similar to that of inductive shunt peaking, and can achieve bandwidth improvements comparable to that of on-chip inductive shunt peaking without the associated area penalty. The measured 3 dB bandwidth of the transceiver is 6.0 GHz, and the input sensitivity (BER $< 10^{-13}$) at 10.0 Gb/s and 11.0 Gb/s are 80 mVpp and 100 mVpp respectively. The total transceiver power consumption, including the 50 Ω source terminated output driver, is 60 mW.

Keywords: active-peaking, LVDS, receiver, amplifier, high-speed integrated circuit, transceiver, CMOS integrated circuit

Classification: Integrated circuits

References

[1] "IEEE standard for low-voltage differential signal (LVDS) for scalable coherent interfaces," *IEEE Std. 1596.3–1996*, 31 July 1996.

[2] Electrical characteristics of balanced voltage digital interface circuits, (ANSI/TIA/EIA-422-B-94) (R200) 01, May 1994.

[3] B. Razavi, "Design of monolithic phase-locked loops and clock recovery circuits — a tutorial," *Monolithic phase-locked loops and clock recovery circuits*, pp.i–ix, IEEE Press, New York, 1996.

[4] B. Madhavan, "Multi-Gigabits/s/channel parallel optical data link design in CMOS technology," Doctoral thesis, University of Southern California, Los Angeles, Aug. 2000.

[5] T. H. Lee, *Design of CMOS radio frequency integrated circuits*, Cambridge University Press, Cambridge, 1998.

[6] P. Wijetunga, "High performance crossbar switch design," *Doctoral thesis*, University of Southern California, Los Angeles, May 2006.

1 Introduction

Low voltage differential signaling (LVDS) is widely accepted in high-data rate parallel interface as an alternative to slower, more power hungry differential

DOI: 10.1587/elex.3.216
Received April 01, 2006
Accepted April 20, 2006
Published May 25, 2006

signaling schemes such as TIA-EIA-422 [1, 2]. With increasing backplane bandwidth demands, there is considerable interest in improving the data rate of CMOS LVDS receivers to multi-GHz range. Most mutli-GHz LVDS receivers include a differential analog front-end followed by limiting amplifier backend with active or passive bandwidth peaking.

Compared to RF designs that require high quality factor Q, in LVDS receivers Q is only a secondary concern. Instead, receiver gain and bandwidth improvement are of higher significance. Designs with large number of periphery LVDS receivers, reducing receiver area are a primary consideration. As a result, for LVDS receivers active peaking strategies are considered as an attractive alternative to passive inductive peaking. This paper presents the initial experimental results for a LVDS receiver designed using a simple active peaking strategy. The simulation and test results indicate that the simple level-shifted diode-connected load can be used to design multi-GHz low-power broadband digital receiver front-ends.

2 Differential amplifier with active peaking

The simplified schematic of the differential amplifier including the active loads is given in Fig. 1. The small signal equivalent circuit of the level-shifted diode-connected MOS load, including the parasitic is given in Fig. 2.

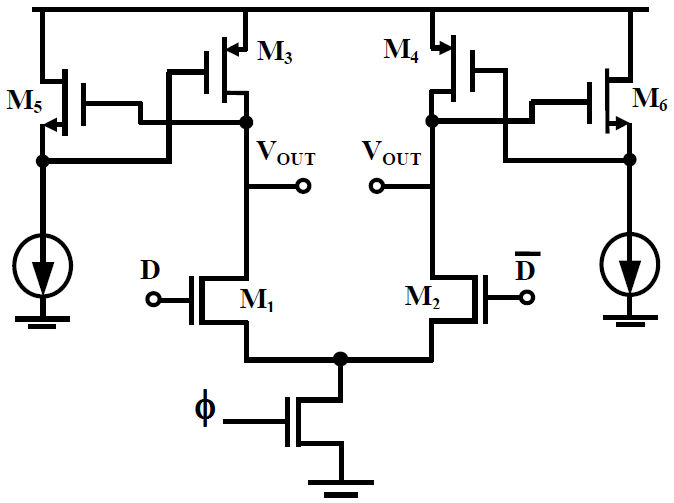


Fig. 1. Simplified schematic of the differential amplifier used in the LVDS receiver.

The level-shifted diode-connected MOS load was first introduced as an alternative to simple a diode-connected load to improve the voltage headroom [3]. In addition to the improved voltage headroom the load also introduces a zero to the transfer function [4].

For most practical designs the normalized output impedance (Z_{OUT} normalized to R_{eff}, normalized to effective impedance) of the active load can be

DOI: 10.1587/elex.3.216
Received April 01, 2006
Accepted April 20, 2006
Published May 25, 2006

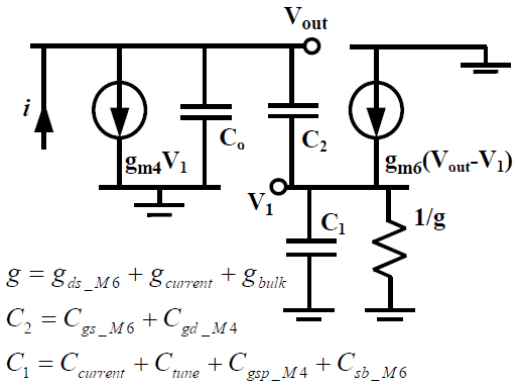


Fig. 2. The small signal equivalent circuit of the active load. C_{tune} is any additional capacitance placed at node 1 for bandwidth tuning purposes. $C_{current}$ and $g_{current}$ are the capacitance and shunt-conductance contributions from the current source.

expressed as [6]:

$$Z_n(s) = \frac{1 + sL_{eff}/R_{eff}}{1 + (1+\beta)R_{eff}C_o s + L_{eff}C_o s^2}. \tag{1}$$

where

$$R_{eff} = \frac{g + g_{m2}}{g_{m1}g_{m2}} = \left(1 + \frac{g}{g_{m2}}\right) \cdot \frac{1}{g_{m1}}. \tag{2}$$

$$L_{eff} = \frac{C_2 + C_1}{g_{m1}g_{m2}}. \tag{3}$$

$$\beta = \frac{g + g_{m1}}{g + g_{m2}} \cdot \frac{C_2}{C_0} > 0_o. \tag{4}$$

Except for the term β Eq. (1) is similar to that of inductive shunt peaking. The variable β models the effect of parasitic coupling between internal node of the load and the output node. Eq. (1) can be used to derive the active peak load maximum bandwidth improvement and maximally flat magnitude (MFM) bandwidth improvement [6]. The impact of β on the maximum achievable bandwidth improvement and MFM bandwidth improvement is given Eq. (5) and Eq. (6) [6].

$$y_C = \sqrt{\left(m + 1 - \frac{m^2(1+\beta)^2}{2}\right) + \sqrt{\left(m + 1 - \frac{m^2(1+\beta)^2}{2}\right)^2 + m^2}}. \tag{5}$$

$$y_C = \frac{1}{\sqrt{2}}\left[1 + \sqrt{1 + \frac{4}{2 + (1+\beta)^2 - 2\sqrt{1 + (1+\beta)^2}}}\right]^{\frac{1}{2}}. \tag{6}$$

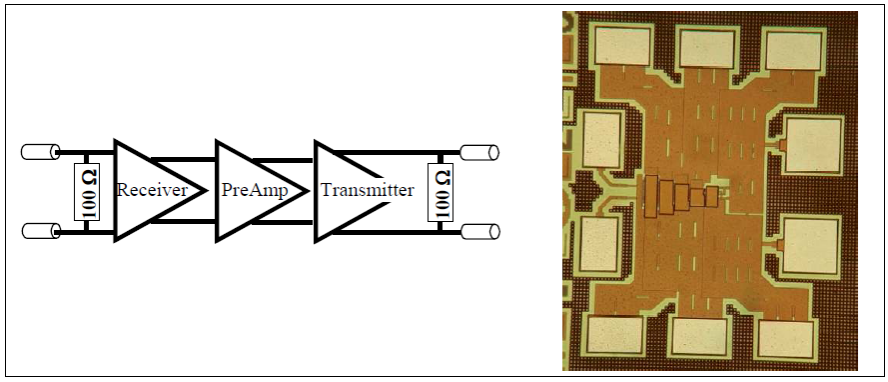
Where y_C is the new bandwidth normalized to the original bandwidth or expected bandwidth improvement and where m is the ratio between the $R_{eff}C_0$ and L_{eff}/R_{eff} time constants. The accuracy of the above analytical

DOI: 10.1587/elex.3.216
Received April 01, 2006
Accepted April 20, 2006
Published May 25, 2006

models is initially verified through spice simulations. The bandwidth improvement projections of the analytical model correspond closely to spice simulations. The error between the model and simulated results is less than 10% for $\beta < 0.3$ [6].

3 Measured results

The active peak load is also used to design the differential front-end and post amplifiers for a 10.0 Gb/s all-active LVDS receiver – transmitter (TxTx) in 0.18 μm CMOS technology. The die micrograph of the test IC is given in Figure 3. The total power consumption of the RxTx including the output driver is 60 mW. The Tx circuit is implemented as a differential current source driver with integrated 50 Ω source termination. The Rx and the post amplifier stages consume a total of 20 mA. The complete Tx circuit consumes 16 mA, of which the Tx pre-amplifier uses 2 mA and the remaining current (14 mA) is supplied to the output.



(a) (b)

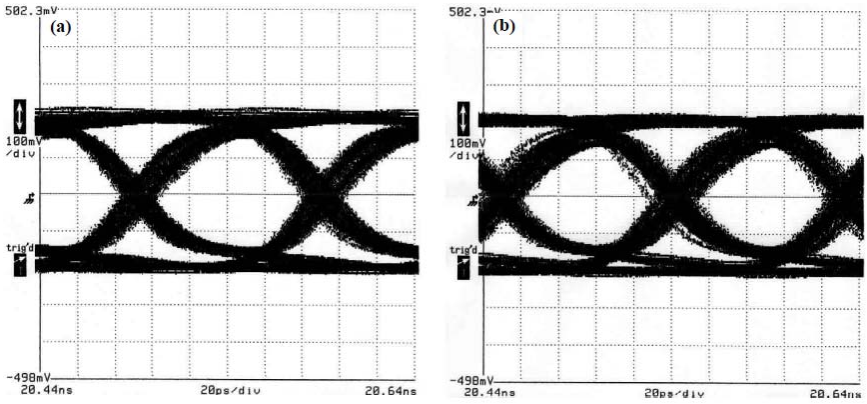
Fig. 3. (a) Block diagram of the LVDS transceiver. (b) Die micrograph of the LVDS transceiver.

The measured 3 dB bandwidth of the transceiver is 6.0 GHz. The high bandwidth results in a complete RxTx input sensitivity is 35 mVpp for a BER = 10^{-9} at 10.0 Gb/s. The BER = 10^{-13} input sensitivity of the RxTx is 80 mVpp and 100 mVpp for 10.0 and 11.0 Gb/s respectively. The 10.0 Gb/s output eye diagram for a 100 mVpp input is given in Fig. 4. The measured 10.0 Gb/s output jitter of the RxTx is better than 4 ps RMS and 24 ps peak-to-peak for inputs higher than 35 mVpp. The 11.0 Gb/s output jitter of the RxTx is better than 4 ps RMS and 27 ps peak-to-peak for inputs higher than 35 mVpp.

4 Conclusion

The effectiveness of active peaking as an alternative to on-chip inductive peaking in multi-GHz LVDS receivers is proven through the design of a 10.0 Gb/s LVDS receiver – transmitter. Receiver bandwidth improvement

DOI: 10.1587/elex.3.216
Received April 01, 2006
Accepted April 20, 2006
Published May 25, 2006



(a) (b)

Fig. 4. The 10.0 Gb/s and 11.0 Gb/s eye diagrams for 100 mVpp $2^{31}-1$ NRZ PRBS LVDS input signal. The output signal amplitude is 370 mVpp across 25 W (50 W source/destination terminated output) (a) 10.0 Gb/s output eye diagram. (b)11.0 Gb/s output eye diagram.

is achieved through the use of an active load. A simple level-shifted diode-connected load is selected as the active peak topology for its simplicity, bandwidth adjustment capability and voltage headroom.

The bandwidth improvements that are comparable to shunt peaking together with the topological simplicity, improved voltage headroom, low-noise and reduced area consumption of the proposed active load makes it ideally suited for dense broadband amplifier arrays. The above attributes also results in excellent process and voltage scaling to smaller geometries.

DOI: 10.1587/elex.3.216
Received April 01, 2006
Accepted April 20, 2006
Published May 25, 2006