IEICE Electronics Express, Vol.8, No.12, 938–943

A 2.4 GHz low phase noise frequency synthesizer for WiMAX applications

Ko-Chi Kuo[a)]

Department of Computer Science and Engineering, National Sun Yat-sen University

No. 70, Lien-Hai Road, Gu-shan District, Kaohsiung 80424, Taiwan

a) *kckuo@cse.nsysu.edu.tw*

Abstract: This paper presents a low phase noise frequency synthesizer for WiMAX applications. The operating frequency of the proposed design ranges from 2.2 GHz to 2.4 GHz with a 1.25 MHz spacing for the 1.25 MHz to 40 MHz channel bandwidth. The proposed VCO suppresses the phase noise effectively by adopting the Q-enhancement technique, the memory reduced tail current, and a noise filter. The high speed frequency divider is implemented by an improved TSPC D-flip-flop. The proposed design is fabricated in a TSMC 0.18 μm CMOS 1P6M process. The measured phase noise is -118 Bc/Hz at an offset of 1 MHz from the center frequency. The fabricated chip consumes 25.5 mW with a 1.5 V supply and occupies a 1.1 mm^2 die area.

Keywords: LC-VCO, frequency synthesizer

Classification: Integrated circuits

References

[1] H. Hedayatic, W. Khalil, and B. Bakkaloglu, "A 1 MHz Bandwidth, 6 GHz 0.18μm CMOS Type-I $\Delta\Sigma$ Fractional-N Synthesizer for WiMAX Applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3244–3252, Dec. 2009.

[2] K. Woo, Y. Liu, E. Nam, and D. Ham, "Fast-lock Hybrid PLL Combining Fractional-N and Integer-N Modes of Differing Bandwidth PLL," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 379–389, Feb. 2008.

[3] A. Bonfanti, D. De Caro, A. D. Grasso, S. Pennisi, C. Samori, and A. G. M. Strollo, "A 2.5-GHz DDFS-PLL With 1.8-MHz Bandwidth in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1403–1413, June 2008.

[4] B. Park, S. Lee, S. Choi, and S. Hung, "A 12-GHz Fully Integrated Cascode CMOS LC VCO With Q-Enhancement Circuit," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 2, pp. 133–135, Feb. 2008.

[5] C. Wu and S. Hsiao, "The design of a 3 V 900 MHz CMOS bandpass amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 159–168, Feb. 1997.

[6] C. C. Boon, M. A. Do, K. S. Yeo, J. G. Ma, and X. L. Zhang, "RF CMOS Low-Phase-Noise LC Oscillator through Memory Reduction Tail Transistor," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 51, no. 2, pp. 85–90, Feb. 2004.

DOI: 10.1587/elex.8.938
Received April 22, 2011
Accepted May 25, 2011
Published June 25, 2011

[7] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.
[8] M. Kozak and I. Kale, "A Pipelined Noise Shaping Coder for Fractional-N Frequency Synthesis," *IEEE Trans. Instrumentation Measurement*, vol. 50, no. 5, pp. 1154–1161, Oct. 2001.

1 Introduction

Due to the high demand of mobile devices such as notebooks, cellular phones, and PDAs, a low cost and high-performance wireless communication device has been the subject of major research in recent years. WiMAX (World Interoperability for Microwave Access) can provide a fixed and portable wireless broadband connectivity without a base station. To provide a fine resolution between adjacent channels, a fractional-N synthesizer is adopted in the proposed design. The channel bandwidth needs to be varied from 1.25 MHz to 20 MHz [1] to accommodate the different WiMAX protocols. The Delta-sigma modulator (DSM) is required to modulate the division ratio in the fractional-N synthesizer. The extra phase noise near the center frequency can be converted by DSM to a higher frequency and can be eliminated by the loop filter with a narrow bandwidth. In this paper, a second-order MASH 1-1 DSM is implemented in the fractional-N synthesizer with the proposed low phase noise Voltage Controlled Oscillator (VCO). Fig. 1 (a) shows the block diagram of the frequency synthesizer.

2 The proposed VCO

Phase noise is one of the most critical performance parameters in the wireless communication devices. Many circuit design techniques have been proposed to improve the phase noise performance [1, 2, 3, 4]. The Q-enhancement circuit [5] was proposed to compensate for the resistive loss in the integrated inductor. The circuit in [4] utilized the cascode circuit to enhance the gain of the VCO core, enhancing the noise performance. However, the output swing is reduced due to the cascode architecture. Hence, the phase noise performance can be degraded, especially when the circuit operates at a lower supply voltage. In addition, two biasing voltages are required to bias the cascode stage. To resolve these issues, the proposed VCO utilizes the Q-enhancement technique without the cascode stage. Therefore, the advantage of the Q-enhancement circuit can be preserved while the output swing can be enlarged. In addition, the two additional biasing voltages can be eliminated.

Fig. 1 (b) shows the proposed VCO design, where C1 and C2 are the varactors. The LC tank is formed by C1, C2 and L1. The cross-coupled NMOS (M5, M6) and PMOS (M3, M4) pairs generate the transconductance to compensate for the loss in the LC tank of the VCO. The Q-enhancement for the LC tank is implemented by capacitors (C5–C12). The output swing of the proposed VCO can be enlarged without using the cascode technique because

DOI: 10.1587/elex.8.938
Received April 22, 2011
Accepted May 25, 2011
Published June 25, 2011

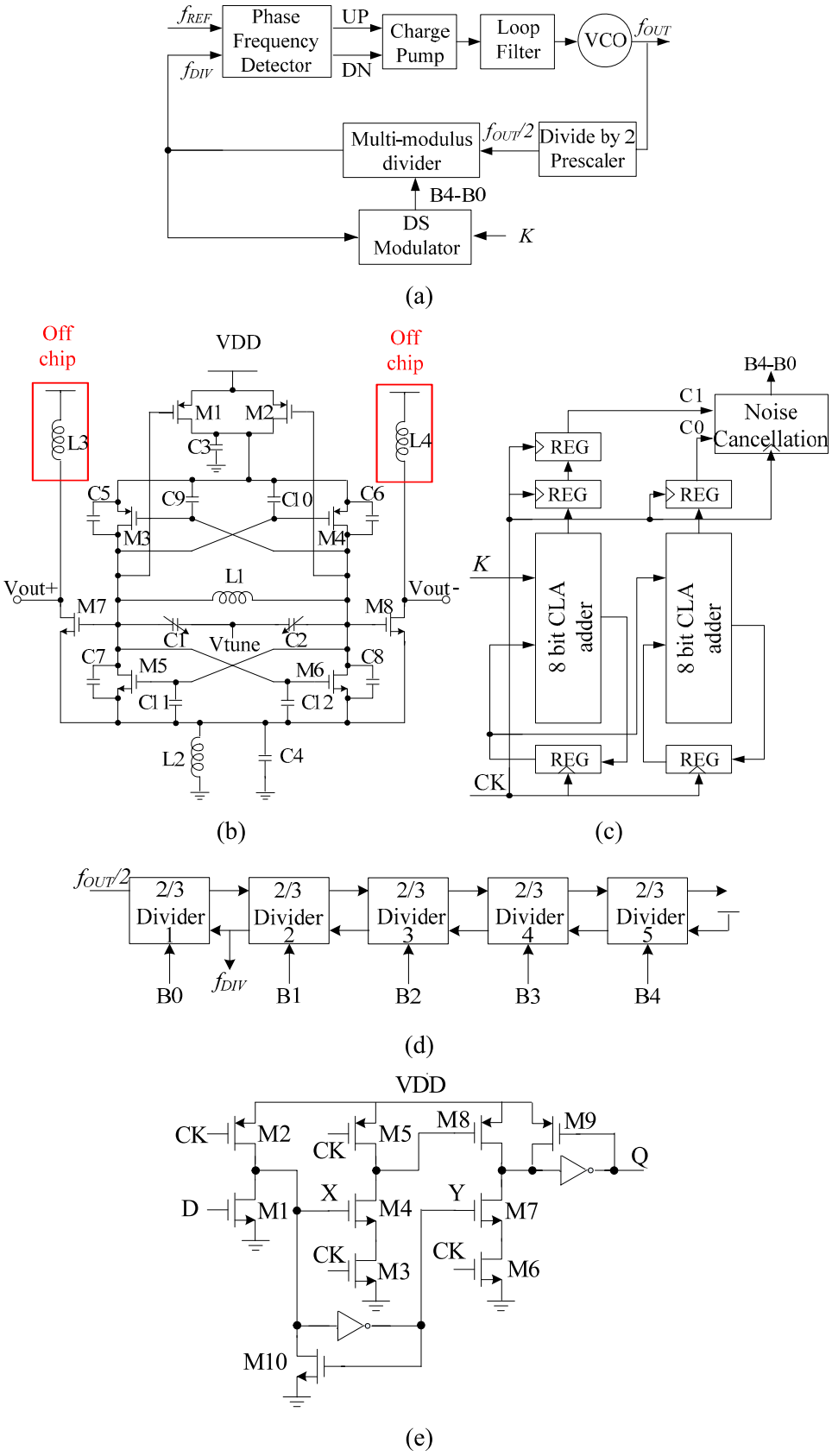


Fig. 1. (a) Multi-modulus fractional-N synthesizer (b) The circuit of the proposed LC VCO (c) The block diagram of the pipeline MASH 1-1 DSM (d) Multi-modulus divider (e) TSPC DFF implemented in the 2/3 divider.

DOI: 10.1587/elex.8.938
Received April 22, 2011
Accepted May 25, 2011
Published June 25, 2011

the cascode stage is removed. However, the Q factor is reduced and the phase noise is degraded. Therefore, both memory reduced tail transistors [6] and noise filter [7] techniques are adopted to enhance phase noise performance. The PMOS (M1, M2) pair is composed of the memory reduction transistors that suppress the flicker noise and lower the current consumption. Instead of applying constant gate-to-source biasing, the PMOS (M1, M2) pair is periodically switched between the ON and OFF states. Because the PMOS (M1, M2) pair does not operate during the OFF state, the overall $1/f$ noise can be reduced. The noise filter formed by C4 and L2 must be inserted at the common source of the differential pair to resonate in parallel with the capacitance when the operation frequency of this node is at $2\,\omega_o$ [7]. It can achieve higher impedance at the tail and reduce the second harmonic of the differential-pair FETs. Transistors M7 and M8 form a simple open-drain output buffer for measurement consideration and L3 and L4 are the off-chips.

3 Delta sigma modulator

The design of a delta-sigma modulator adopts the MASH 1-1 architecture as shown in Fig. 1 (c). The hardware complexity and power consumption can be reduced by implementing the pipeline architecture [8]. An 8-bit carry look-ahead adder (CLA) is used in the pipeline stage to reduce the delay time. A divide-by-2 prescaler is placed after the VCO and the reference frequency is 20 MHz. Hence, the channel resolution can be expressed as:

$$\text{Channel resolution} = \frac{f_{REF}}{2^K} = \frac{20 \times 2}{2^8} = 0.15625 \text{ MHz} \tag{1}$$

where K is the number of bits in the adder. The actual channel bandwidth can be varied from 0.15625 MHz to 40 MHz as indicated by (1). The minimum channel spacing is 1.25 MHz by setting K to 8. Hence, the bandwidths of various WiMAX protocols can be 1.25, 2.5, 5, 10, and 20 MHz by setting K to 8, 16, 32, 64, and 128, respectively. The proposed design can also extend the bandwidth to 40 MHz by setting K to 0.

4 Multi-modulus divider

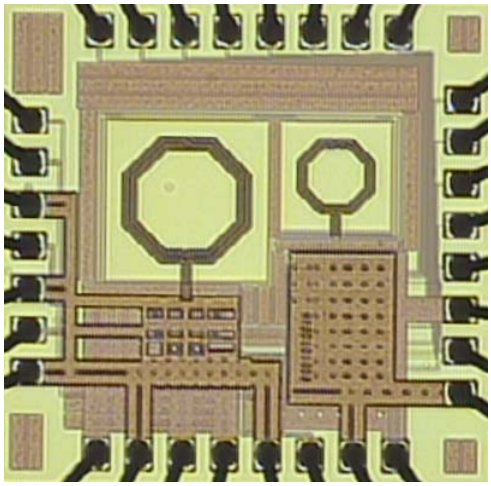
The programmable multi-modulus divider (MMD) is implemented in the frequency divider, as shown in Fig. 1 (d). The MMD can provide a wider frequency division. It is composed of the synchronous divided-by-2/3 dividers. The 5-bit control signals ($B_4B_3B_2B_1B_0$) are generated by the delta-sigma modulator (DSM). The range of the divisor is between 2^m and $2^m - 1$, where m is the number of stages in the divider. Therefore, the division of the divider ranges from 32 to 63. The equation of divisor is shown below.

$$Divisor = 2^5 + 2^4 \cdot B_4 + 2^3 \cdot B_3 + 2^2 \cdot B_2 + 2^1 \cdot B_1 + 2^0 \cdot B_0 \tag{2}$$

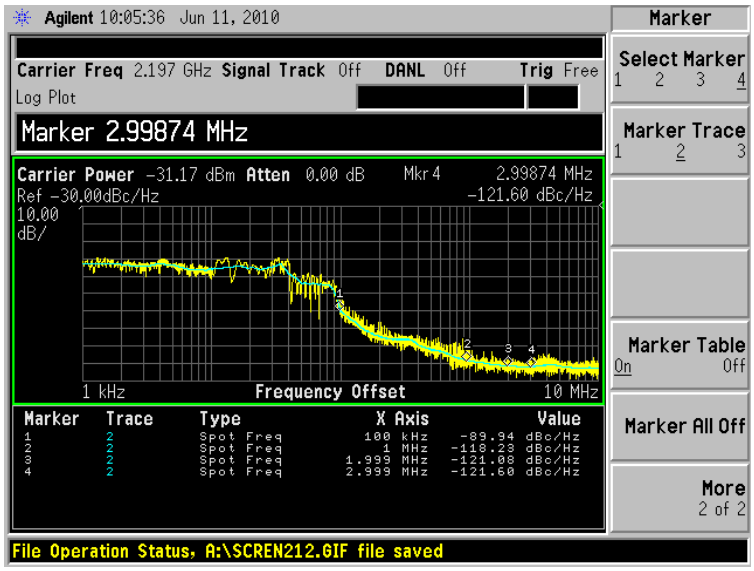
The first stage of the MMD needs to be operated at a higher operating frequency. This can be achieved by reducing the parasitic capacitance in the feedback with a careful layout and transistor sizing. The True-Single-Phase-Clock (TSPC) D-flip-flop (DFF) is implemented in the high-speed divider.

DOI: 10.1587/elex.8.938
Received April 22, 2011
Accepted May 25, 2011
Published June 25, 2011

TSPC dividers are well known for their low power consumption, compared to the current mode logic (CML). The improved TSPC DFF is shown in Fig. 1 (e). The pseudo-NMOS inverter is placed in the first stage of the TSPC DFF to enhance the operating speed. The N-precharged stage is placed in the middle. The pseudo-PMOS inverter in the output stage is replaced with the M6-M8. In this case, the size of M8 can be reduced because M7 is turned off by the inverter controlled by node X before the end of the precharge. M9 and M10 are placed in parallel with two inverters to reduce the charge sharing issue.



(a)



(b)

Fig. 2. (a) Microphotograph of the proposed frequency synthesizer and (b) The measured phase noise.

DOI: 10.1587/elex.8.938
Received April 22, 2011
Accepted May 25, 2011
Published June 25, 2011

5 Measurement results

The proposed design has been fabricated in a TSMC 0.18-μm 1P6M CMOS process and the microphotograph is shown in Fig. 2 (a). The overall design occupies 1.1 mm^2 including the core area and pads. The power dissipation is 25.5 mW with the 1.5 V power supply. The measured operating frequency ranges from 2.2 GHz to 2.4 GHz when the tuning voltage is between 0.6 V and 1.0 V. The measured phase noise is about -118.23 dBc/Hz at a 1 MHz offset frequency at a 2.2 GHz operating frequency as shown in Fig. 2 (b). Table I summarizes the measurement results of the proposed frequency synthesizer and the performance comparison with other recently published works. The proposed VCO design can effectively enhance the phase noise performance with a lower supply voltage. Hence, compared to other works shown in Table I, both low phase noise and low power consumption can be achieved.

6 Conclusion

The design of the low phase noise frequency synthesizer was presented and fabricated in TSMC 0.18-μm 1P6M CMOS process. By adopting a Q-enhancement technique with a memory reduced tail and filtering in the VCO design, the proposed frequency synthesizer can achieve a measured phase noise of -118 Bc/Hz at a 1 MHz offset from the centre frequency. The proposed design can be implemented for various WiMAX protocols with 1.25 MHz spacing for the 1.25 MHz to 40 MHz channel bandwidth.

Table I. Performance comparison of the frequency synthesizer.

Reference	[1]	[2]	[3]	This work
Technology(μm)	0.18	0.18	0.35	0.18
Output Frequency (GHz)	6.12	2.368 – 2.496	2.4 – 2.484	2.2 – 2.4
Reference Frequency(MHz)	38	64/1	74	20
Loop Bandwidth(kHz)	1000	1000	1000	400
Supply (V)	1.8	1.8	3/2	1.5
Phase noise@ 1MHz(dBc/Hz)	−110	−113	−110	−118
Power consumption (mW)	47	29.6	120	25.5
Chip area (mm^2)	3.24	2.08	5.12	1.10
Year	2009	2008	2008	2011

Acknowledgments

This work was supported by the National Science Council (NSC) Taiwan, under grant number NSC99-2220-E-110-009. The authors would like to express their greatest thanks to the National Chip Implementation Center of National Applied Research Laboratories (NARL) Taiwan, for their thoughtful chip fabrication and measurement service.

DOI: 10.1587/elex.8.938
Received April 22, 2011
Accepted May 25, 2011
Published June 25, 2011