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A fast transient response shunt low dropout regulator

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Abstract: In this paper, the proposed shunt regulator is presented. Compared with a series voltage regulator, the shunt voltage regulator gives wideband power supply rejection (PSR) and fast transient response at the expense of large quiescent current. In this paper, a novel shunt regulator architecture is proposed to achieve the genuine characteristic of a shunt regulator with small quiescent current. The proposed shunt regulator transient response is 3.98 μsec over full load current rising step and it is at least 3.5 times faster than series regulator. PSR characteristic of the proposed shunt regulator shows −22.4 dB up to 200 kHz.

Keywords: LDO, series or shunt regulator, transient response, PSR

Classification: Integrated circuits

References

[1] W. Oh, P. Nadimpalli, and D. Kadam, "CMOS Fast-settling Time Low Pass Filter associated with Voltage Reference and Current Limiter for Low Dropout Regulator," *IEICE Electron. Express*, vol. 6, no. 22, pp. 1595–1601, Nov. 2009.

[2] W. Oh, B. Bakkaloglu, C. Wang, and S. K. Hoon, "A CMOS Low Noise Low-Dropout Regulator with Current-Mode Feedback Error Amplifier," *IEEE Trans. Circuits Syst. II*, vol. 55, no. 10, pp. 3006–3015, Nov. 2008.

[3] C. K. Chava and J. Silva-Martinez, "A Frequency Compensation Scheme for LDO Voltage Regulators," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 6. pp. 1041–1050, June 2004.

[4] K. N. Leung and P. K. T. Mok, "A Capacitor-Free CMOS Low-Dropout Regulator with Damping-Factor-Control Frequency Compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

1 Introduction

As the mobile electronics market is growing with unexpected speed, it is not surprising that power management ICs (PMICs) are playing a key role in battery operated mobile electronic products. PMICs contain three major components: linear dropout voltage regulator (LDO), switching mode power

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supply (SMPS) and charge pump circuits. PMICs should provide a constant supply line and, in certain applications, a higher voltage line than the supply line to operate LCD drivers as well. Compared with SMPS and charge pump circuits, LDOs are widely used in PMICs since they provide a clean DC supply line and have simple architectures compared with other power supplies [1, 2]. Many of the latest linear regulator schemes use series voltage regulators. The advantage of series voltage regulators is that they provide high power supply rejection (PSR) and good load and line regulation. The drawback of series voltage regulators is their narrow-band PSR and extremely slow transient response at light load conditions. To improve these drawbacks, the series regulator should consume large current itself, which degrades battery life.

The shunt regulator is an excellent candidate to achieve wideband PSR and a fast transient response. However, the shunt regulator consumes high current at zero load conditions. This paper presents a novel shunt regulator to overcome this problem. Section II first reviews the prior arts in series and shunt regulator architectures and then summarizes the state of the arts. While Section III introduces and details the performance of the proposed shunt regulator, Section IV shows the simulation results of the proposed shunt regulator. Section V draws relevant conclusions.

2 Prior arts in series and shunt regulators

Fig. 1 shows the prior architecture of both series and shunt regulators. A series regulator in Fig 1 (a) is widely used in current power management ICs since it provides high PSR and good load/line regulation, and its architecture is very simple. The main drawbacks of a series regulator are narrow band PSR due to large decoupling capacitor (C_o) and the need for a large compensation capacitor to achieve stability. In addition, the large decoupling capacitor causes slow transient response over a full load current step. To improve these negative aspects, several techniques have been developed, such as inserting a buffer stage between the error amplifier and pass device, or using a wideband low gain multi stage amplifier instead of a single high gain amplifier [3, 4]. These techniques are helpful to improve PSR only, not transient response.

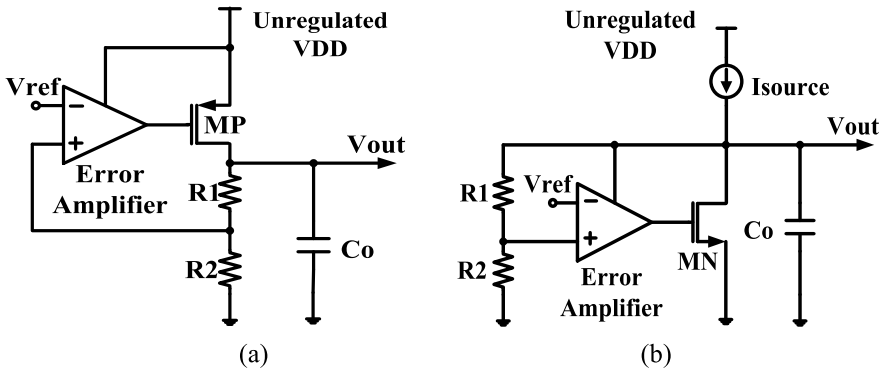

Fig. 1. The prior architecture of (a) series regulator and (b) shunt regulator.

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The shunt regulator in Fig. 1 (b) is a good candidate to achieve wideband PSR and a fast transient response. The architecture of a shunt regulator is similar to a series regulator except that the current source (Isource) provides power to both the amplifier and pass device. The obstacle of a shunt regulator, however, is how to implement this current source and control the current according to loading conditions. Several prior designs have used bipolar transistors, zener diodes, or CMOS diodes to implement the current source. In the standard CMOS process, bipolar transistors and zener diodes are not available so CMOS diodes are utilized. The problem with using a CMOS diode is that it causes large current consumption at no load condition. Since the size of this CMOS diode is determined by the maximum load current condition, the CMOS diode generates maximum current no matter the load condition. Therefore, using CMOS diode causes the device MN required large geometry to handle huge current at no load condition. In addition, the efficiency is degraded due to the voltage drop (closed to 0.7 V) of CMOS diode. Compared to a series regulator, a shunt regulator has wideband PSR and fast transient response characteristics at the expense of large quiescent current since the current source implemented by the pass device always provides large current at any loading condition.

In this paper, the pass device of the proposed shunt regulator is biased using a current sensing feedback circuit to prevent large current consumption at no load conditions. Owing the current sensing feedback circuit, the novel shunt regulator can achieve a significant reduction in current consumption while the regulator keeps providing wideband power supply rejection and a fast transient response. More details will be described in next section.

3 Proposed shunt regulator

The proposed shunt regulator is shown in Fig. 2 (a). The shunt regulator utilizes an adaptively biased pass device using a current sensing feedback circuit. The current source is implemented by PMOS transistor MP. The gate bias of MP is controlled by an adaptive biasing controller which generates V_{cont} by sensing the current in MN1_1. At no load conditions, the current of MP flows into MN1_1 and thus the current in MN1_1 increases. The sensing current induced in the bias controller (MP1, MP2, R_c) also increases which in turn increase V_{cont} and thus decreases the current in MP as compared to the current in MP in full load conditions. At heavy load conditions V_{cont} should be decreased so that MP drives a large current to the output. In this condition, the current through MN1_1 is decreased because most of the current flows into the load and the sensing current also decreases, which generates a low V_{cont} as desired.

There are several important design considerations for the proposed shunt regulator. First, the current I_{s1} is defined by $I_{s1} = I_1 + I_2 + I_3 = I_{s1\_no\_load}$ at no load conditions. At heavy load conditions, the bias controller senses MN1_1 current through mirror devices (MN1_2 and MP1 and MP2) and converts the gate voltage of pass device MP to drive the desired load current,

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I_{s1} which is expressed as $I_{s1} = I_{load} + I_{s1\_no\_load}$.

Second, the stability of system can be achieved very easily using miller compensation between the output of the amplifier and the output of the regulator, since NMOS pass device MN1_1 is very small to prevent large current consumption. In order to analyze the stability, the small signal equivalent model of the proposed shunt regulator is shown in Fig. 2 (b). To analyze the loop response, the loop is broken between the positive input of operational amplifier (V_{fb}) and feedback network resistors (V_{fb_a}). The loop transfer function of the shunt regulator, $LG(s) = V_{fb\_a}(s)/V_{fb}(s)$, is

$$LG(s) = \frac{\begin{array}{c} g_{me}g_{mn2}g_{mp}r_{oe}R_c r_{op}\dfrac{R_2}{R_1+R_2}\left[1+sC_c\left(R_z-\dfrac{1}{g_{mn2}g_{mp}R_c}\right)\right] \\ \times(1+sC_oR_{esr})\left(1-s\dfrac{C_{gdp}}{g_{mp}}\right) \end{array}}{\begin{array}{c} (1+sC_or_{op})(1+sC_cg_{mn2}g_{mp}R_cr_{op}r_{oe})(1+sC_pR_c) \\ \times\left(1+s\dfrac{C_1R_z}{g_{mn1}r_{op}}\right)(1+sC_{gdp}R_{esr})\left(1+s\dfrac{C_2}{g_{mp1}}\right) \end{array}} \quad (1)$$

where g_{me}, g_{mp}, g_{mp1}, g_{mn1}, and g_{mn2} are the transconductance of the error amplifier, MP, MP1, MN1_1 and MN1_2. Each transconductance of MN1_1 and MN1_2 is equal due to current mirror configuration. MP1 and MP2

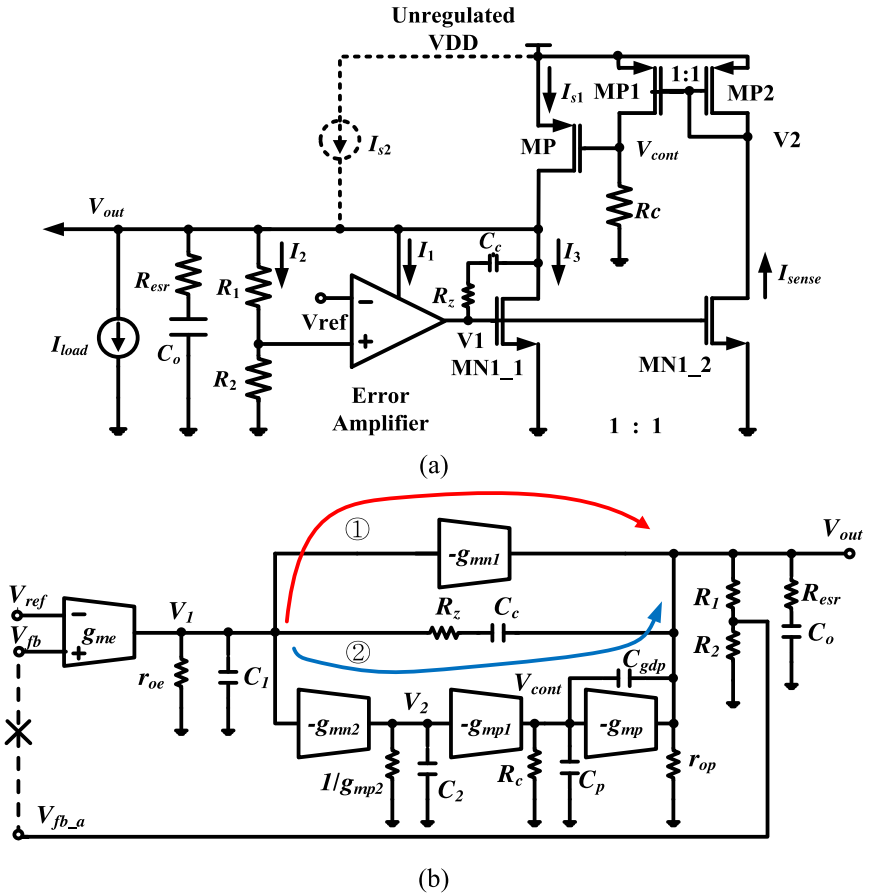

Fig. 2. (a) Proposed shunt regulator architecture (b) small signal equivalent model.

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have the same transconductance as well. C_1 is parasitic capacitors at V1 node excluding the miller effect. C_2 is parasitic capacitors at V2 node. C_p is the total parasitic capacitor at the gate of MP and it consists of gate-source capacitor (C_{gsp}), miller effected capacitance of C_{gdp}, which is the gate-drain capacitor of MP, and other parasitic capacitors which can be ignored. The order of capacitance size is $C_o \gg C_c \gg C_p \gg C_{gdp}$. r_{oe} and r_{op} are the output impedance of the error amplifier and MP, respectively. The order of impedance is $r_{oe} \gg R_z \gg R_c \gg r_{op} \gg R_{esr}$.

After error amplifier, there are two paths to the output as seen in Fig. 2 (b). First path is through single inverting device MN1_1. Second path is through three inverting devices MN1_2, MP1, and MP. Since the second path gain is much higher than the first path gain, the second path introduces a dominant miller effect. Therefore, miller effect through second path is considered for stability. From the above equation, the proposed shunt regulator is six poles and three zeroes system. The first pole is generated by the output capacitor and output impedance of MP ($p_1 = 1/C_o r_{op}$). External and miller compensation schemes cancel out the second and third poles such as $p_2 = 1/(C_c g_{mn2} g_{mnp} R_c r_{op} r_{oe})$ and $p_3 = 1/(C_p R_c)$ and the others are beyond the unity gain frequency. The pole at V2 node is located at very high frequencies. This system generates positive zero due to C_{gdp}, but the zero location is at higher frequencies than unity gain frequency. Then, this zero does not have effect on the stability, neither does other non-dominant poles. Therefore, the stability of the shunt regulator is guaranteed.

Third, depending on the error amplifier architecture, the LDO output has the minimum voltage limitation. In other words, the output of the regulator should be higher than the minimum required voltage to operate the error amplifier. Fourth, comparing prior shunt regulator architecture as seen in Fig. 1, quiescent current of the proposed regulator at no load condition is reduced significantly and quiescent current is decreased at heavy load conditions. The NMOS pass device MN1_1 and NMOS sense device MN1_2 do not need to be large geometry devices. The PMOS pass device MP still needs to be a large geometry device depending on current driving capability.

In addition, the current source I_{s2} can be added, depending on the application, to achieve a faster transient response. This current source can be implemented as a simple current mirror circuit and provide the specific amount of current for the regulator to operate at no load condition. It means that the pass device does not provide any current. This accelerates the transient response when loading conditions change abruptly from maximum to no current.

4 Simulation and comparison

The proposed shunt regulator is designed using 0.5 μm standard digital CMOS process and simulated with Cadence. To verify the performance of the proposed regulator, transient response and PSR characteristics are simulated and compared with a series regulator, which is composed of the same ampli-

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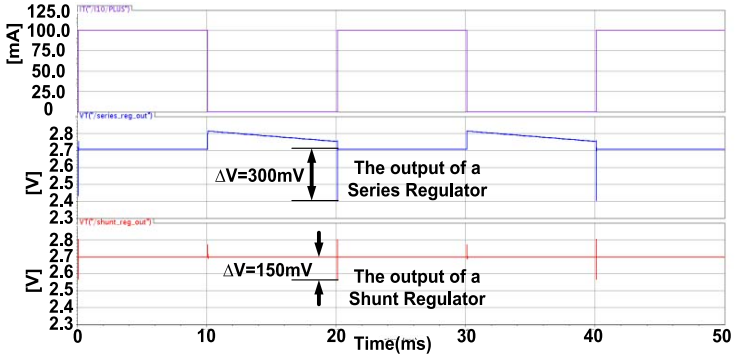
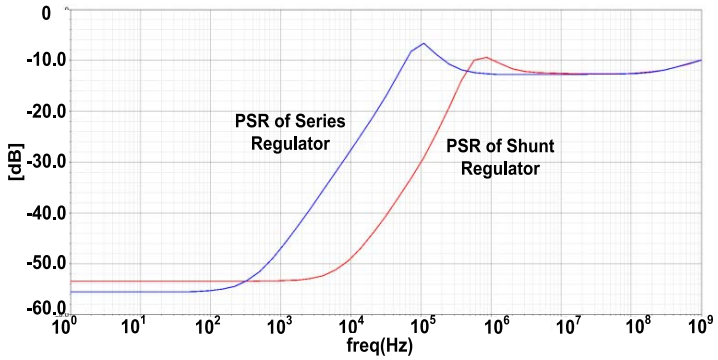
fier as used in the shunt regulator. Both regulators have the same geometry pass device and output capacitor ($C_o = 1\,\mu$F) and effective series resistance ($R_{esr} = 0.5\,\Omega$). Fig. 3 shows the transient and PSR response of a conventional series and novel shunt regulator.

Fig. 3 (a) shows transient response of each regulator over a full loading current step (0 to 100 mA). The transient settling time of the series regulator shows 14.34 μsec and more than 10 msec at the rising and falling of the current step. The transient response of the proposed shunt regulator shows 3.98 μsec and 99.4 μsec at the rising and falling of the full load transient step. From the simulation results, the proposed shunt regulator achieved at least 3.5 times fast settling response than the series regulator. The transient voltage variation (ΔV) is smaller than that of series regulator. Fig. 3 (b) shows



(a)



(b)

	Series regulator	Shunt regulator
Vin [V]	3~5	
Vout [V]	2.7	
Quiescent current Iq [μA]	100.5	100.9
Current efficiency [%]	99.91	99.87
PSR	-27.1dB @ 10 kHz	-48.5dB @ 10 kHz
Transient time [μsec]	14.34 @ (I_{load}:0 → 100 mA)	3.98 @ (I_{load}:0 → 100 mA)
	>10,000 @ (I_{load}:100 → 0 mA)	99.4 @ (I_{load}:100 → 0 mA)
Load regulation	0.087 mV/mA	0.015 mV/mA

(c)

Fig. 3. (a) Transient response, (b) PSR response of series and proposed shunt regulators, (c) Performance comparison table.

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PSR response of each regulator at full load current. The PSR response of series regulator is −40 dB at 2.4 kHz and −20 dB at 23.4 kHz. The proposed shunt regulator shows a wider PSR response such as −40 dB at 34.4 kHz and −20 dB at 238.7 kHz. Fig. 3 (c) shows the performance of proposed regulator compared with series regulator.

5 Conclusion

In this paper a novel shunt regulator is presented. The proposed regulator shows a fast transient response over heavy loading variation. In addition, the proposed regulator shows wide range power supply rejection characteristics. The proposed fast transient response shunt regulator will contribute to the improved performance of power management integrated circuits in future.

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