LETTER
IEICE Electronics Express, Vol.11, No.12, 1–6

Interface circuit of sigma-delta accelerometer with on-chip-test function

Xiaowei Liu[1], **Honglin Xu**[1], **Chong He**[1], **and Mingyuan Ren**[1,2a)]
[1] *MEMS Center, Harbin Institute of Technology, No.92, Street Xidazhi, Harbin, China*
[2] *School of Software, Harbin University of Science and Technology, No.23, Road Sandadongli, Harbin, China*
a) *xhlzf2006@126.com*

Abstract: A fifth-order fully differential interface circuit (IC) with on-chip-test function is presented to improve the noise performance for micromechanical sigma-delta (Σ-Δ) accelerometer. The proposed on-chip-test technique for Σ-Δ accelerometers avoids a shaker table applying a sinusoidal signal as the simulated acceleration which involves distortion itself. An electrostatic force feedback linearization circuit is presented to reduce the harmonic distortion resulting in a larger dynamic range (DR). The post-simulation results show that the electrostatic force feedback linearization circuit decreases the harmonic distortion effectively and the proposed on-chip-test technique achieves 98 dB third-order harmonic distortion detection, and the nonlinearity of the proposed circuit is 0.02%.

Keywords: interface circuit, on-chip-test, sigma-delta, linearization
Classification: Integrated circuits

References

[1] Y. F. Dong, M. Kraft and W. R. White: IEEE Trans. Instrum. Meas. **56** (2007) 1666. DOI:10.1109/TIM.2007.904477
[2] Gannon and Jeffery: Meeting of the Society of Exploration Geophysicists (1999).
[3] Goldberg and Howard: Proc. of Sensor Expo Fall 2000 (2000) 479.
[4] J. F. Wu and L. R. Carley: IEEE Trans. Circuits Syst. I **53** (2006) 274. DOI:10.1109/TCSI.2005.857084
[5] Y. Dong, M. Kraft and W. R. White: J. Micromech. Microeng. **16** (2006) S54. DOI:10.1088/0960-1317/16/6/S09

1 Introduction

Micromechanical Σ-Δ accelerometers have been proven to improve linearity, dynamic range and bandwidth, and also provide a direct digital output [1]. Previous work mainly focused on low noise, stability and higher-order architecture. However, the harmonic distortion is an important performance for

© IEICE 2014
DOI: 10.1587/elex.11.20140320
Received April 6, 2014
Accepted April 28, 2014
Publicized May 23, 2014
Copyedited June 25, 2014

micromechanical Σ-Δ sensors. The conventional method is to use a shaker table to make the off-chip-test for accelerometers which depends on the precision of the vibration table. The distortion of high precision vibration table is usually larger than 0.003%, so distortion within the vibration table limits the distortion measurement [2, 3]. In addition, a high precision vibration table is very expensive.

This letter proposes the on-chip-test technique for a high-order Σ-Δ accelerometer to measure distortion without using vibration table. The high precision vibration table is not needed any more, and the harmonic distortion of the sensor interface is tested easily and truly. A lead compensator is adopted in the proposed fifth-order IC to ensure stability of the closed-loop high-order system. A low noise capacitance detection circuit is also described with a correlated-double-sampling (CDS) technique to decrease 1/f noise and offset of the operational amplifier. In addition, to improve the linearity and DR of the accelerometer, a force feedback linearization circuit is proposed.

2 Proposed architecture

Fig. 1 presents a fifth-order feedforward and distributed-feedback (DFFF) topology for micromechanical Σ-Δ accelerometer. This topology is advantageous in a larger input range and a lower integrator output swing. To ensure the robust stability of high order system, a lead compensator is inserted between the displacement-voltage conversion and third-order modulator. The lead compensator is described in z-domain shown as:

$$H_{cm}(z) = 1 - \alpha z^{-1} \quad (1)$$

α in (1) is the compensation factor which compensates the second-order micromechanical transducer to obtain sufficient stability margin [4].

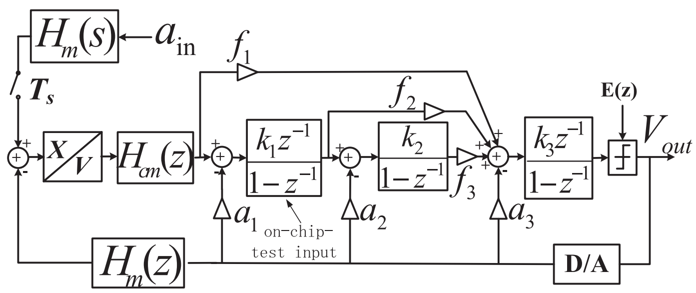

Fig. 1. Proposed fifth-order DFFF topology for micromechanical Σ-Δ accelerometer

The on-chip-test input is applied to the first integrator which is presented in Fig. 1. The relationship between on-chip-test input signal amplitude and system output in low frequency is given in (2):

$$\frac{Y_0}{V_{self}} = \frac{1}{a_1 + (1-\alpha) A_{XV} H_m A_{VF}} \quad (2)$$

In this expression, a_1 is the feedback factor of the first integrator. A_{XV} is the

© IEICE 2014
DOI: 10.1587/elex.11.20140320
Received April 6, 2014
Accepted April 28, 2014
Publicized May 23, 2014
Copyedited June 25, 2014

IEICE Electronics Express, Vol.11, No.12, 1–6

gain of displacement-voltage conversion. H_m is the low frequency gain of the micromechanical transducer. A_{VF} is the gain of voltage-force conversion.

3 Circuit realization

Fig. 2 presents the interface circuit diagram of micromechanical Σ-Δ accelerometer which consists of charge sensitization, CDS and hold, lead compensator, Σ-Δ modulator, 1-bit DAC and linearization circuit. In Fig. 2, electrostatic feedback and charge sensitization are accomplished in different phases of one cycle, which greatly eliminates feedthrough between feedback signal and pick-up charge signal. The Σ-Δ modulator circuit applied in Fig. 2 with on-chip-test input is shown in Fig. 3. Selecting the first integrator as the input of on-chip-test is the best choice for the Σ-Δ accelerometer which will not change the poles of system and ensure a maximum dynamic range. A sinusoidal signal as a simulated acceleration is applied to the input in the on-chip-test mode, otherwise the on-chip-test voltage is V_{ref}.

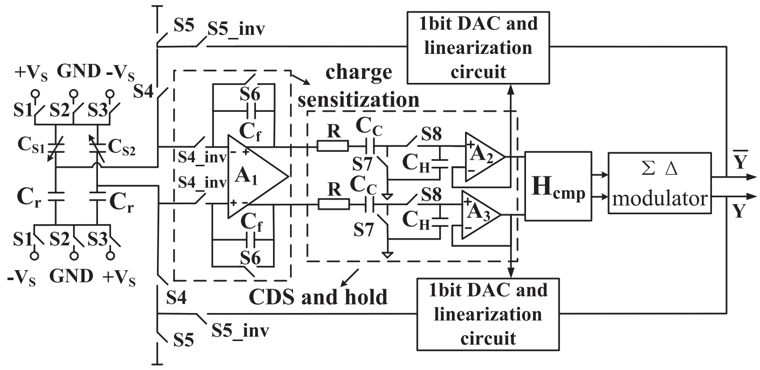

Fig. 2. Micromechanical Σ-Δ accelerometer interface circuit

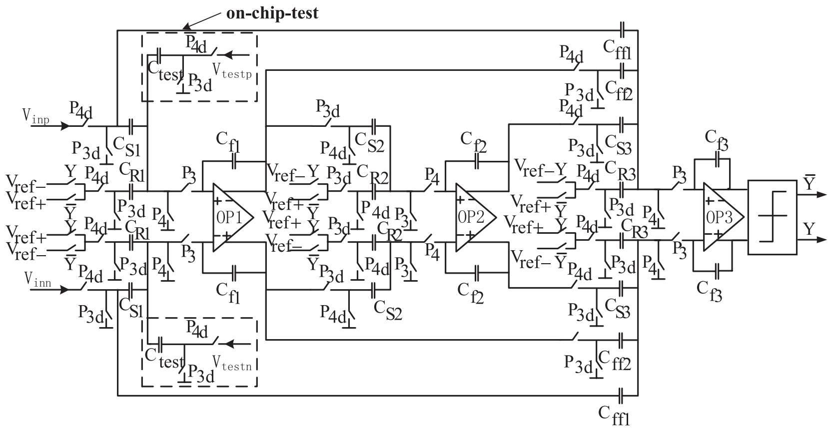

Fig. 3. Σ-Δ modulator applied in accelerometer interface circuit with on-chip-test input

The relationship shown in (2) can be rewritten by the following expression:

$$\frac{Y_0}{V_{self}} = \frac{C_f d_0{}^2 M}{a_1 C_f d_0{}^2 M + 4(1-\alpha) V_r{}^2 C_0{}^2 H_m} \tag{3}$$

© IEICE 2014
DOI: 10.1587/elex.11.20140320
Received April 6, 2014
Accepted April 28, 2014
Publicized May 23, 2014
Copyedited June 25, 2014

Where C_f is the integration capacitance, d_0 is the initial sensing gap distance, M is the proof mass, V_r is the reference voltage and C_0 is the static capacitance of the mass and electrode.

An ideal 1-bit DAC is linear, but for a mechanical accelerometer, the conversion of a voltage to an electrostatic feedback force on the proof mass is nonlinear which depends on the residual proof mass motion and is described as [5]:

$$F = \mathrm{sgn}(Y)\frac{2C_0{V_{ref}}^2}{d_0\left(1-\mathrm{sgn}(Y)\dfrac{x}{d_0}\right)^2} \tag{4}$$

where x is the proof mass motion. It indicates that the conversion is nonlinear. To reduce the nonlinearity of the electrostatic force feedback, an electrostatic force feedback linearization circuit is proposed in Fig. 4.

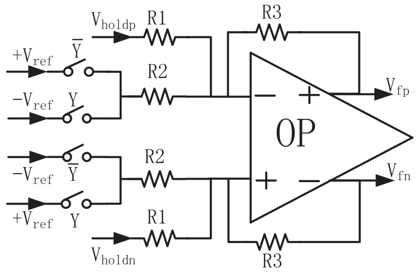

Fig. 4. Electrostatic force feedback linearization circuit

The feedback voltage V_f in Fig. 4 can be written as:

$$V_f = sgn(Y)V_{ref}\frac{R_3}{R_2} - V_{hold}\frac{R_3}{R_1} \tag{5}$$

Where V_{hold} is the hold voltage shown as:

$$V_{hold} = \frac{2C_0V_{ref}x}{C_fd_0} \tag{6}$$

If $R_3 = R_2$ and $R_3 = R_1\dfrac{C_f}{2C_0}$, then:

$$V_f = sgn(Y)V_{ref} - \frac{x}{d_0}V_{ref} = sgn(Y)V_{ref}\left(1 - sgn(Y)\frac{x}{d_0}\right) \tag{7}$$

Replacing the feedback voltage V_{ref} in (4) with (7), the electrostatic feedback force is changed to

$$F = \mathrm{sgn}(Y)\frac{2C_0{V_{ref}}^2}{d_0} \tag{8}$$

The linearization circuit eliminates the nonlinearity of electrostatic force feedback which is independent on the mass motion.

4 Layout and post-simulation results

The layout of the IC shown in Fig. 5 is implemented in a standard CMOS technology and operates at a sampling frequency of 250 kHz. The active circuit area is about 7.8 mm^2.

© IEICE 2014
DOI: 10.1587/elex.11.20140320
Received April 6, 2014
Accepted April 28, 2014
Publicized May 23, 2014
Copyedited June 25, 2014

IEICE Electronics Express, Vol.11, No.12, 1–6

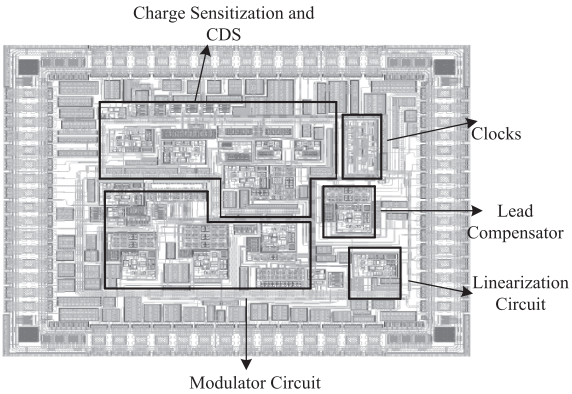

Fig. 5. Layout of Σ-Δ accelerometer interface circuit

To prove the validity of the on-chip-test function, a sinusoidal signal with amplitude of 150 mV worked at 244.14 Hz is applied to the proposed accelerometer interface circuit. A 65536-bit digital output sequence of the post-simulation result is calculated to obtain the output power spectral density (PSD) and shown in Fig. 6. The result indicates that the noise floor of the digital accelerometer is about $-140\,\text{dBV/Hz}^{1/2}$ at low frequency, the sensitivity is 321 mV/g. The on-chip-test function is achieved with an 89 dB third-order harmonic distortion.

Fig. 7 is the on-chip-test result with electrostatic force feedback linearization, and a 98.2 dB third-order harmonic distortion is gotten, and the second-order harmonic distortion disappears. To vary the amplitude of on-chip-test voltage from 150 mV to 500 mV, the output amplitudes of the post-simulation results and the calculated results in (3) are both given in Fig. 8. The nonlinearity of on-chip-test result is 0.02%, and the output amplitude is proportional to the on-chip-test voltage which coincides with relation described in (3).

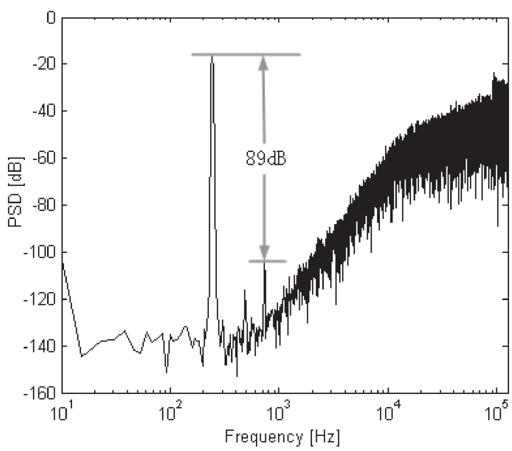

Fig. 6. PSD for the on-chip-test output of Σ-Δ accelerometer

© IEICE 2014
DOI: 10.1587/elex.11.20140320
Received April 6, 2014
Accepted April 28, 2014
Publicized May 23, 2014
Copyedited June 25, 2014

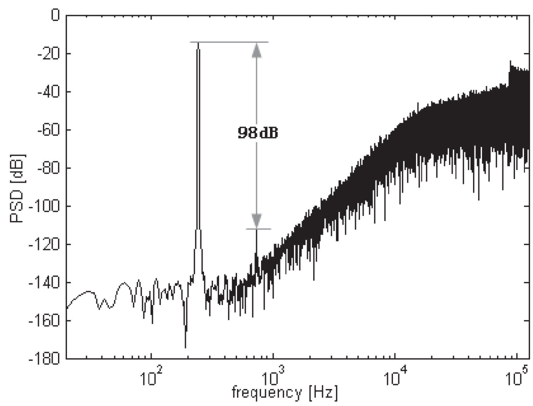

Fig. 7. On-chip-test result with force feedback linearization

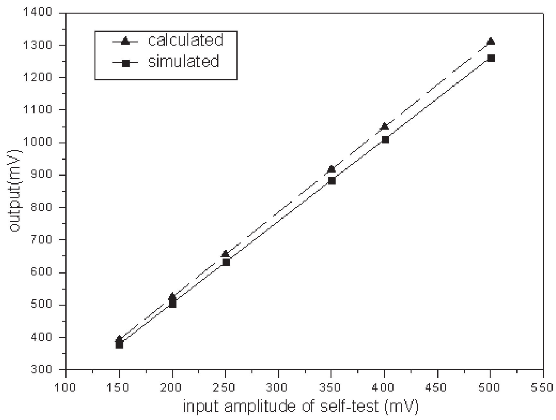

Fig. 8. Relation between amplitudes of on-chip-test input and output

5 Conclusions

The on-chip-test technique is presented to measure distortion of micromechanical Σ-Δ accelerometer without using vibration table in this paper. To verify the effectiveness of the proposed technique, a fifth-order DFFF topology Σ-Δ interface circuit is designed for micromechanical accelerometer. To reduce the distortion caused by electrostatic force feedback nonlinearity, a linearization circuit is proposed. The post-simulation results confirm that the on-chip-test and linearization circuits are effective and agree with the calculated results.

Acknowledgments

This work was supported by National Natural Science Foundation of China (Project 61204121) and National Hi-Tech Research and Development Program of China (863 Program) (Grant No. 2013AA041107).

© IEICE 2014
DOI: 10.1587/elex.11.20140320
Received April 6, 2014
Accepted April 28, 2014
Publicized May 23, 2014
Copyedited June 25, 2014