

A modified H-bridge multilevel inverter for photovoltaic system

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Abstract: This paper presents a modified H-bridge seven-level single-phase grid-connected inverter for photovoltaic system with a novel pulse-width-modulated (PWM) control scheme. The inverter is capable of producing seven output-voltage levels (V_{dc} , $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$) from the dc supply voltage. Perturb and Observe (P&O) algorithm is used to extract maximum power from the PV module. MPPT and current control algorithm were implemented in an eZdsp board, TMS320F2812. The proposed system was implemented in a prototype.

Keywords: multilevel inverter, PWM, current control

Classification: Science and engineering for electronics

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1 Introduction

Various single-phase grid-connected inverter topologies for low-power photovoltaic systems have been suggested or used. Recently, multilevel inverter topologies are popular in photovoltaic systems. Multilevel inverters offer several advantages over H-bridge conventional inverter. They have nearly-sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI; all making them cheaper, lighter, and more compact [1, 2, 3, 4].

Various topologies for multilevel inverter have been proposed. Common ones are diode-clamped, flying capacitor or multicell, cascaded H-bridge, and modified H-bridge multilevel [6]. The modified H-bridge topology is significantly advantageous over other topologies; less power switch, less anti-parallel diodes, power diodes, and less capacitors for inverters of the same number of levels.

This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode-embedded bidirectional switches and a novel PWM technique. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker and a current-control algorithm.

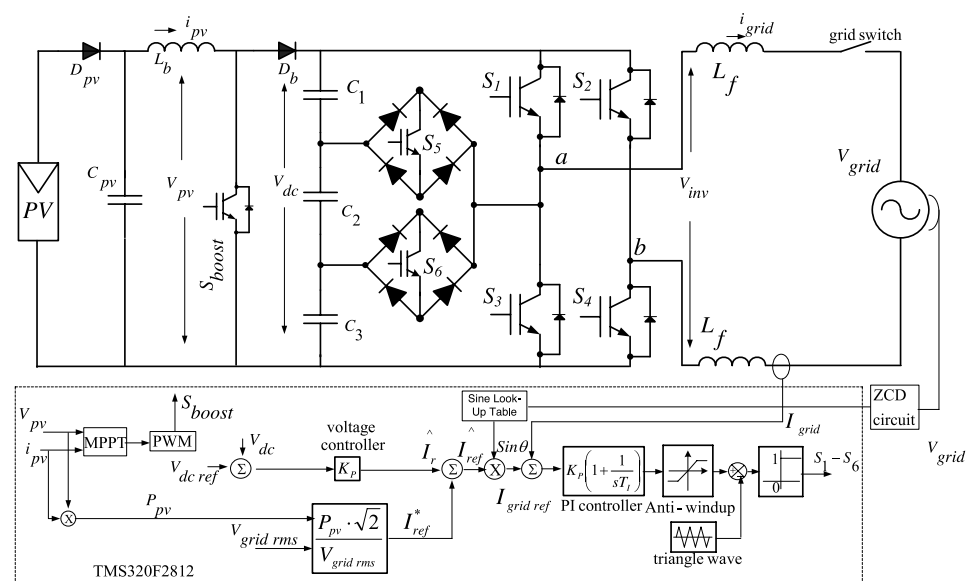


Fig. 1. The proposed multilevel inverter with control algorithm

2 Proposed multilevel inverter topology

The proposed topology comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by C_1 , C_2 , and C_3 as in Fig. 1. Although voltage balancing at each capacitor is

not perfectly balanced, it is still achievable by placing a large capacitor for C_1 , C_2 , and C_3 PV arrays with blocking diode D_{pv} and capacitor C_{pv} were connected to the inverter via a DC-DC boost converter. As this topology is used in a grid-connected system, the power from the PV solar arrays is transferred to the power network rather than to a load. The DC-DC boost converter is used to step up inverter output voltage V_{inv} to more than $\sqrt{2}$ of grid voltage V_g to ensure power flow from PV arrays to the grid. Since no transformer is used, V_{inv} should be more than 340V (assuming $V_g = 240V$). A filtering inductance L_f was used to filter the current injected into the grid.

Proper switching of the inverter can produce seven output-voltage levels. Table I shows the switching combinations that generated the seven output-voltage levels (V_{dc} , $2V_{dc}/3$, $V_{dc}/3$, 0 , $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$). For voltage level 0^* or 0 , they are the same, however, for commutation purposes, the switch configuration is different for the zero voltage level in the first half cycle of the output voltage from that in the second half cycle.

Table I. output voltage according to switches on-off condition

V_{inv}	S1	S2	S3	S4	S5	S6
V _{dc}	on	off	off	on	off	off
2V _{dc} /3	off	off	off	on	on	off
V _{dc} /3	off	off	off	on	off	on
0	off	off	on	on	off	off
0*	on	on	off	off	off	off
-V _{dc} /3	off	on	off	off	on	off
-2V _{dc} /3	off	on	off	off	off	on
-V _{dc}	off	on	on	off	off	off

3 PWM modulation

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals, V_{ref1} , V_{ref2} and V_{ref3} were in turns compared with the carrier signal $V_{carrier}$. The reference signals had the same frequency and amplitude, and were in phase with an offset value equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If V_{ref1} had exceeded the peak amplitude of $V_{carrier}$, V_{ref2} was compared with $V_{carrier}$ until it had exceeded the peak amplitude of $V_{carrier}$. Then onwards, V_{ref3} would take charge and would be compared with $V_{carrier}$ until it reached zero. Once V_{ref3} had reached zero, V_{ref2} would be compared until it reached zero. Then onwards, V_{ref1} would be compared with $V_{carrier}$. Fig. 2 shows the resulting switching pattern. Switches S_1 , S_3 , S_5 , and S_6 would be switching at the rate of the carrier signal frequency, whereas S_2 and S_4 would operate at a frequency equivalent to the fundamental frequency.

For one cycle of the fundamental frequency, the proposed inverter operated through six modes. The six modes are described as follows:

Mode 1: $0 < \omega t < \theta_1$, and $\theta_4 < \omega t < \pi$

Mode 2: $\theta_1 < \omega t < \theta_2$, and $\theta_3 < \omega t < \theta_4$

$$\begin{aligned}
 &\text{Mode 3: } \theta_2 < \omega t < \theta_3 \\
 &\text{Mode 4: } \pi < \omega t < \theta_5, \text{ and } \theta_8 < \omega t < 2\pi \\
 &\text{Mode 5: } \theta_5 < \omega t < \theta_6, \text{ and } \theta_7 < \omega t < \theta_8, \\
 &\text{Mode 6: } \theta_6 < \omega t < \theta_7,
 \end{aligned} \tag{1}$$

The phase angle θ_1 - θ_7 depends on modulation index M_a . Theoretically, for a single reference signal and a single carrier signal, the modulation index is defined to be

$$M_a = \frac{A_m}{A_c} \tag{2}$$

While for dual reference signal and single carrier signal, the modulation index is defined to be [7]

$$M_a = \frac{A_m}{2A_c} \tag{3}$$

As the proposed seven-level PWM inverter uses three reference signals, the modulation index is defined to be

$$M_a = \frac{A_m}{3A_c} \tag{4}$$

Where A_c is the per unit (pu) peak-to-peak value of the carrier signal, and A_m is the (pu) peak value of the voltage reference signal V_{ref} .

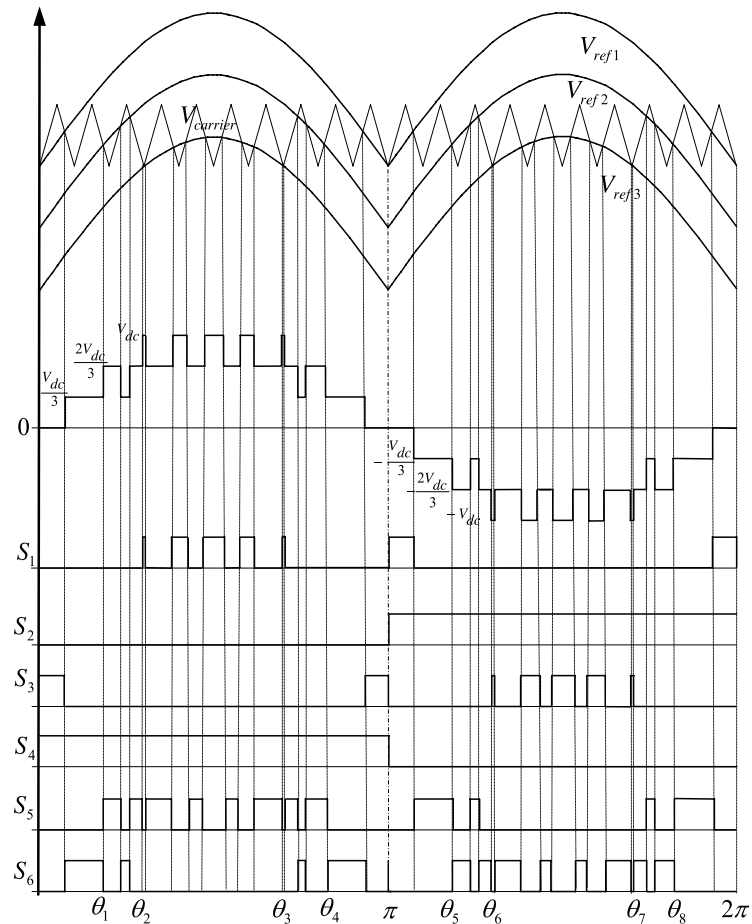


Fig. 2. Switching pattern for the single-phase seven-level inverter

When the modulation index is less than 0.33, the phase-angle displacement is

$$\theta_1 = \theta_2 = \theta_3 = \theta_4 = \frac{\pi}{2} \quad (5)$$

$$\theta_5 = \theta_6 = \theta_7 = \theta_8 = \frac{3\pi}{2} \quad (6)$$

On the other hand, when the modulation index is more than 0.33 and less than 0.66, the phase-angle displacement is determined by

$$\begin{aligned} \theta_1 = \sin^{-1} \left(\frac{A_c}{A_m} \right) \quad ; \quad \theta_2 = \theta_3 = \frac{\pi}{2}; \quad \theta_4 = \pi - \theta_1; \\ \theta_5 = \pi + \theta_1; \quad \theta_6 = \theta_7 = \frac{3\pi}{2}; \quad \theta_8 = 2\pi - \theta_1 \end{aligned} \quad (7)$$

If the modulation index is more than 0.66, the phase-angle displacement is determined by

$$\begin{aligned} \theta_1 = \sin^{-1} \left(\frac{A_c}{A_m} \right) \quad ; \quad \theta_2 = \sin^{-1} \left(\frac{2A_c}{A_m} \right) \\ \theta_3 = \pi - \theta_2; \quad \theta_4 = \pi - \theta_1; \\ \theta_5 = \pi + \theta_1; \quad \theta_6 = \pi + \theta_2; \\ \theta_7 = 2\pi - \theta_2; \quad \theta_8 = 2\pi - \theta_1. \end{aligned}$$

For M_a equal to, or less than, 0.33, only the lower reference wave, V_{ref3} is compared with the triangular carrier signal. The inverter's behavior is similar to a conventional full-bridge three-level PWM inverter. However, if M_a is more than 0.33 and less than 0.66, only V_{ref2} and V_{ref3} reference signals are compared with the triangular carrier wave. The output voltage consists of five dc-voltage levels. The modulation index is set to be more than 0.66, for seven levels of output voltage to be produced. Three reference signals have to be compared with the triangular carrier signal to produce switching signals for the switches.

4 Control system

Fig. 1 shows the control system, which comprises a maximum-power-point tracker (MPPT) algorithm, a DC-bus voltage controller, reference-current generation, and a current controller. Two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, also with grid-voltage harmonics present. The proposed inverter uses the P&O algorithm for its wide usage in MPPT owing to its simple structure and requirement of only a few measured parameters. It periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with that of the previous perturbation cycle. If the power increased the perturbation continues in the same direction in the next cycle, otherwise, the direction reverses. This means the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm oscillates around it.

P&O algorithm was implemented in the DC-DC boost converter. The output of the MPPT is the duty-cycle function. As the dc-link voltage V_{DC}

was controlled in the DC-AC seven-level PWM inverter, the change of the duty-cycle changes voltage at the output of the PV panels. A DC voltage controller with proportional gain was implemented to keep the output voltage of the dc-dc boost converter, V_{dc} , constant, by comparing V_{dc} and V_{dcref} and feeding the error into the voltage controller which then tries to reduce the error. In this way, V_{dc} can be maintained, and at more than $\sqrt{2}$ of V_{grid} to inject power into the grid.

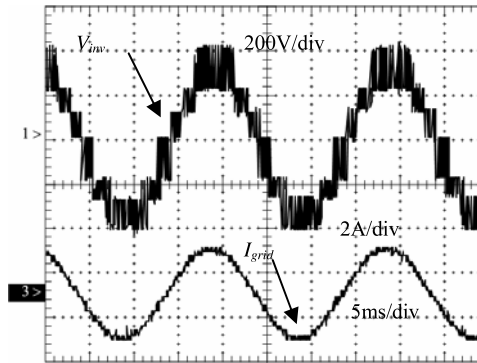
To deliver energy to grid, frequency and phase of the PV inverter must equal those of the grid; therefore a grid synchronization method is needed. The sine lookup table that generates reference current must be brought into phase with the grid voltage (V_{grid}). For this, the grid period and phase must be detected. The proposed inverter provides an analog zero-crossing detection (ZCD) circuit on one of its input ports where the grid voltage is to be connected. The zero-crossing circuit then produces an in-phase square-wave output which is fed into the digital I/O port on the eZdsp board, TMS320F2812.

PI algorithm was used as the feedback current controller for the application. The current injected into the grid, also known as grid current I_{grid} , was sensed and fed back to a comparator that compared it with the reference current $I_{gridref}$. $I_{gridref}$ is the result of the MPPT algorithm. The error from comparing I_{grid} with $I_{gridref}$ was fed into the PI controller. The output of the PI controller, known also as V_{ref} , goes through an anti-windup process before being compared with the triangular wave to produce the switching signals for S_1 to S_6 . Eventually, V_{ref} becomes V_{ref1} ; V_{ref2} and V_{ref3} can be derived from V_{ref1} by shifting the offset value, which is equivalent to the amplitude of the triangular wave. The mathematical formulation of the PI algorithm and its implementation in the DSP are detailed in [4].

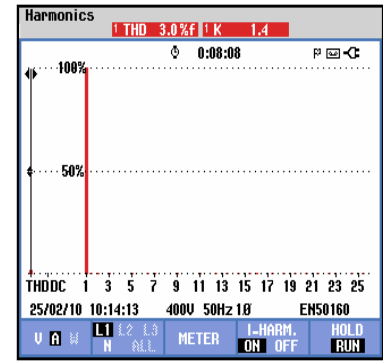
5 Experiment result

TMS320F2812 DSP was used to implement the control algorithm. 750 W PV arrays were used as the inverter's input source. Ten SIEMENS SP75 modules were connected in series to produce 750 W of peak power. For this experiment prototype, the value of L_b is 3 mH and L_f is 5 mH. Capacitance value of 4400 μ F is used for C_1 , C_2 and C_3 respectively. Fig. 3a shows the experiment results for V_{inv} and I_{grid} . V_{inv} consists of seven output-voltage levels, and I_{grid} had been filtered to resemble a pure sinewave. At this instant, the modulation index Ma was above 0.66. The dc-bus voltage was set to 400V to inject current into the grid. The waveforms for when Ma was reduced, shown in Figures 3c and 3e.

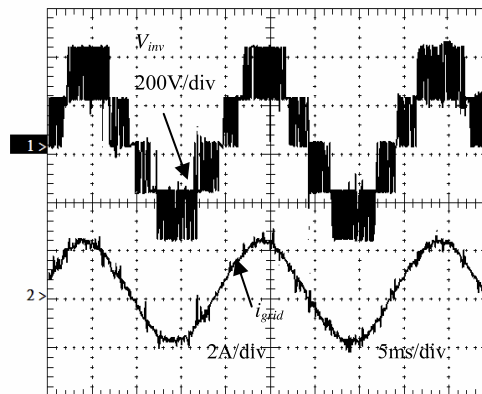
FLUKE 434 Power Quality Analyzer measured the THD and the power factor. The THD measurement of Fig. 3b corresponds to the waveform of Fig. 3a, while THD measurements of Figures 3d and 3f correspond to the waveforms of Figures 3c and 3e, respectively. Comparing all three THD measurements, the seven-level inverter produced the lowest THD compared with the five-level and the three-level ones. This proves that as the level increases, the THD reduces, which is an essential criterion for grid-connected



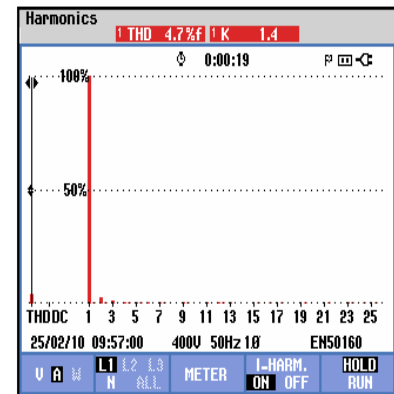
(a)



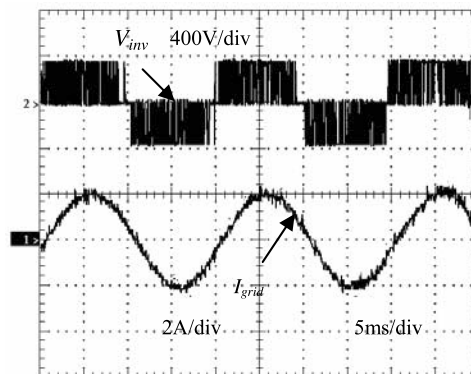
(b)



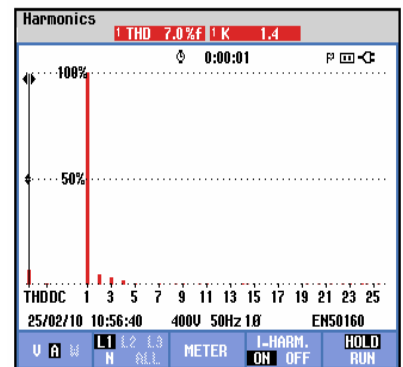
(c)



(d)



(e)



(f)

Fig. 3. (a) Experiment results of V_{inv} and I_{grid} for seven levels, (b) current THD for seven levels, (c) V_{inv} and I_{grid} for five levels, (d) current THD for five levels, (e) V_{inv} and I_{grid} for three levels, (f) current THD for three levels.

PV systems.

6 Conclusion

This paper presented a single-phase seven-level inverter for PV application with a novel PWM switching scheme. PWM switching signals were generated by comparing three reference signals with a triangular carrier signal. The circuit topology, control algorithm, and operational principle of the proposed

inverter were analyzed. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. Less THD in the seven-level inverter compared with that in the five-level and the three-level inverters is an attractive solution for grid-connected PV inverters.