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Switched capacitor bandgap voltage reference for sub-1-V operation

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Abstract: A switched capacitor bandgap voltage reference circuit capable of sub-1-V operation is presented. The proposed circuit generates a sub-1-V reference voltage with a switched capacitor operation, offering several performance advantages over the current-mode sub-1-V counterpart. The proposed design provides an improved supply rejection and outperforms in the presence of process variation. In addition, the circuit does not require a start-up circuit and the associating trimming circuitry is simplistic and cost effective. The proposed sub-1-V switched capacitor BGR can be a practical sub-1-V reference candidate in ultra deep sub-micron CMOS processes.

Keywords: CMOS, voltage reference, sub-1-V, switched capacitor

Classification: Integrated circuits

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1 Introduction

The need for stable, precise on-chip voltage references in numerous system-on-a-chip (SoC) applications continues to call for the bandgap voltage reference (BGR) circuit. As its name suggests, the output voltage of a conven-

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tional BGR is close to the band-gap voltage of silicon, which is approximately 1.2 V at room temperature [1]. However, as CMOS technology scales down to 130 nm and lower, the conventional BGR is no longer compatible with 1.2-V or lower supply voltage.

Banba et al. [2] proposed a current mode BGR capable of sub-1-V operation. Although the circuit is capable of generating sub-1-V output voltage, there are significant performance issues that must be considered. First is the compromised power supply rejection (PSR) and line regulation, which is more prominent with decreasing MOSFET output resistance due to scaling feature size and less use of cascode circuit topologies due to shrinking supply voltage. Another potential problem is the existence of both positive and negative feedback loops with nearly identical loop gain, which can cause instability or start-up difficulty.

Apart from the continuous-time BGR, discrete-time BGR circuits by Westwick [3] and Gilbert [4] are attractive for clocked systems. Both circuits use a switched capacitor network in conjunction with one p-n junction diode to form the core of the circuit, whose operation consists of a pre-charge mode and reference voltage mode. There are several important advantages these switched capacitor BGR circuits have over the continuous-time BGR: the diode device mismatch is eliminated by using a single p-n junction diode, the PSR of the switched capacitor BGR is better, and the circuit is less vulnerable to process variation with capacitor matching. Although Gilbert's switched capacitor BGR cannot generate a sub-1-V output whereas Westwick's BGR can (further demonstrated by Gregoire [5]), Gilbert's BGR is superior in its performance and simplicity. More specifically, Gilbert's BGR has a more reasonable common-mode voltage level for its operational amplifier (thus simplifying the opamp design), less dependence on matching between switches, and requires more simplistic control signals [4]. The proposed BGR circuit inherits these desirable merits while generating a sub-1-V output, offering compatibility with deep sub-micron processes.

2 Circuit Description

Fig. 1 shows the proposed switched capacitor sub-1-V BGR. The circuit consists of two ratioed current sources (I_1 and I_2), an opamp, a p-n junction diode (D_1), and a switched capacitor network (S_1-S_4 and C_1-C_3). Two phases are involved in its operation, which are pre-charge/reset phase ($\Phi1$) and reference output phase ($\Phi2$). In these two phases, a different level of current is injected into D_1 generating two different voltage drops, to emulate ΔV_{BE} from two BJT-based diodes with different emitter sizes as in a conventional BGR [1]. With the switching operation, a proportional-to-absolute temperature (PTAT) voltage is generated and combined with a complementary-to-absolute temperature (CTAT) voltage to achieve a temperature stable voltage in $\Phi2$.

During $\Phi1$, the switches S_1, S_4 are closed and S_2, S_3 are open. With the current I_1 being injected into D_1, the negative feedback action of the opamp

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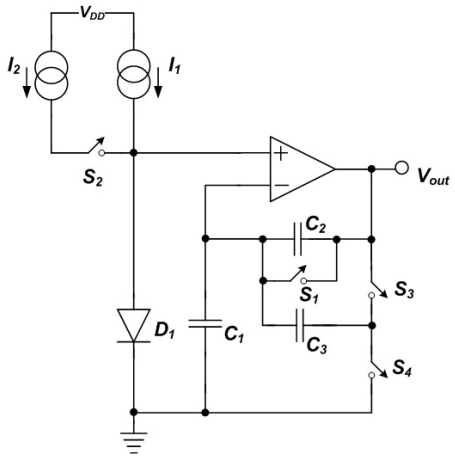

Fig. 1. Schematic of the proposed sub-1-V switched capacitor BGR

places voltage V_{D1} across the parallel capacitors C_1 and C_3, where V_{D1} is given by

$$V_{D1} = nV_T \ln\left(I_1/I_S\right) \tag{1}$$

where V_T is the thermal voltage and n is the emission coefficient of the diode.

During $\Phi 2$, the switches S_1, S_4 are open and S_2, S_3 are closed, and the sum of currents I_1 and I_2 is injected into D_1. The voltage at the opamp's minus input terminal becomes

$$V_{D2} = nV_T \ln\left[\left(I_1 + I_2\right)/I_S\right]. \tag{2}$$

Alternating between these two phases, the charge stored in capacitor combination of C_1 and C_3 is conserved and redistributed among C_1, C_2, and C_3. Thus, the output voltage in $\Phi 2$ can be written as

$$V_{OUT} = \frac{C_2}{C_2 + C_3}\left[V_{D2} + \frac{C_1 + C_3}{C_2}\ln\left(\frac{I_1 + I_2}{I_1}\right)\cdot V_T + V_{OS}\right] \tag{3}$$

where V_{OS} is the offset voltage of the opamp, assuming opamp offset varies negligibly between the two phases. Note the sub-1-V BGR output voltage is a bandgap voltage (the bracketed term in equation (3)) scaled by the factor $C_2/(C_2+C_3)$. The offset voltage caused by the opamp is also scaled by the same factor, which in turns reduces the temperature drift impact from opamp offset.

In order to achieve a precise reference in the presence of process variation, a trimming method is necessary. The proposed sub-1-V switched capacitor BGR enables efficient trimming that can be readily implemented in design and suitable for commercial applications. For the conventional BGR, the slope of the PTAT voltage vs. temperature characteristic is established by physical layout of the design, therefore trimming is often done by altering one of the resistors (e.g., laser trimming). For the switched capacitor BGR, the PTAT voltage slope can be altered by injecting a small current level into the p-n junction diode, which can provide trimming functionality with relatively small silicon area and low complexity. A possible implementation would be

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using a current-mode digital-to-analog converter (DAC) and connecting it to the non-inverting terminal of the opamp in the BGR circuit. To design a sub-1-V switched capacitor BGR for fabrication, dummy current mirrors can be included to provide additional trimming flexibility via a metal mask change or possibly on-chip fuses.

3 Simulation Results

The proposed switched capacitor BGR is simulated using a BSIM3V3 model for a 130-nm commercial CMOS process. The circuit uses 1.2-V supply and standard threshold devices. The current mirror ratio, I_2 to I_1, is chosen to be 12 to 4. And the capacitor C_1, C_2, and C_3 are 2.71 pF, 2.17 pF, and 2.17 pF, respectively. The device sizes are carefully chosen with consideration of optimum matching for physical design.

Fig. 2 (a) shows the switched capacitor BGR output voltage at multiple temperatures. Calibrated with current-mode DAC, the optimum temperature drift is less than 250 μV in the entire temperature range, as Fig. 2 (b) shows. In the design, a two-phase non-overlapping clock generator is used to control the switching between $\Phi 1$ and $\Phi 2$. The BGR outputs roughly a diode turn-on voltage during $\Phi 1$ and approximately 552 mV reference output during $\Phi 2$. A non-symmetrical duty cycle can be readily implemented to maximize the reference voltage phase duration. The opamp is designed to provide 30 pF load driving capability and the switches are carefully sized to minimize their 'ON' resistance.

As mentioned previously, the switched capacitor BGR has the advantage of better immunity to process variation and PSR/line regulation compared to continuous-time sub-1-V output BGRs. Monte-Carlo statistical simulation was performed on this proposed sub-1-V switched capacitor BGR, and the output voltage spread is shown in Fig. 3. At room temperature, the sub-1 V switched capacitor BGR has a 3δ-dispersion of 5.8%, as compared to 8.8% from Banba's current-mode sub-1-V BGR circuit designed in the same process. The PSR/line regulation improvement is approximately 20 dB over the current-mode design. In addition, the sub-1-V switched capacitor BGR

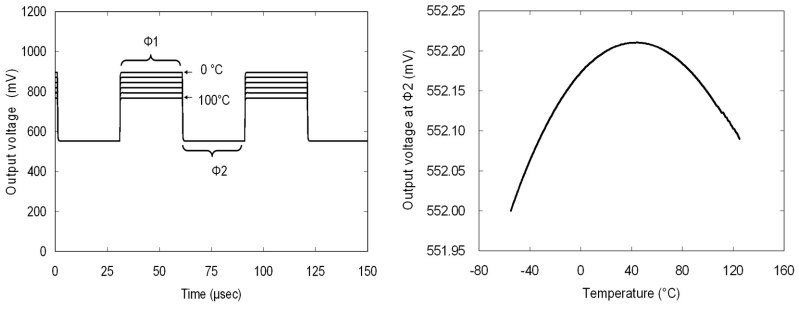

Fig. 2. (a) Output voltage of switched capacitor sub-1-V BGR at 0°C, 20°C, 40°C, 60°C, 80°C, and 100°C, (b) Output voltage from −55°C to 125°C during phase $\Phi 2$

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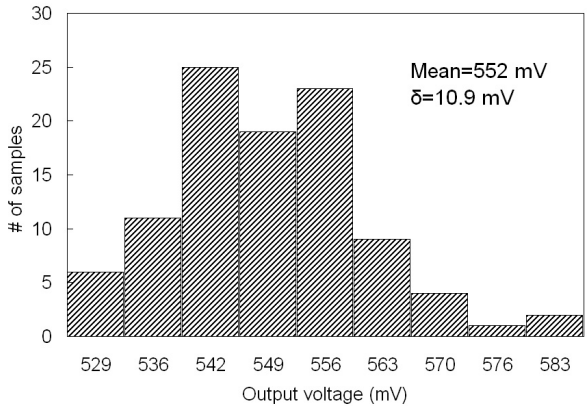

Fig. 3. Sub-1-V switched capacitor BGR output voltage distribution using Monte-Carlo statistical simulation (100 runs) at room temperature

does not require a start-up circuit, which reduces circuit complexity and power consumption.

4 Conclusion

A novel switched capacitor BGR that enables sub-1-V operation is presented. The circuit operation is discussed and simulation results are provided. Compare to the current-mode sub-1-V BGR, the proposed sub-1-V switched capacitor BGR has several advantages. It provides an improved supply rejection and does not require a start-up circuit. Also, it performs better in the presence of process variation and the associating trimming circuitry is more simplistic and cost effective. The proposed sub-1-V switched capacitor BGR can be an attractive approach for generating a stable sub-1-V reference voltage in ultra deep sub-micron CMOS processes.

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