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Modeling and optimization of noise coupling in TSV-based 3D ICs

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Abstract: This paper first proposes an impedance-level model of coupling channel between through silicon vias (TSVs) based on the two-port network theory. In order to get an accurate estimation of the coupling level from TSV-TSV in the early designing stage, we convert the impedance parameters of the model into the ABCD matrix to derive the formula of coupling coefficient, and the accuracy of the proposed formula is validated by comparing with 3D full-wave simulations. Furthermore, a design technique of optimizing the coupling between TSVs is proposed, and through SPICE simulations the proposed technique shows a desirable result to reduce the TSV-TSV coupling.

Keywords: 3D integration, though silicon via (TSV), two-port network, equivalent impedance, noise coupling reduction

Classification: Integrated circuits

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1 Introduction

3D integration is considered as a feasible solution to preserve Moore's law by providing vertical interconnects for stacked dies using through silicon vias (TSVs) [1]. However, with the technology scaling and TSV count rising, TSV-TSV noise coupling becomes a major coupling source in 3D integrated circuits (3D ICs) and can have a significantly negative impact on signal integrity.

Previous works reported about the techniques to reduce TSV-induced noise typically include using coaxial TSVs [2] and providing a backside ground [3].

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However, manufacturing coaxial TSVs is not mature and the additional manufacturing steps cost more than regular cylinder-shaped TSVs. And for [3], it introduces unnecessary inductance coupling by placing a metal ground between adjacent dies.

In this paper, we first propose an impedance-level model of TSV-TSV coupling channel based on the two-port network theory, and then by employing ABCD matrix, the coupling coefficient from TSV-TSV can be precisely estimated with a wide frequency range. Furthermore, we propose a design technique to optimize the TSV-TSV coupling achieved by tuning the port impedances.

2 Modeling of TSV-TSV coupling channel based on two-port network

Fig. 1 shows the physical structure of TSV-based 3D IC comprised of stacked dies which are vertically connected by the Ground-Signal-Signal-Ground (GSSG)-type TSV. The GSSG-type TSV is used as the TSV-TSV coupling test vehicle in this paper which is established in a 3D full-wave EM simulator HFSS, and the design parameters and material properties are listed in Table I.

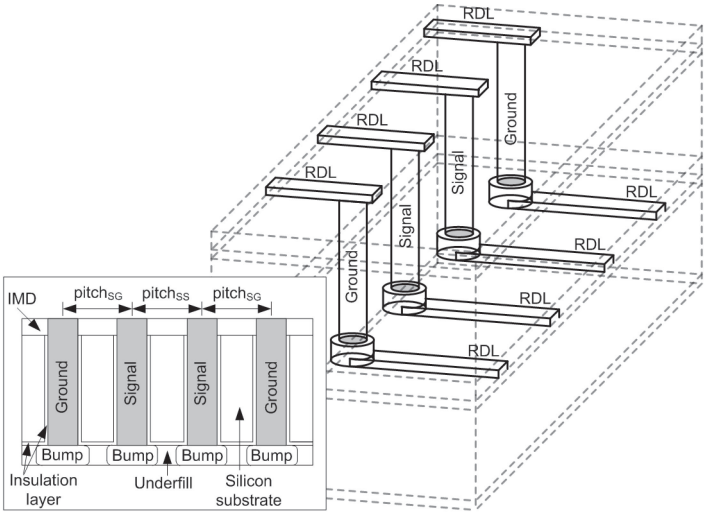

Fig. 1. Physical structure of GSSG-type TSV in 3D IC.

Table I. Design parameters used in this paper

Design parameter	Value	Design parameter	Value
TSV diameter (d_{TSV})	6 µm	IMD height (l_{IMD})	5 µm
TSV height (l_{TSV})	60 µm	Underfill height ($l_{underfill}$)	8 µm
Bump height (l_{Bump})	8 µm	Conductivity of silicon (σ_{si})	10 S·m
Bump diameter (d_{Bump})	10 µm	Dielectric constant of silicon (ε_{si})	11.8
Pitch between SS TSVs (p_{SS})	20 µm	Dielectric constant of insulator (ε_{ox})	4
Pitch between SG TSVs (p_{SG})	30 µm	Dielectric constant of IMD (ε_{IMD})	4
Insulator thickness (t_{ox})	0.5 µm	Dielectric constant of underfill ($\varepsilon_{underfill}$)	4.2
Silicon substrate height (l_{si})	55 µm		

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As shown in Fig. 1, there are four TSVs in parallel in the GSSG configuration. The inner two signal TSVs provide vertical interconnects for signal delivery between stacked dies. The rest two TSVs on the external sides known as ground TSVs do not transfer signals but act as an indispensable part for stacked dies in 3D IC by providing the reference ground for signal delivery. To deliver signals horizontally, the redistribution layer (RDL) line placed above the inter-metal dielectric (IMD) layer plays a significant role in providing a horizontal interconnect to redistribute signals between adjacent stacked dies, and the bump in the underfill layer provides a joint for adjacent stacked dies. Since the TSV is a vertical interconnect via filled with metal which penetrates the entire silicon substrate, the coupling effect happens not only on the surface of the silicon substrate, but also deep inside the substrate, which is more complicated as compared to the coupling in traditional 2D systems.

To analyze the TSV-TSV coupling, we should first determine and investigate the TSV-TSV coupling channel. Between two adjacent TSVs, there are the silicon substrate layer and the IMD layer, and both of the layers contribute to the coupling channel. Since the silicon substrate is very lossy, there is not only the resistance (R_{si}), but also the capacitance (C_{si}) existing between the two TSVs in the silicon substrate layer. And in the IMD layer, the capacitance (C_{IMD}) exists between the two TSVs as well. Meanwhile, in the underfill layer, the coupling capacitance (C_{Bump}) existing between two bumps also contributes to the coupling channel. Moreover, to prevent the DC leakage between the TSV and the conductive silicon substrate, a thin oxide insulation layer is surrounded with the TSV, and the insulation layer typically has a thickness of a few tenths of a micrometer, thus leading to a large capacitance (C_{ox}) between the TSV and the silicon substrate. Therefore, the coupling channel can be considered as a function of C_{si}, R_{si}, C_{IMD}, C_{Bump}, and C_{ox}. The values of these components can be obtained by using the formulas in [4].

$$C = \frac{\pi \varepsilon l}{\cosh^{-1}(p/d)} \tag{1}$$

$$R_{si} = \frac{\varepsilon_{si}}{C_{si}\sigma_{si}} \tag{2}$$

$$C_{ox} = \frac{1}{4} \frac{2\pi\varepsilon_{ox} l_{TSV}}{\ln\left(\dfrac{d_{TSV}/2 + t_{ox}}{d_{TSV}/2}\right)} \tag{3}$$

It is worth to note that C_{si}, C_{IMD}, C_{Bump} are all calculated in Eq. (1) with putting the proper parameters such as the pitch (p), the diameter (d), the dielectric constant (ε), and the height (l) of corresponding material, and all the parameter values are provided in Table I.

The impedance-level model of TSV-TSV coupling channel based on the two-port network is proposed in Fig. 2. Z_1 and Z_2 are the equivalent impedance between adjacent Signal-Ground (SG) TSVs, and Z_1 equals to Z_2 due to the symmetry of GSSG configuration. Z_3 represents the equivalent impedance of the coupling channel between Signal-Signal (SS) TSVs. The expressions of Z_1, Z_2 and Z_3 are listed below,

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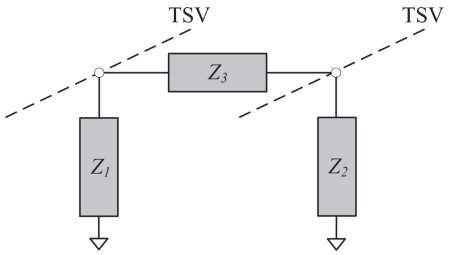

Fig. 2. Impedance-level model of TSV-TSV coupling channel.

$$Z_1(\omega) = Z_2(\omega) = 1/j\omega C_{IMD(SG)} \parallel (Z_{si(SG)}(\omega) + 4/j\omega C_{ox}) \parallel 1/j\omega C_{Bump(SG)} \parallel Z_{port}, \tag{4}$$

$$Z_3(\omega) = 1/j\omega C_{IMD(SS)} \parallel (Z_{si(SS)}(\omega) + 4/j\omega C_{ox}) \parallel 1/j\omega C_{Bump(SS)}, \tag{5}$$

where Z_{si} is the impedance between two adjacent TSVs in the silicon substrate, and can be expressed as,

$$Z_{si}(\omega) = R_{si} \parallel 1/j\omega C_{si} \tag{6}$$

To obtain an accurate estimation of the coupling level in the early designing stage, we convert the impedance parameters as shown above into the ABCD matrix of the model in Fig. 2 to derive the formula of coupling coefficient between two coupled TSVs.

The ABCD matrix of the model with the two-port network structure has the form,

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}, \tag{7}$$

where V and I are the port voltage and current. Based on the model shown in Fig. 2, we can obtain,

$$A = \left.\frac{V_1}{V_2}\right|_{I_2=0} = 1 + Z_3/Z_2 \tag{8}$$

$$B = \left.\frac{V_1}{I_2}\right|_{V_2=0} = Z_3 \tag{9}$$

$$C = \left.\frac{I_1}{V_2}\right|_{I_2=0} = 1/Z_1 + 1/Z_2 + Z_3/(Z_1Z_2) \tag{10}$$

$$D = \left.\frac{I_1}{I_2}\right|_{V_2=0} = 1 + Z_3/Z_1 \tag{11}$$

Thus, the ABCD matrix is expressed as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 + Z_3/Z_2 & Z_3 \\ 1/Z_1 + 1/Z_2 + Z_3/(Z_1Z_2) & 1 + Z_3/Z_1 \end{bmatrix} \tag{12}$$

With the definition of transmission characteristic for a two-port network, the formula of coupling coefficient (S_{21}) can be derived from the ABCD matrix as,

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} = \frac{2Z_1Z_2}{Z_1Z_2 + Z_A + Z_BZ_0 + Z_C/Z_0}, \tag{13}$$

where Z_0 is the normalized impedance, and Z_A, Z_B, and Z_C are given as

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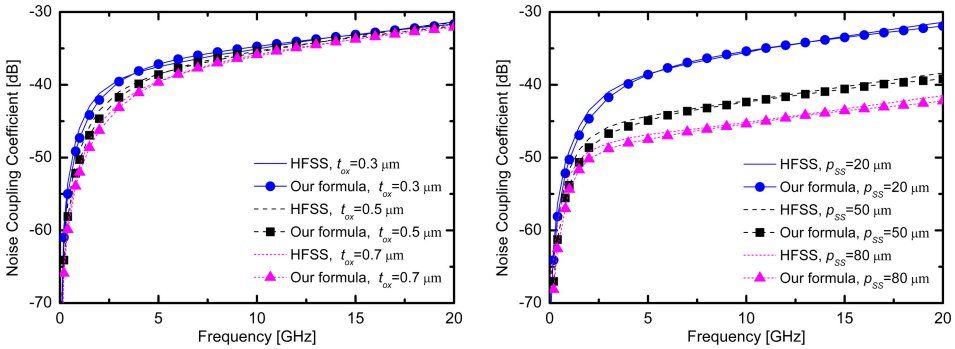
$$Z_A = Z_1Z_2 + Z_1Z_3 + Z_2Z_3 \tag{14}$$

$$Z_B = Z_1 + Z_2 + Z_3 \tag{15}$$

$$Z_C = Z_1Z_2Z_3 \tag{16}$$

To validate the accuracy of the proposed formula of coupling coefficient in Eq. (13), we compare it with the 3D full-wave simulator HFSS. As can be observed from Fig. 3(a) and 3(b), the coupling coefficient from the proposed formula and HFSS simulation show a good correlation up to 20 GHz. By increasing the insulator thickness (t_{ox}) and the pitch between SS TSVs (p_{SS}), the coupling level decreases. That is due to the fact that the decreased C_{ox} and increased R_{si} make Z_3 larger, resulting in the improved coupling coefficient between the two coupled TSVs. And the changing trend of the coupling coefficient due to the variation of design parameters has been well captured by the proposed formula.



(a) (b)

Fig. 3. Comparison results of the proposed formula and HFSS, (a) with t_{ox} variation, and (b) with p_{SS} variation.

3 A design technique of optimizing TSV-TSV noise coupling

Fig. 4(a) shows the structure of two coupled TSVs. Since the TSV impedance comprised of the TSV resistance and inductance is very low due to the short TSV height, the TSV impedance is ignored in this structure. We consider one TSV as an aggressor, and the other as a victim. A buffer is connected with the TSV on the source and sink end, respectively, functioning as the driver and load. Thus, each single TSV can be considered as driven by R_{dr} and terminated with C_{load} as shown in Fig. 4(a). The simplified model for coupling analysis is presented in Fig. 4(b). Z_{port1}, Z_{port2}, Z_{port3} and Z_{port4} are the port impedances which represent the TSVs termination conditions. Z_3 is the impedance of the coupling channel between the two coupled TSVs. To reduce the TSV-TSV noise coupling, the most direct and intuitive way is to increase the distance between the two coupled TSVs to make Z_3 higher, however, this inevitably leads to a large area overhead. In this paper, we propose a technique of tuning port impedances to optimize the noise coupling.

As shown in Fig. 4(b), I_1 is the source current flowing from the driving port to node A on the aggressor net, and I_2 is the current flowing from A to the sink. I_3 is the coupling current induced by the coupled TSVs flowing between A and B, and on the victim net I_3 is divided into two branches of I_{31} and I_{32}. In order to reduce

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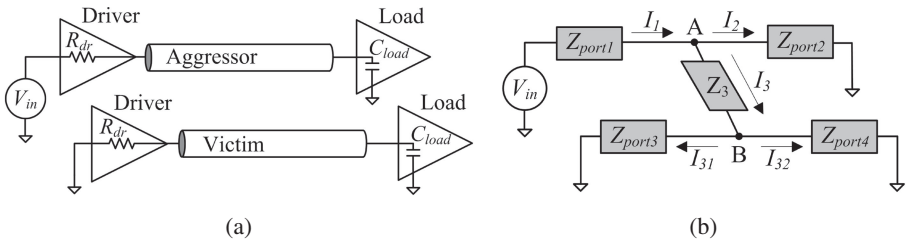

Fig. 4. (a) Structure of two coupled TSVs, and (b) its simplified model for coupling analysis.

the coupling between the aggressor and victim TSV, we can reduce the coupling current I_3 by either increasing I_2 (to decrease Z_{port2}) or decreasing I_1 (to increase Z_{port1}) according to Kirchhoff's Current Law. Furthermore, if I_3 is assumed as a fixed value from the coupling channel, we can also reduce the coupling by lowering the voltage at B, which can be achieved by optimizing the port impedances on the victim net (to decrease Z_{port3} and Z_{port4}). Here, we adjust the gate size of the buffer on each end of the TSV to tune the port impedances. All buffers are implemented in standard CMOS technology provided by NCSU 45 nm PDK. We perform SPICE simulations to observe the impact of gate sizing on the coupling noise voltage, and the simulation results are shown in Fig. 5.

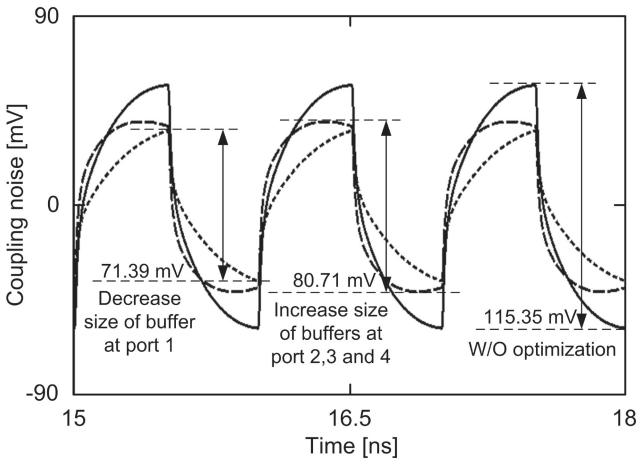

Fig. 5. Coupling noise voltage measured at the load of the victim TSV with a 1 GHz input signal injected into the driving port of the aggressor TSV.

The size of buffer used for initial simulation setup is two times (2×) as big as that of the minimum-sized buffer. A rectangular input signal V_{in} with a rising/falling time of 10 ps is injected into the driving port (Port 1) of the aggressor, and the coupling noise voltage is measured at the load (port 4) of the victim. As shown in Fig. 5, by decreasing the size of buffer (to 1× minimum size) at port 1 and increasing the size of buffers (to 4× minimum size) at the rest three ports, the peak-peak coupling noise voltage can be optimized by 38% and 30%, respectively. Therefore, it indicates that tuning the port impedances can be used as a powerful knob for adjusting variables in coupled TSVs, and this bring more freedom for designers to achieve the goal of noise coupling reduction between coupled TSVs.

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4 Conclusion

In this paper, we first proposed an impedance-level model of TSV-TSV coupling channel based on two-port network, and then we derived the formula of coupling coefficient by employing the ABCD matrix of the model. The comparison results of the proposed formula and HFSS showed a good correlation, which validated the accuracy of the proposed formula. Furthermore, a design technique to reduce the noise coupling between two coupled TSVs was proposed. By adjusting the size of buffers only two times at the driving port (port 1) and at the rest three ports (port 2, 3 and 4), the peak-peak coupling noise voltage can be optimized by 38% and 30%, respectively.

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