

Tri-level capacitor-splitting switching scheme with high energy-efficiency for SAR ADCs

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Abstract: An energy-efficient tri-level capacitor-splitting switching algorithm for successive approximation register (SAR) analog-to-digital converters (ADCs) is proposed. The proposed switching scheme is a combination of the zero-power-consumption switching algorithm and the one-side double-level switching technique. By zero-power-consumption switching algorithm, there is no switching power dissipation during the first three bit cycles. Furthermore, only one-side capacitors are switched between two reference voltages (ground and V_{CM}) during the remaining bit conversions, which is more energy-saving than the monotonic switching method. The proposed switching method reduces the switching energy by 50.59% compared to the Sanyal and Sun proposed one.

Keywords: switching scheme, one-side double-level, capacitor-splitting, energy-efficient

Classification: Integrated circuits

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1 Introduction

In SAR ADCs, the main sources of power consumption are the comparator, the digital control logic and the capacitive digital-to-analog converter (DAC). Dynamic comparator consumes no static current and the digital control logic benefits from the technology scaling. Therefore, the capacitive DAC dominates the overall power consumption. In recent years, some low-power switching methods have been actively introduced to reduce the switching energy of the capacitive DAC [1, 2, 3, 4, 5, 6, 7, 8, 9, 10]. The split-capacitor technique [1] achieves 37% switching energy reduction compared to the conventional one. The set and down switching technique [2] achieves 81% reduction in switching energy. The charge-average switching method [3] reduces switching energy by 93.5%. The common-mode voltage V_{CM} , which is $V_{REF}/2$, is introduced in [4] with 87.5% less switching energy, whereas a 96.89% reduction is achieved by the new tri-level switching scheme in [5]. [6, 7, 8] are more energy-efficient, but involve more switches and references. By optimizing the tri-level switching algorithm, [9, 10] achieve lower power consumption, 98.43% and 98.83% less, respectively. However, the switching scheme from the fourth bit cycle in [9, 10] is not energy-efficient as monotonic switching algorithm is used. In this Letter, an energy-efficient tri-level capacitor-splitting switching scheme is proposed which achieves 99.23% switching energy reduction.

2 Proposed tri-level capacitor-splitting switching scheme

By zero-power-consumption switching scheme similar to those in [9, 10], the first three bit cycles consume no power, leading to more power reduction because of large switched capacitor value and voltage variation. To reduce the switching energy during generations of the remaining bits, the switching algorithm is realized by one-side double-level switching technique, as shown in Fig. 1. The principle is that capacitors are switched upward or downward on only one side. Besides, only two reference voltages, ground and V_{CM} instead of ground and V_{REF} , are used.

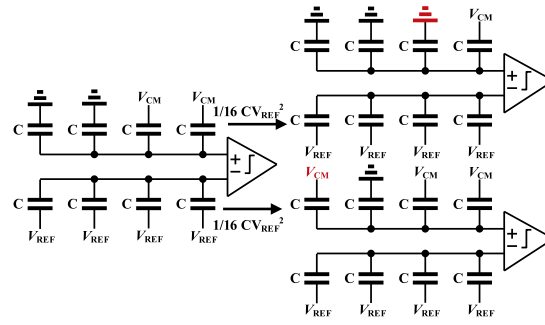


Fig. 1. Illustration of idea of one-side double-level switching scheme

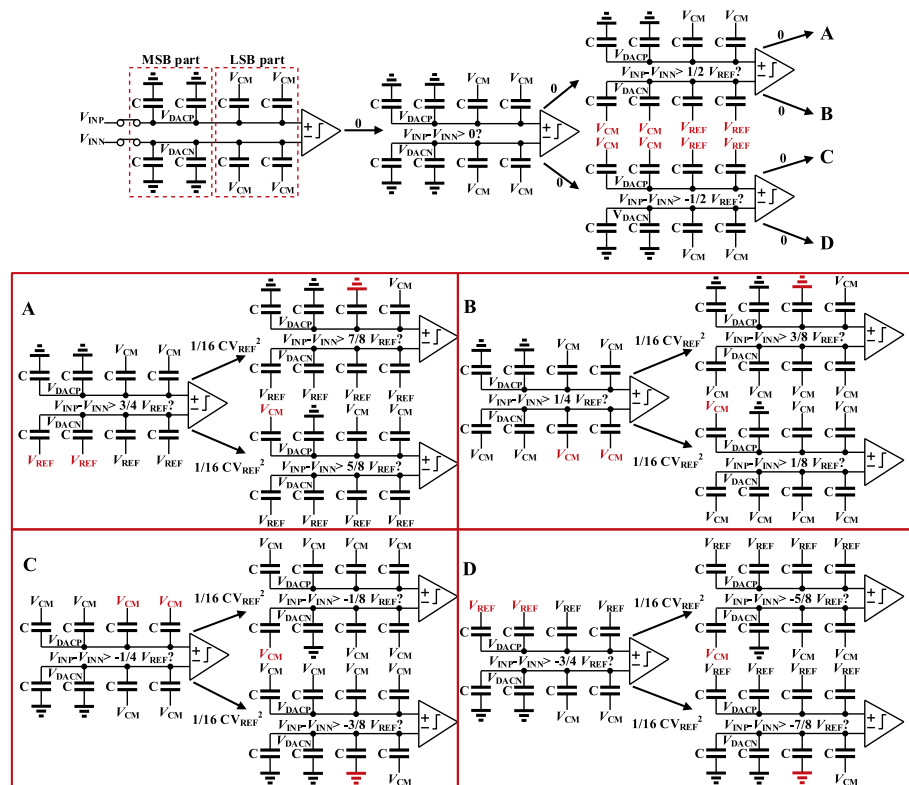


Fig. 2. Proposed switching scheme with 4-bit SAR ADC

Fig. 2 demonstrates the proposed switching scheme with 4-bit SAR ADC. During the sampling phase, the input signal is sampled on the top plates of the capacitors with the bottom plates of the most significant bit (MSB) part capacitors and the least significant bit (LSB) part capacitors set to ground and V_{CM} , respectively. MSB is obtained with no switching power dissipated. Then, the LSB part capacitors on the lower voltage side are switched from V_{CM} to V_{REF} and the MSB part capacitors on the same side from ground to V_{CM} with capacitors on the other side unchanged. There is also no power consumption to get the second bit. For simplicity, only the MSB = “1” is described. If the second bit is “1”, the MSB part capacitors on the V_{DACN} side are switched from V_{CM} to V_{REF} ; if the second bit is “0”, the LSB part capacitors on the V_{DACN} side are switched from V_{REF} to V_{CM} . By comparison, the third bit is achieved. Fortunately, this bit cycle consumes no power. If the third bit is “1”, the largest capacitor in the LSB part on the V_{DACP} side is

switched from V_{CM} to ground; otherwise, the largest capacitor in the MSB part on the V_{DACP} side is switched from ground to V_{CM} . Then, the fourth bit is achieved by another comparison. The former bit cycle is repeated until the LSB is obtained.

3 Switching energy analysis

The behavioral simulation of the proposed tri-level capacitor-splitting switching scheme for a 10-bit SAR ADC was performed in MATLAB. Its switching energy is compared with those in [9, 10], shown in Table I. The proposed switching algorithm requires only $10.54 CV_{REF}^2$ average switching energy, 50.59% less than that in [9]. The average switching energy for the N-bit SAR ADC is given below:

$$E_{avg} = \sum_{i=1}^{N-3} 2^{N-6-i} (1 - 2^{-i}) CV_{REF}^2 \quad (1)$$

Fig. 3 shows the switching energy for the proposed switching scheme and those in [9, 10] against the output code. Obviously, the proposed scheme is the most energy-efficient. Besides, four maximum average switching energy points appear at $1/8 V_{FS}$, $3/8 V_{FS}$, $5/8 V_{FS}$ and $7/8 V_{FS}$ because monotonic switching method is not used and only one-side capacitors begin to consume power from the fourth bit cycle.

Table I. Comparison of switching schemes for 10-bit SAR ADC

Switching scheme	Average energy (CV_{REF}^2)	Energy saving (%)
Sanyal and Sun [9]	21.33	Reference
Hybrid [10]	15.88	25.55
This work	10.54	50.59

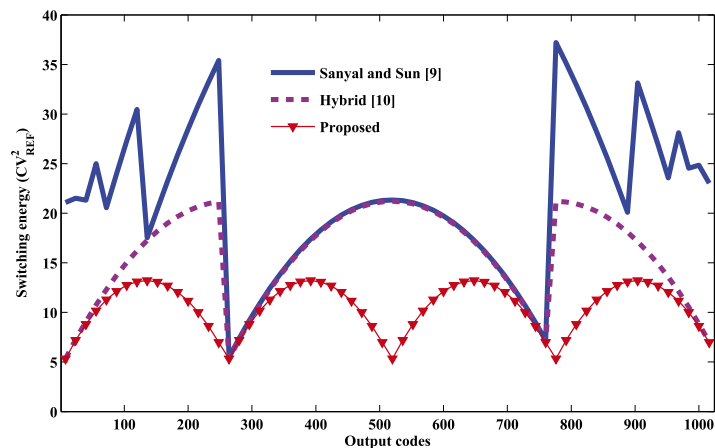


Fig. 3. Switching energy against output code

4 Linearity

As described in (1), the value of the unit capacitor should be as small as possible. However, it is usually determined by the capacitor mismatch. Assume that the unit capacitor obeys a Gaussian distribution, modeled with a nominal value of C_u and a

standard deviation of σ_u . For a binary-weighted capacitor array, each capacitor is unit capacitors in parallel.

The first three MSBs are determined without causing any mismatch. Thus, the maximum DNL (Differential-Nonlinearity) and INL (Integral-Nonlinearity) occur at $1/8V_{FS}$, $3/8V_{FS}$, $5/8V_{FS}$ and $7/8V_{FS}$. Fig. 4 shows behavioral simulation results of 512 Monte Carlo runs of 10-bit DAC with proposed switching scheme. The DNL and INL curves are the root-mean-square (rms) values and unit capacitor is Gaussian random variable with standard deviation of 1% ($\sigma_u/C_u = 0.01$). Clearly, the proposed switching algorithm has good linearity.

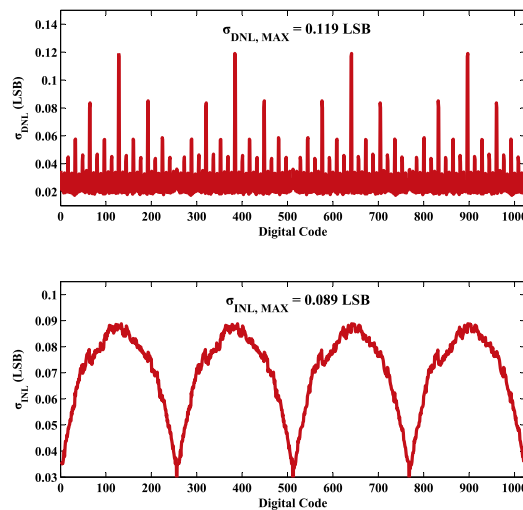


Fig. 4. The standard deviation of DNL and INL versus output

5 Conclusion

A tri-level capacitor-splitting switching scheme with high energy-efficiency for SAR ADCs is proposed. By combining zero-power-consumption switching algorithm and the one-side double-level switching technique, the proposed switching algorithm achieves 50.59% energy-saving compared to the Sanyal and Sun proposed one. Therefore, the proposed switching scheme is more energy-efficient among the reported switching techniques.

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