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Generalized DC-DC multiplier converter topology

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Abstract: Several DC-DC converters based on voltage multipliers have been recently published with advantages such as high voltage gain and few inductors used. This paper presents a generalized topology from which several of the state of the art and new topologies may be derived.

Keywords: DC-DC converter, voltage multiplier, high voltage gain

Classification: Electron devices, circuits, and systems

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1 Introduction

Many applications require a dc-dc converter with high step-up voltage gain, one of the most important and growing applications is the green energy generation, where the low voltage from a renewable energy source needs to be boosted for feeding a load or a grid connected inverter [1, 2, 3, 4, 5, 6].

A high voltage gain is difficult to achieve with traditional topologies of DC-DC converters because of several reasons such as: parasitic components, the requirement of an extreme duty cycles or transformers, this limits the switching frequency and systems size [1, 2]. Several topologies have been proposed to overcome those challenges with high voltage gain without the use of extreme duty cycles [1, 2, 3, 4, 5, 6].

In ref [6] it was presented a derivation of PWM DC-DC hybrid converters by combining traditional converters with the Cockcroft–Walton voltage multiplier, the voltage multiplier of each converter is driven with the same transistor of the basic topology; this fact makes the structure of the new converters very simple and provides high-voltage gain.

In this work it is shown how a multiplier converter can become a generalized topology and how some of the traditional converters and several state-of-the-art converters can be derived from the generalized topology.

2 The Multilevel Boost Converter MBC

Proposed in [1], the MBC combines the boost converter and the Cockcroft-Walton voltage multiplier, see Fig. 1 (a), it contains only one switch, when the switch is closed (Fig. 1 (b)), the capacitor c_{1p} clamps the voltage in c_{2p} by transferring charge throw diode d_{2p}, when the switch opens (Fig. 1 (c)) the inductor current tends to close d_{1p} connecting c_{2p} and c_{3p} to the same potential, then c_{2p} transfer charge to c_{3p} throw d_{3p} since c_{3p} was discharged by the load in the former switching state, this basic operation may be repeated and a full voltage multiplier is driven with only one switch, this behavior makes all capacitor to get the same voltage, and all switches devices to block the same voltage when they are open, leading to a *build-in blocks* topology

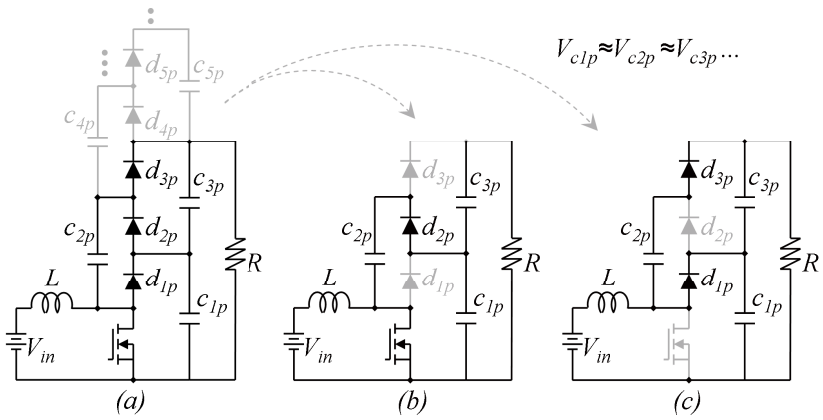

Fig. 1. (a) Generalized topology and two examples of new converters in (b) and (c).

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the voltage multiplier may be extended with more capacitors and diodes (Fig. 1 (a)) leading to a high voltage gain.

The naturally continuous input current along with the high voltage gain, made the MBC suitable for being applied in renewable energy sources where a low dc voltage need to be boosted several times with a continuous input current. Detailed analysis of this interesting topology may be found in [1].

3 The generalized topology

The generalized multiplier converter topology is shown in Fig. 2 (a), similar to the multilevel boost converter [1] with an optional low-pass filter (depends in the selected number of diodes). Diodes and capacitors are labeled and number as positive or negative according with their relative position to the switch.

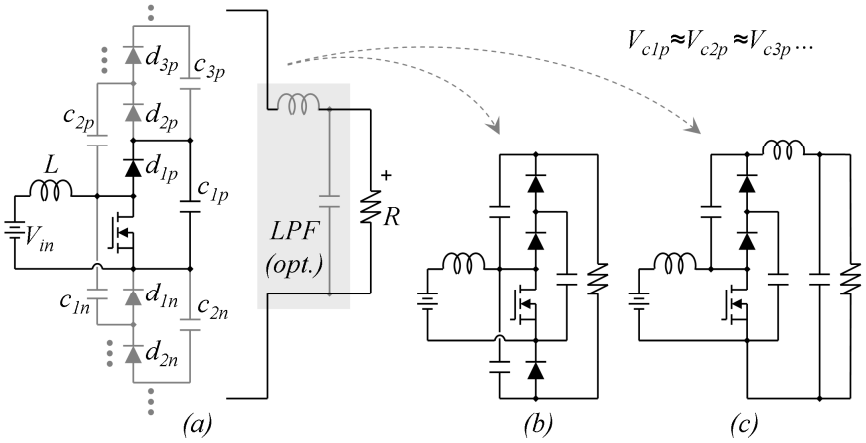

Fig. 2. (a) Generalized topology and two examples of new converters in (b) and (c).

The principle of operation may be as simple as: all even diodes (d_{2p}, d_{2n}, $d_{4p}, d_{4n} \ldots$) are driven synchronized with the switch, and all odd diodes ($d_{1p}, d_{1n}, d_{3p}, d_{3n} \ldots$) switch complementary with the transistor.

The average voltage in each capacitor may be expressed by equation (1).

$$\langle v_C \rangle = \frac{1}{1-D} V_{in} \tag{1}$$

All diodes are connected to the same voltage when they are open, which is the voltage in each capacitor; this is one of the advantages of the topology which follows the multilevel converters principle [1].

In this case since the load is connected along a series of switching devices (diodes and transistor), knowing the average voltage in switching devices is helpful to easily express the voltage in the load.

The average voltage in the switch and diodes synchronized with the switch is:

$$V_d = \langle v_d \rangle = (1-D)\frac{1}{1-D} V_{in} = V_{in} \tag{2}$$

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Which is the voltage in all capacitor times the compliment of the duty cycle (averaging principle), in the other hands the voltage in diodes which are complementary with the switch is:

$$V'_d = \langle v'_d \rangle = D\frac{1}{1-D}V_{in} \tag{3}$$

And finally, the rules for deriving a topology from the generalized topology are two: (i) *Select any number of positive and negative diodes along with their respective capacitors*, and erase components over-under the more positive/negative diode we select. And (ii) *If the load is connected among a series connection of capacitors, do not use the low-pass filter, otherwise use it.*

4 Deriving converters from the generalized topology

Not any topology can be derived from this generalized topology but many of them; it is interesting seeing those simple rules working, all topologies may get a resonant function with soft switching if a proper small resonant inductor is connected in series with C_{2p} and C_{1n}, but this will be cover in a future publication.

For example, let's start following the rules with basic examples:
(i) If only the first positive diode is selected d_{1p} (with its capacitor c_{1p}), the load would be connected among one capacitor and then the low pass filter is not required, this would obtain a traditional boost converter, the output voltage is the sum of V_d plus V'_d, (2) plus (3), which would be the voltage gain in a boost converter. The derivation of the multilevel boost converter [1] is also evident and straight forward but obtaining the voltage gain of specific selection of levels is much easier with the rules described before.
(ii) In Fig. 2 (b) a new converter is shown where the load is connected from d_{1n} to d_{2p}, among two capacitors (c_{1n} and c_{2p}) and then the LPF is not required, the output voltage is equal to the sum of the average voltage in the switch, d_{1p}, d_{2p} and d_{2n}, the switch and d_{2p}, have a V_d voltage while d_{1n} and d_{1p} have a V'_d voltage, and then the load voltage one may add twice of (2) plus twice of (3) and get:

$$V_{out1(b)} = \frac{2}{1-D}V_{in} \tag{4}$$

The same result would be gotten by realizing the load is connected among two capacitors and then the voltage is twice of equation (1).
(iii) Other derived topology is shown in Fig. 2 (c) two diodes are used d_{1p} and d_{2p}, the load is connected among capacitors and diodes (c_{1p} and d_{2p}) and then the LPF is required. Since capacitors have the voltage in (1), and d_{2p} have the voltage expressed in (2) the output voltage would be given by:

$$V_{out1(c)} = V_{c1p} + \langle v_{d2p} \rangle = \left(\frac{1}{1-D} + 1\right) V_{in} = \frac{2-D}{1-D}V_{in} \tag{5}$$

Converters shown in Fig. 2 (b) and 1 (c) are new, but they are only examples of specific topologies derived from the generalized topology, and they won't be deeply studied.

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(iv) By taking d_{1n} and c_{1n} along with d_{1p} and c_{1p}, the result is the converter shown in Fig. 3, since the output is not given by a series of capacitors, the low pass filter is required as stated before, the low pass filter doesn't affect the voltage gain only ensures the output voltage is continuous. Converters shown in Fig. 3 are two of the topologies proposed in [3] as C-switching blocks converters, (same as Fig. 8 and Fig. 15 from [3]). It should be mentioned that authors of [3] got those converter following a different procedure and proposed other topologies which doesn't follow the generalized topology.

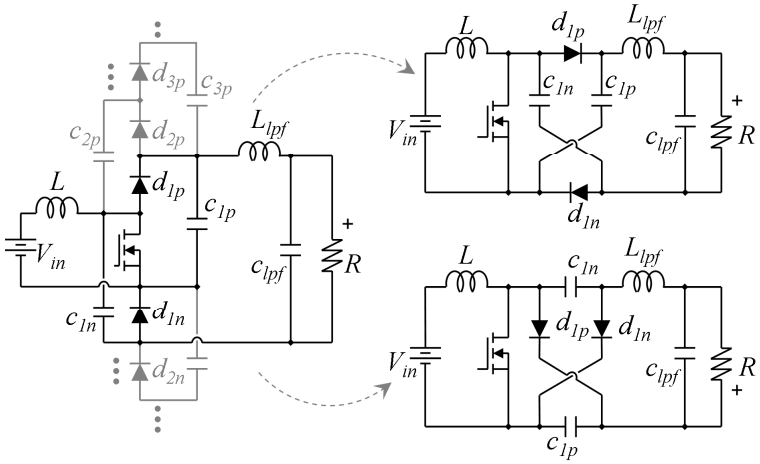

Fig. 3. Getting two of the topologies proposed in [3], it is important to remember that $V_{c1p} \approx V_{c2p} \approx V_{c3p} \ldots$ and $V_{c1p} \approx V_{c1n} \approx V_{c2n} \approx V_{c3n} \ldots$

Since the output voltage would be Vc_{1p} plus the average voltage in d_{1n}, which is give by (3), the voltage in the output is expressed as:

$$V_{out2} = V_{c1p} + \langle v_{d1n} \rangle = \left(\frac{1}{1-D} + \frac{D}{1-D} \right) V_{in} = \frac{1+D}{1-D} V_{in} \tag{6}$$

Equation (6) is consistent with [2], note that the converter in Fig. 2 (c) which hasn't being published has a higher voltage gain than both converters shown in Fig. 3 with the same number of components rated to the same parameters.
(iv) Another example is: if we select only d_{1n} and c_{1n}, see Fig. 4, and by connecting the load in d_{1n} (with the low-pass filter since the load would not be connected among a series of capacitors) the traditional Cuk converter can be derived. As expected the load voltage would be given by (3) since that is the average voltage in all diodes which switch complementary with the transistor, as d_{1n} which is an odd-numbered negative diode.

It is important to notice that the way of connecting the low-pass filter, with the inductor in the cathode or in the anode of the diode affects neither the operation nor the output voltage.
(v-vi) If more negative diodes are selected (keeping the odd number) a multiplier extension of the Cuk converter can be obtained as published in [6]. And the rules described here can be used to get a straight forward expression of the voltage gain.

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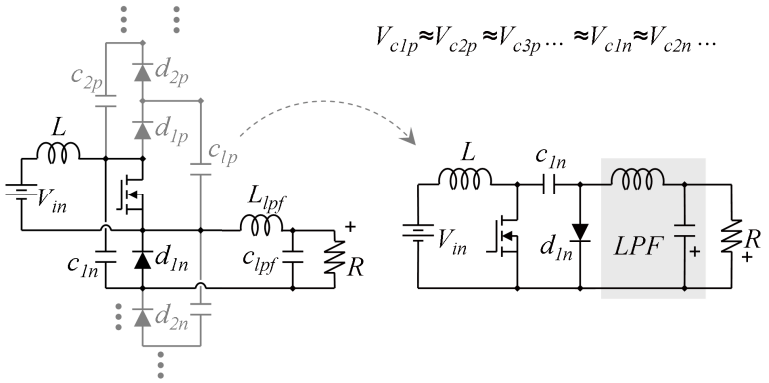

Fig. 4. Getting the Cuk converter.

(vii-ix) When a multiplier converter is derived from the generalized topology, it can be selected to use or not to use the output low-pass filter; not using the LPF saves one inductor which is desirable. If a pair-number of diodes is selected in the negative side of the generalized topology, the low pass filter can be avoided as shown in Fig. 5, which results in a circuit that have been proposed in converters published in [2, 4] and [5].

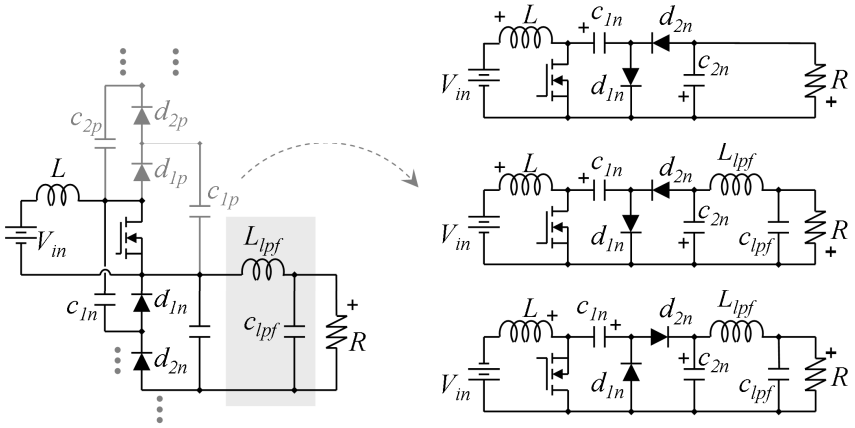

Fig. 5. Converters proposed [2, 4] and [5], it is important to remember that $V_{c1p} \approx V_{c2p} \approx V_{c3p} \ldots$ and $V_{c1p} \approx V_{c1n} \approx V_{c2n} \approx V_{c3n} \cdots$

5 Conclusion

This letter presents a generalized topology from which several of the state of the art and new topologies may be derived. It is shown how nine converters can be derived from this topology and a simple procedure to calculate the voltage gain in an easy and fast manner, consistent with the gain published individually in each converter.

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