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A 2.4 GHz to 3.86 GHz digitally controlled oscillator with 18.5 kHz frequency resolution using single PMOS varactor

Yangyang Niu, Wei Li[a)], Ning Li, and Junyan Ren

State Key Laboratory of ASIC & System, Fudan University,
825 Zhangheng Road, Shanghai 201203, China

a) *w-li@fudan.edu.cn*

Abstract: A novel varactor using single PMOS is proposed. By utilizing the capacitance difference between saturation and linear region, the proposed varactor can improve frequency resolution of a LC-tank based digitally controlled oscillator without introducing extra fixed loading capacitance. A digitally controlled oscillator with the proposed varactor is designed using 0.13 μm CMOS technology for verification. Measurement results show that the minimum frequency resolution is achieved around 18.5 kHz in a frequency range of 2.4 GHz to 3.86 GHz, indicating the minimum achievable capacitance step of 30 aF. The measured phase noise is −120.6 dBc/Hz at 1 MHz offset for 3.05 GHz carrier. The power consumption is 2.9 mW.

Keywords: varactor, digitally controlled oscillator, all-digital phase-locked loop

Classification: Integrated circuits

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1 Introduction

All-digital phase-locked loop (ADPLL) has drawn much attention due to its flexibility and compatibility with scaling of CMOS technology. Digitally controlled oscillator (DCO) is a crucial module in ADPLL. However, because of its finite frequency resolution, quantization noise introduced by DCO may degrade the performance of ADPLL.

In order to achieve better frequency resolution, pioneering recent works have demonstrated numerous schemes of varactor. Capacitance resolution can be improved by incrementally sizing varactor units [1], but this method requires a complicated design on device size. Another novel varactor exploits the fact that capacitance of PMOS varactor in inversion mode changes slightly from that of accumulation mode [2]. Traditional inversion-mode varactor unit is composed of one MOSFET, therefore the fixed loading capacitance is the gate capacitance of one MOSFET. The varactor unit using the above technique [2] consists of two MOSFETs, thus the fixed loading capacitance is the gate capacitance of two MOSFETs, which will restrict its application in high frequency DCOs. Additionally, bulk-controlled PMOS varactor [3, 4] can also realize high frequency resolution, but it is sensitive to control voltage.

In this paper, a novel varactor using single PMOS is proposed, which is as concise as inversion-mode varactor. The varactor utilizes the capacitance difference of one PMOS between the saturation and linear region. The goal of this work is to realize finer frequency resolution without an extra fixed capacitance.

2 Proposed varactor

Tracking bank or fine tuning bank in LC DCO is usually unit-weighted to reduce mismatch. A simplified capacitor tuning bank utilizing the proposed varactor is shown in Fig. 1. A proposed varactor unit consists of one PMOS, with its source and body tied to power supply. The tuning voltage V_{TUNE} is applied to the drain. The varactors in the bank are unit-weighted, and each varactor is controlled by a digital bit $(d_0, d_1, \ldots, d_n)$.

By taking the minimum-sized PMOS in the 0.13 μm CMOS technology with $V_{DD} = 1.2$ V, the C-V characteristic of the proposed varactor is illustrated in Fig. 2.

The principle of the proposed varactor is to employ the capacitance difference of single PMOS between the saturation and linear region. In Region I, when the tuning voltage is 1.2 V, the PMOS varactor works in linear region,

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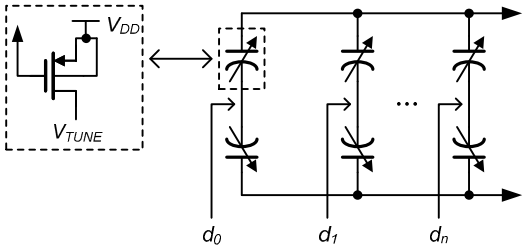

Fig. 1. A simplified fine tuning bank using the proposed varactor.

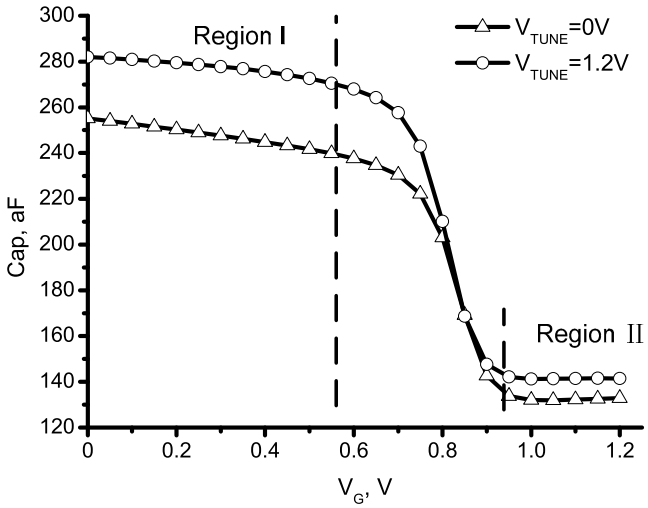

Fig. 2. The C-V characteristic of the proposed varactor.

and its capacitance can be expressed as follows [5]:

$$C_{high\_linear} = W \times L \times C_{ox} + 2 \times W \times C_{ov} \tag{1}$$

Where W and L are gate width and length of the PMOS varactor respectively, C_{ox} represents the gate oxide capacitance per unit area, and C_{ov} stands for the overlap capacitance per unit width. Also in Region I, when the tuning voltage is zero, the PMOS varactor works in saturation region, and its capacitance can be denoted as follows [5]:

$$C_{high\_satu} = \frac{2}{3} \times (W \times L \times C_{ox}) + 2 \times W \times C_{ov} \tag{2}$$

In this region, the varactor works as transistor, and its channel noise current can be expressed as:

$$\overline{I_n^2} = 4kT\gamma g_m \tag{3}$$

It should be noted that in the implemented DCO, the varactor power supply is V_{DDC}, which is not the DCO supply V_{DDA}, as illustrated in Fig. 3. The varactor channel noise current flows only through the varactor supply V_{DDC}. Therefore, there is little noise contribution to the DCO phase noise.

In Region II, the PMOS varactor is in depletion mode, and its capacitance remains low. Therefore, the capacitance step ΔC of the proposed varactor can be derived from Eq. (1) and Eq. (2), which is approximately:

$$\Delta C = \frac{1}{3} \times (W \times L \times C_{ox}) \tag{4}$$

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Obviously, it is much smaller than that of conventional inversion-mode MOS varactor. Furthermore, because the proposed varactor unit consists of only one PMOS, its fixed loading capacitance remains the same as that in a conventional inversion-mode PMOS varactor. No extra fixed loading capacitance is introduced.

3 The DCO architecture

In order to verify the proposed varactor, a digitally controlled oscillator applying the proposed varactor is designed in 0.13 μm CMOS technology. As shown in Fig. 3, it consists of a cross-coupled NMOS and PMOS pair, a current bias, and a 2.2 nH inductor. Besides, four capacitor tuning banks are included: a binary-weighted coarse tuning bank using switched MIM capacitors; a binary-weighted moderate tuning bank using conventional inversion-mode PMOS (I-PMOS) varactors; a unit-weighted fine tuning bank employing minimum-sized inversion-mode PMOS varactors; and a unit-weighted capacitor tuning bank employing proposed varactors. Both the coarse, the moderate and the fine banks are used to extend the total tuning range, while the proposed varactor bank are designed to improve frequency resolution.

4 Experimental results

This DCO is fabricated in TSMC 0.13 μm CMOS technology. The die photo of the designed DCO is shown in Fig. 4, with core area of 0.4 mm^2. The DCO covers a frequency range from 2.4 GHz to 3.86 GHz. The power consumption is 2.9 mW.

Measurement results of frequency resolution achieved by both the minimum-sized I-PMOS varactor in the fine tuning bank and the proposed varactor at

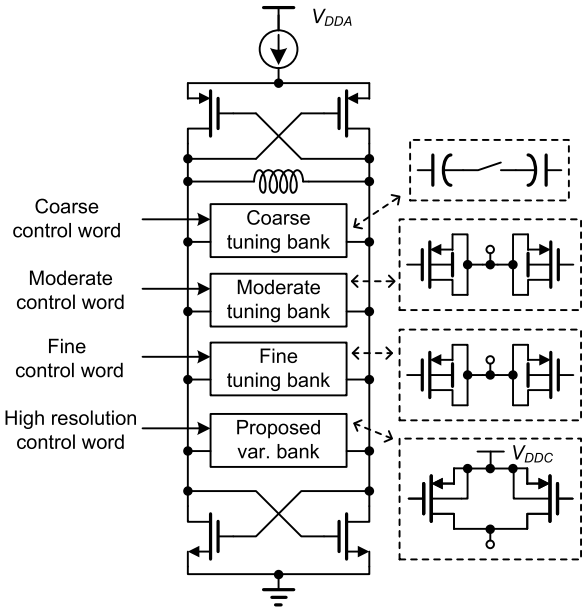

Fig. 3. DCO architecture with coarse, moderate, fine capacitor tuning banks and proposed varactor bank.

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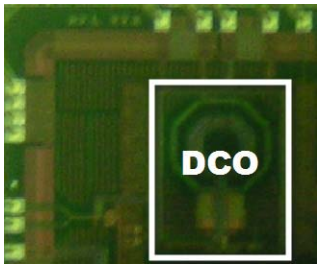
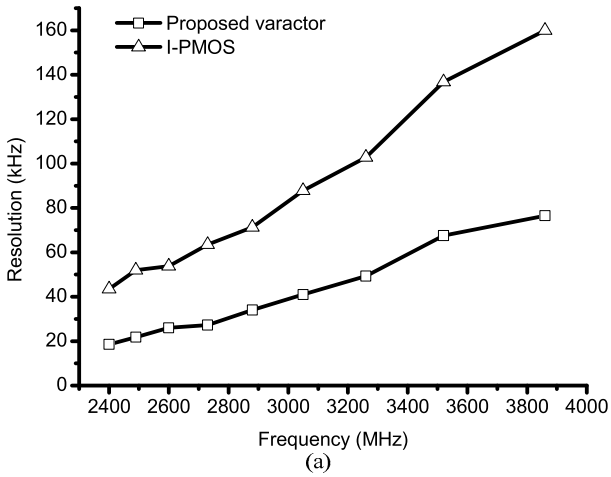
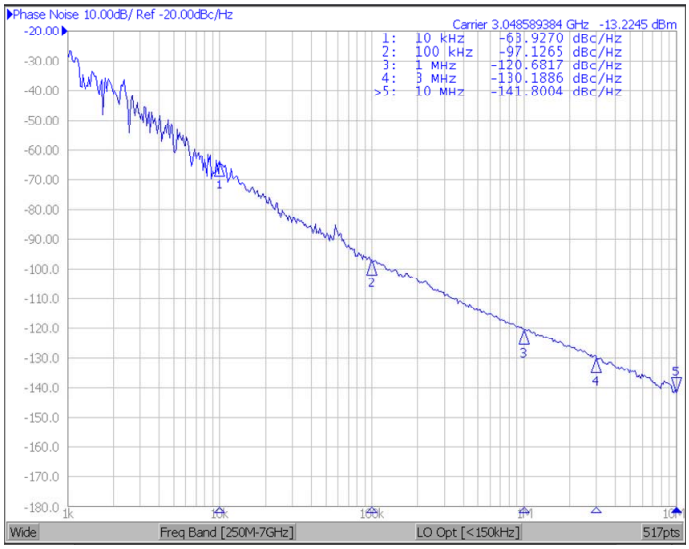


Fig. 4. The die photo of the DCO.



(a)



(b)

Fig. 5. (a) Measured frequency resolution; (b) Measured phase noise of the DCO.

various output frequencies are depicted in Fig. 5 (a). The proposed varactor can improve frequency resolution by more than 50%, compared with the minimum-sized I-PMOS varactor. The measured phase noise result is shown in Fig. 5 (b) when the tuning voltage is 0, and gate bias is 0.5 V. The phase noise is −120.6 dBc/Hz at 1 MHz offset for 3.05 GHz carrier.

By employing the proposed varactor, the measured minimum frequency resolution is achieved at about 18.5 kHz ($f_{res,avg}$) around 2.4 GHz (f_1) output,

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Table I. Performance comparison with the recent works.

Reference	[1]07	[2]09	[3]10	[4]11	This work
Process (nm)	90	180	90	180	130
Supply (V)	1.2	1.8	1.2	1.8	1.2
Results	Meas.	Meas.	Meas.	Meas.	Meas.
Fine varactor unit	Increment-ally sized	2 PMOS	Bulk controlled	Bulk controlled	1 PMOS
Center freq. (GHz)	3.35	6	35.56	0.3	3.13
Tuning range (MHz)	600	600	1100	300	1460
Min. freq. resolution (kHz)	5	90	230/60	N/A	18.5
Min. ΔC (aF)	10	28	40/10	70	30
Norm. ΔC (aF)	10	1.62	40/10	4.05	2.35
Varactor unit C_{fix} (aF)*	N/A	1286	N/A	1375	211.7
Norm. C_{fix} (aF)	N/A	74.38	N/A	79.52	16.56
Phase noise (dBc/Hz)	-118 @1M	-117 @1M	-99.67 @10M	44ps#	-120.6 @1M
	3.06GHz	5.9GHz	35.56GHz	450MHz	3.05GHz
Power (mW)	2.4 (DCO)	9.2 (DCO)	44 (PLL)	9.6-16.2 (PLL)	2.9 (DCO)

*: C_{fix}= (C_{high}+C_{low})/2. #: Peak-to-peak jitter.

implying that the minimum capacitance step (ΔC) is about 30 aF, which is calculated by the following equation:

$$\Delta C = \frac{1}{4\pi^2 L}\left(\frac{1}{f_1^2} - \frac{1}{(f_1 + f_{res,avg})^2}\right) \tag{5}$$

Where 2.2 nH PDK inductor value is adopted. Generally, the ΔC in Fig. 2 is defined as the difference between the equivalent capacitance for $V_{TUNE} = 0$ and $V_{TUNE} = 1.2$ V, depending on the output DC bias and the amplitude of the oscillator. The estimated minimum ΔC in Fig. 2 in this design is about 25 aF. It is worth noting that the real ΔC (30 aF) is not the same as the estimated one (25 aF). Actually, such difference comes from the deviation of the real inductor value in the tuning tank from the PDK value, mainly caused by the chip manufacturing.

A smaller DCO frequency resolution will make a lower reference spurs level of PLL. Based on symmetric rectangular modulating signal and narrow-band frequency modulation analysis [6], the spur level for nth harmonic of the PLL is:

$$P_{spur} = 20\log\left(\frac{1}{2n}\cdot\frac{\pi f_{res}}{\omega_m}\cdot \sin c\left(\frac{n\pi}{2}\right)\right) \tag{6}$$

Where f_{res} is the DCO frequency resolution, ω_m is the modulating frequency. For reference spur analysis, ω_m equals to the reference frequency. Eq. (6) shows that the spur level power is lower as frequency resolution becomes finer.

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Table II. Capacitance of MOSFET in various processes [7].

Process	NMOS			PMOS		
	C_{on}	C_{off}	ΔC	C_{on}	C_{off}	ΔC
65nm	200aF	104aF	96aF	183aF	94aF	89aF
90nm	253aF	143aF	110aF	266aF	159aF	107aF
130nm	3.7fF	2.0fF	1.7fF	3.4fF	1.6fF	1.8fF
180nm	4.2fF	2.2fF	2.0fF	4.6fF	2.5fF	2.1fF

Fortunately, the proposed varactor can realize finer frequency resolution, thus decreasing the spur level.

Performance comparison is listed in Table I. In order to decline the contributions of process disparity, the normalized capacitance steps (Norm. ΔC) in 90 nm CMOS technology for [1, 2, 3, 4] and the proposed work are estimated. The capacitances of MOSFET in various processes are obtained from Table II [7]. First, the scaling factors are denoted by "quotients of $C_{on,PMOS}$ in various process divided by $C_{on,PMOS}$ in 90 nm process", and then the normalized capacitance step equals to "scaling factor dividing capacitance steps (ΔC)". Normalized fixed loading capacitance (Norm. C_{fix}) is calculated in a similar way.

5 Conclusion

A novel varactor employing the difference between the saturation and linear region capacitance of a single PMOS is proposed, in order to realize high frequency resolution without introducing extra fixed loading capacitance. A DCO prototype using the proposed varactor is designed and fabricated in 0.13 μm CMOS technology for verification. Measurement results show that the minimum frequency resolution is achieved at 18.5 kHz in a frequency range of 2.4 GHz to 3.86 GHz, implying a minimum capacitance step of 30 aF. The power consumption is 2.9 mW. The measured phase noise is -120.6 dBc/Hz at 1 MHz offset for 3.05 GHz carrier.

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