IEICE Electronics Express, Vol.5, No.22, 967–972

Low power and low voltage chopper amplifier without LPF

Yoshihiro Masui[a)], **Takeshi Yoshida, and Atsushi Iwata**

Graduate School of Advanced Sciences of Matter, Hiroshima University, 1–3–1 Kagamiyama, Higashihiroshima, Hiroshima 739–8530, Japan

a) *masui@dsl.hiroshima-u.ac.jp*

Abstract: A mobile sensor system for very low level biological signals such as neuron spikes is required to implement with a scaled CMOS technology. For a key circuit of these systems, a chopper amplifier (CA) which suppresses DC offset and 1/f noise of MOS devices is widely used. However, the conventional CA consumes large power because it requires a wide-band amplifier exceed a chopping frequency and a post Low Pass Filter (LPF) for eliminating modulation noise. In this paper, a new CA architecture for reducing power consumption is presented. In the architecture, the demodulator is placed at the input of 2nd stage amplifier and the 2nd stage has a narrow band determined with a 1st pole. Moreover the post LPF is not required. The proposed CA was designed and simulated with a 0.18 μm CMOS process and a 1.2 V supply. When the ratio of chopping frequency and signal band width is set to 100 (= 10 kHz/100 Hz), the power consumption of the CA is reduced to 1/88 (= 7 μW/616 μW) compared with the conventional CA.

Keywords: flicker noise, chopper AMP, low-power, low-noise

Classification: Integrated circuits

References

[1] T. Yoshida et al., "A design of neural signal sensing LSI with multi-input-channels," *IEICE Trans. Fundamentals*, vol. E87-A, no. 2, pp. 376–383, Feb. 2004.

[2] K. D. Wise, "Wireless implantable microsystems coming breakthroughs in health care," *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 106–109, June 2002.

[3] T. Yoshida et al., "A 1 V Supply 50 nV/$\sqrt{\text{Hz}}$ Noise PSD CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization," *Symposium on VLSI Circuits*, pp. 118–121, June 2005.

[4] M. A. T. Sanduleanu et al., "Low-Power Low-Voltage Chopped Amplifier with a New Class AB Output Stage for Mixed Level Applications," *ProRISC Workshop on Circuits, Systems and Signal Processing, Proceedings*, 1997.

DOI: 10.1587/elex.5.967
Received October 07, 2008
Accepted October 20, 2008
Published November 25, 2008

IEICE Electronics Express, Vol.5, No.22, 967–972

1 Introduction

Recently, biological information sensing systems using mixed-signal CMOS technology have been utilized for various medical purposes such as a healthcare, a medical care and a study of biological neural networks [1, 2]. Especially, an electroencephalogram (EEG), an electrocardiogram (ECG) and a neural signal datum are important information in medical science and biology. The biological information sensing systems need to observe these small level signals for a long term. Therefore it is necessary to realize a low noise characteristic, low power consumption and low voltage operation [3]. A low-noise amplifier is one of the key circuits for detecting the small level signals in the biological information sensing chip. In CMOS technologies, 1/f noise becomes a serious problem. A chopper amplifier (CA) which can reduce 1/f noise is widely used. However, the conventional CA is not low power consumption. In general, a cutoff frequency of amplifier is designed to the signal bandwidth. On the other hand, the amplifier which composes the conventional CA needs cutoff frequency which is higher than a chopping frequency (f_{chop}). The f_{chop} is set to more than 10 times larger the signal band width. Thus the conventional CA consumes large power.

A cascode CA that has low power consumption was proposed [4]. However, the cascode CA is not suitable for low supply voltage operation, because it degrades the output voltage range. Therefore, a new chopper amplifier with low power and wide output voltage range is demanded for the mobile sensing system.

2 Chopper Stabilization Principle

The principle of the conventional chopper stabilization technique is illustrated in Fig. 1. In the modulator operated by the chopping frequency (fchop), the input signal is converted to around the fchop which is higher than the 1/f noise corner frequency of the amplifier as shown in Fig. 1 (b). Then the modulated signal is converted back to the base band after amplification in the demodulator, the dc offset voltage (V_{off}) and 1/f noise (V_{fn}) of the amplifier are converted to around the fchop as shown in Fig. 1 (c). Since V_{off} and 1/f noise are suppressed by LPF, the CA can provide a high SNR output signal.

A disadvantage of the conventional CA is large power consumption. For precise operation of the circuit, the amplifier needs a higher cutoff frequency than f_{chop} as shown in Fig. 1 (d). The f_{chop} is decided by the 1/f corner frequency and cutoff characteristics of the LPF. Since the conventional CA generates large power of the chopping noise as shown in Fig. 1 (c), the noise power must be suppressed by increase of f_{chop} or the LPF order. However the both ways increase power consumption.

The cascode CA is shown in Fig. 1 (f). The demodulators are placed at low impedance nodes. The cascode circuit which utilizes low impedance nodes can modulate input signal to high frequency band without extra power. In addition, cascode transistors provide low-pass filtering for the large modulated noise coming from chopping. However the cascode CA has small output

DOI: 10.1587/elex.5.967
Received October 07, 2008
Accepted October 20, 2008
Published November 25, 2008

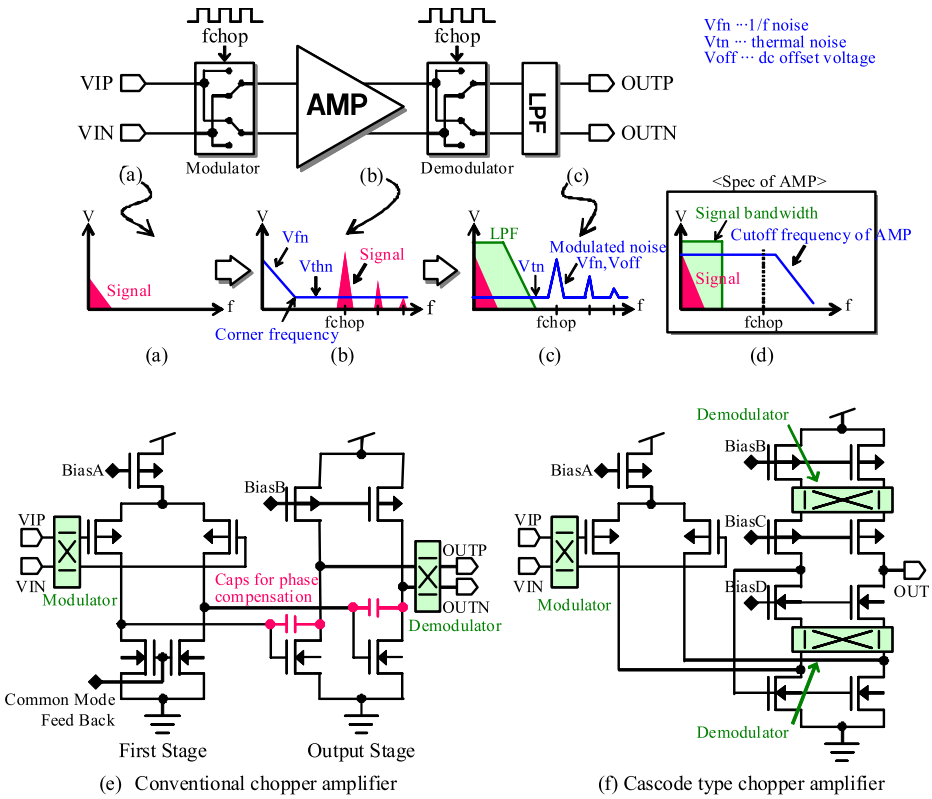


Fig. 1. Principal of the conventional chopper stabilization technique

voltage range. For example, when the over-drive voltage is set to 200 mV, the output voltage range of cascade CA is reduced 400 mV narrower than that of a conventional CA. This voltage range degradation causes the 6 dB loss of signal-to-noise ratio (SNR) at 1.2 V supply voltage. If an extra output buffer is added which recovers small output range, power consumption is increased. Thus the cascode CA is not applicable to low supply voltage systems. A new circuit architecture of low voltage and low power CA is necessary for battery operated mobile or wireless sensing systems.

3 Proposed Circuit

Figure 2 shows a circuit schematic of the proposed CA. It consists of a two-stage opamp and a modulator and a demodulator. The notable features of the circuit are a position of the demodulator and pole configuration of 2-stage amplifier. In this architecture, a dominant pole (P_1) is placed at the 2nd stage and a 2nd pole (P_2) is placed at 1st stage as shown in Fig. 2 (a). To ensure the phase margin of the amplifier, the cutoff frequency (f_c) of 1st stage is designed to be higher than the gain crossover frequency of the amplifier.

In the conventional CA, the modulated signals are demodulated at output of the CA. On the other hand, the proposed CA demodulates signals before the 2nd stage. Thus the cutoff frequency (fc) of the 2nd stage can be designed lower than the fchop as shown in Fig. 2 (b). In addition, phase compensation capacitor (C) works as a narrow band 1st-order LPF, and the CA does not

DOI: 10.1587/elex.5.967
Received October 07, 2008
Accepted October 20, 2008
Published November 25, 2008

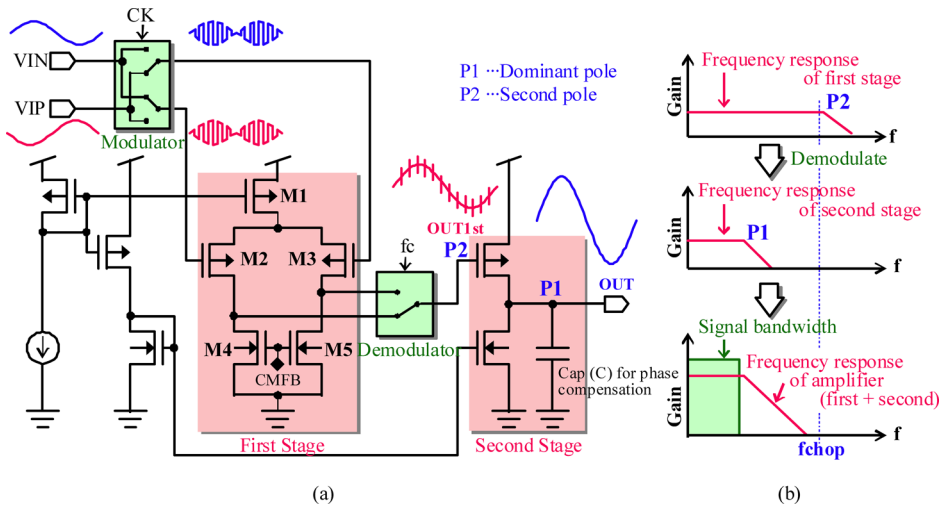


Fig. 2. Principle of proposed chopper amplifier (a) Proposed chopper amplifier (b) Frequency response of each stage

need an post LPF. From the above-mentioned, the power of CA dissipation can be drastically reduced.

The input referred noise ($V_{n,in}$) of the proposed CA is given by

$$V_{n,in} = V_{tn1} + (V_{fn2} + V_{tn2})/A_1 \tag{1}$$

where V_{tn1} and V_{tn2} are the thermal noise of the first stage and the second stage, respectively. V_{fn2} is 1/f noise of the second stage and A_1 is the first stage gain. The V_{tn1} is dominant because A_1 is as high as 30 dB. V_{tn1} can be decreased by raising the bias current. Therefore, the proposed CA can minimize the $V_{n,in}$ by increasing the gain and current of the first stage.

A disadvantage of the conventional CA is that a post LPF is needed to reject large modulation noise at the chopping frequency. The proposed CA removes modulated noise by the narrow bandwidth 2nd stage which works as a 1st-order LPF. A reduction ratio of modulated noise (K_{noise}) depends on a ratio of fchop and first pole frequency (f_{p1}), and given by

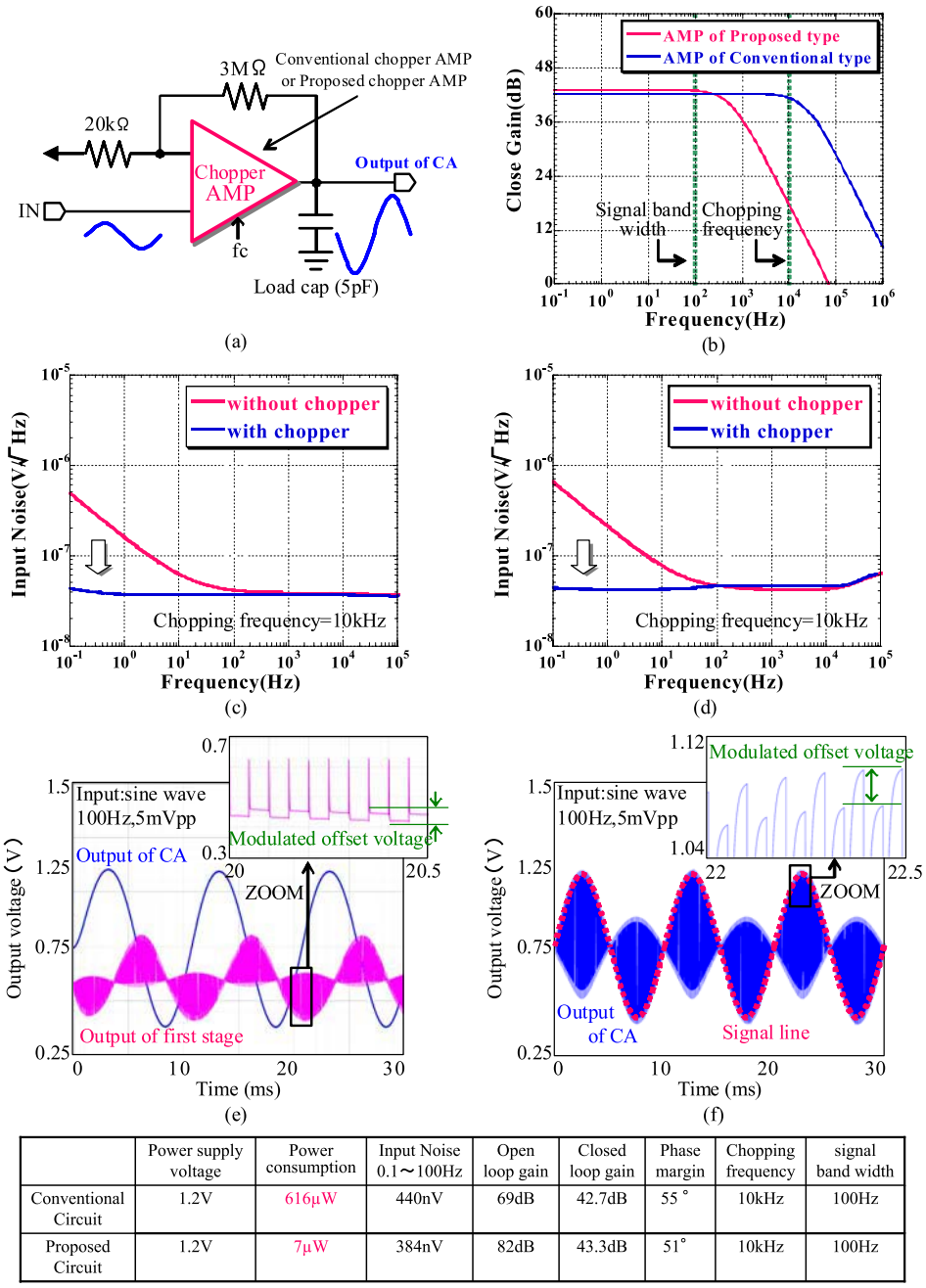
$$K_{noise}(dB) = -20\log_{10}(fchop/f_{p1}) \tag{2}$$

The proposed CA needs large load capacitance for phase compensation. Therefore, the CA is suitable for the combination with ADC which has a large input capacitance such as successive approximation ADC.

4 Simulation results

The conventional CA and the proposed CA were designed and simulated with a 0.18 μm CMOS technology. Figure 3 shows simulation results. The proposed CA has 82 dB open loop gain, 7 μW power consumption and 384 nV input referred noise (0.1-100 Hz) at 1.2 V supply voltage and 10 kHz chopping frequency. The conventional CA has 69 dB open loop gain, 616 μW power consumption and 440 nV input referred noise (0.1-100 Hz) at 1.2 V supply

DOI: 10.1587/elex.5.967
Received October 07, 2008
Accepted October 20, 2008
Published November 25, 2008



	Power supply voltage	Power consumption	Input Noise 0.1～100Hz	Open loop gain	Closed loop gain	Phase margin	Chopping frequency	signal band width
Conventional Circuit	1.2V	616μW	440nV	69dB	42.7dB	55 °	10kHz	100Hz
Proposed Circuit	1.2V	7μW	384nV	82dB	43.3dB	51°	10kHz	100Hz

(g)

Fig. 3. Simulation results (a) Test circuit (b) Frequency response of AMP (c) Noise characteristic of proposed chopper AMP (d) Noise characteristic of conventional chopper AMP (e) Output waves of proposed chopper AMP (f) Output waves of conventional chopper AMP (g) Performance summary

voltage and 10 kHz chopping. Both CAs were simulated with a test circuit configuration as shown in Fig. 3 (a).

Both CAs have 100 Hz signal band width. However the cutoff frequency (fc) of amplifiers which compose CAs is different as shown in Fig. 3 (b). The f_c of conventional AMP is 20 kHz. It is higher than the fchop (10 kHz) as

DOI: 10.1587/elex.5.967
Received October 07, 2008
Accepted October 20, 2008
Published November 25, 2008

discussed in chapter 2. On the other hand, the f_c of the 2nd stage is 500 Hz. It is considerably lower than the f_{chop}. As a result, the power consumption of the proposed CA is drastically reduced. The simulations reveal that the power consumption of proposed CA is 1/88 (= 7 uW/616 uW) compared with the conventional CA when the ratio of f_{chop} and signal bandwidth is set to 100 (= 10 kHz/100 Hz). The effect of noise reduction is almost equal to two kinds of CA as shown in Fig. 3 (c) (d). In addition, the proposed CA does not need LPF which clean up modulated noise. Fig. 3 (e) and (f) show simulation results when offset voltage of AMP is added. The input referred offset voltage is 100 uV. In the proposed CA, the offset is suppressed by through the 2nd stage which works as LPF as shown Fig. 3 (e). On the other hand, the output of conventional CA has large modulated noise as shown in Fig. 3 (f).

5 Conclusion

New Chopper Amplifier (CA) architecture is presented for biological sensing systems. The CA has achieved both large output voltage range like the conventional CA and low power consumption like the cascode CA by devising pole position and the demodulator position. In addition, the proposed CA does not need extra LPF. The CA was designed and simulated with a 0.18 μm CMOS process, and achieved 82 dB open loop gain, 7 μW power consumption and 384 nV input referred noise (0.1-100 Hz) at 1.2 V supply voltage and 10 kHz chopping. The CA improved the power consumption with the effect of noise reduction kept. When the ratio of chopping frequency and signal band width is set to 100 (= 10 kHz/100 Hz), the power consumption of proposed CA is 1/88 (= 7 μW/616 μW) compared with the conventional CA.

Acknowledgments

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

DOI: 10.1587/elex.5.967
Received October 07, 2008
Accepted October 20, 2008
Published November 25, 2008