

A CMOS 4.6 ppm/°C curvature-compensated bandgap voltage reference

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Abstract: A novel high precision high order curvature-compensated bandgap reference (BGR) is presented in this paper designed using the subthreshold current of self-cascode transistors in standard digital 0.18 μm CMOS process. Simultaneously its temperature coefficient is typically 4.6 ppm/°C in the temperature range of -25 to 120°C with a supply current of $17.25 \mu\text{A}$. A power supply rejection ratio (PSRR) of -51 dB is achieved while the layout area is no more than 0.0022 mm^2 .

Keywords: CMOS, voltage reference, subthreshold, high-order curvature -compensation, high PSRR, self-cascode transistor

Classification: Integrated circuits

References

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1 Introduction

Bandgap voltage reference (BGR) is a building block in various mixed-signal and radio frequency circuits, such as Data converter, switching power supplies, class-D audio amplifiers, DRAMs and so on [1, 2, 3, 4, 5].

Employed in the analog blocks in SOC's, the voltage reference circuits must be amenable to standard digital CMOS process, since the characterized vertical or lateral parasitic bipolar transistors may not be available or reliable, therefore, p-channel transistors acting as diodes are used.

Also, the reference must generate an accurate output voltage (V_{ref}), which is almost independent of supply, temperature variations, and process. Besides, low voltage and low power are two important design criteria in all systems, especially in battery-operated products. As a step toward low voltage and low power, a reference circuit is developed which can operate with an ultra-low current in the subthreshold region of MOSFET [2]. Unfortunately, the subthreshold region of MOSFET circuits commonly employs high values of resistors, while the application of polysilicon resistors not only increases the area and cost but also worsens the coupling effect of the substrate noise, so some structures without using resistors have been proposed [4].

This paper presents a high-order curvature-compensated bandgap reference with a TC of 4.6 ppm/°C using only one resistor. In contrast to [1, 2, 3, 5], our design has higher precision and PSRR.

2 Principle of proposed BGR

The traditional BGRs (first order Curvature-Compensated) get V_{ref} by

$$V_{ref} = V_{BE} + K'(V_T \ln(n)) \quad (1)$$

Where V_{BE} is diode voltage, K' is the coefficient of the Proportional to Absolute Temperature (PTAT) voltage.

Due to first-order temperature compensated architecture, the temperature coefficient of traditional reference is commonly limited between 20 and 100 ppm/°C [5], such as reference [2]. The principle of our voltage reference circuit is illustrated in Fig. 1 (a). In response to the higher order temperature characteristics of V_{BE} , selecting -5°C and 50°C as two zero points, the second-order compensation is achieved, then with the technique of subsection compensation, the third-order compensation is implemented, while the temperature coefficient is greatly improved.

2.1 Principle of second order curvature-compensation circuit

The circuit consists of a current source subcircuit, self-cascode composite transistors, high-order curvature-compensated circuits and a Wilson current mirror.

The current source subcircuit is β multiplier self-biasing circuit that uses a MOS resistor R_{Mn} instead of ordinary resistor. Generating an I_{BIAS} of 750 nA, R_{Mn} is operated in strong-inversion, deep-triode region [2].

Mp10 acts as PN diodes (V_{BE}), whose gate, source, and drain are connected together. The gate-bulk voltage of this transistor has a temperature coefficient of $\sim -1.69 \text{ mV}/^\circ\text{C}$ [3]. Accurate equations of V_{BE} are developed from

$$V_{BE}(T) = V_G(T) - \left(\frac{T}{T_0}\right) V_G(T_0) + \left(\frac{T}{T_0}\right) V_{BE}(T_0) + \frac{kT}{q} \ln \left[4 \left(\frac{T}{T_0}\right) \frac{\bar{\mu}(T_0)}{\bar{\mu}(T)} \frac{I_C(T)}{I_C(T_0)} \right] \quad (2)$$

$$\bar{\mu}(T) = \frac{q\bar{D}(T)}{kT} \quad (3)$$

Where $V_G(T)$ is the bandgap voltage at temperature T , T_0 a “reference” temperature (often, not necessarily, room temperature), $D(T)$ the “effective” minority carrier diffusion constant in the base [6]. With coefficients in (2) replaced by parameters a_0 , a_1 , and a_2 , equation (2) can be rewritten as

$$V_{BE} = a_0 - a_1T - a_2T \ln T \quad (4)$$

Without BJTs, we get a PTAT voltage through the difference of gate-source voltage of two MOS transistors ($\Delta V_{GS} = V_{GS1} - V_{GS2}$) operating in weak inversion mode (subthreshold region) resulting in the negative temperature coefficient of V_{GS} working in subthreshold region. So we can generate V_T as similarly one can do by means of vertical or lateral parasitic BJTs. Generating ΔV_{GS} with a self-cascode composite transistor (subthreshold region) is shown in Fig. 1 (b). V_{DS2} is equal to ΔV_{GS} [2].

$$\Delta V_{GS} = V_{DS2} = n \cdot V_T \cdot \ln [S_1 \cdot I_{D2} / S_2 \cdot I_{D1}] \quad (5)$$

With PN diodes (V_{BE}) and ΔV_{GS} one can generate V_{ref} similarly to the traditional BGR as shown in Fig. 1 (a)

$$V_{ref} = V_{GB10} + V_{DS5} + V_{DS7} + V_{DS9} \quad (6)$$

According to (4) (5) and (6), (6) can be rewritten as

$$V_{ref} = a_0 - a_1T - a_2T \ln T + n \cdot V_T \cdot \ln \cdot \left[\frac{S_{n4} \cdot S_{n6} \cdot S_{n8} \cdot (S_{p4} + S_{p5} + S_{p6} + S_{p7}) \cdot (S_{p5} + S_{p6} + S_{p7}) \cdot (S_{p6} + S_{p7})}{S_{p4} \cdot S_{p5} \cdot S_{p6} \cdot S_{n5} \cdot S_{n7} \cdot S_{n9}} \right] \quad (7)$$

With third order Taylor series expansion of $T \ln T$, we find

$$\frac{\partial V_{ref}}{\partial T} = a_2 \frac{1}{2T_0^2} T^2 - a_2 \frac{2}{T_0} T + \left(\frac{3}{2} a_2 - a_2 \ln(T_0) - a_2 + c - a_1 \right) = 0 \quad (8)$$

Where c is equal to

$$n \cdot \frac{\partial V_T}{\partial T} \cdot \ln \left[\frac{S_{n4} \cdot S_{n6} \cdot S_{n8} \cdot (S_{p4} + S_{p5} + S_{p6} + S_{p7}) \cdot (S_{p5} + S_{p6} + S_{p7}) \cdot (S_{p6} + S_{p7})}{S_{p4} \cdot S_{p5} \cdot S_{p6} \cdot S_{n5} \cdot S_{n7} \cdot S_{n9}} \right]$$

Through (7) and (8) it is possible to verify that the temperature compensation of V_{ref} can be implemented by proper sizing of devices $Mp4 \sim Mp7$ and $Mn4 \sim Mn9$. The two roots of (8) T_1 and T_2 introduce two zero points forming the wave of V_{ref} , as shown in Fig. 2 (a), and size of transistors have been shown in Table I. We regulate T_1 and T_2 nearby the low temperature region (T_1 is about -5°C , T_2 about 50°C), which is propitious to the higher order curvature-compensate work.

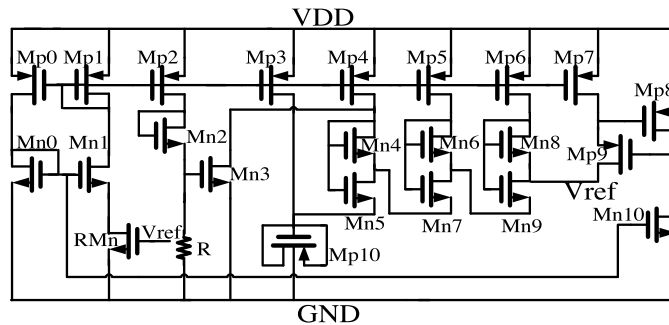
2.2 Principle of higher (third) order curvature-compensation circuit

$Mn3$ shown in Fig. 1 (a) is the third order curvature-compensation transistor, which only works in triode region while the temperature rises to a certain value by designing the gate voltage of $Mn3$ properly. That is to say, this temperature T_{3th} (this work is 100°C) is the initial temperature of third order compensation. The gate-source voltage of $Mn3$ is proportional to temperature. Meanwhile, assuming that the change of source-drain voltage versus temperature can be neglected, the current of $Mn3$ can be represented as

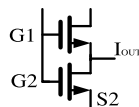
$$I_{Mn3} = \begin{cases} 0, & T < T_{3th} \\ I_D = I_O \cdot \exp\left(\frac{V_{gs}}{nV_T}\right), & \geq T_{3th} \end{cases} \quad (9)$$

With I_{Mn3} increasing, equation (5) and (8) can be rewritten as (10) and (11). Meanwhile, we find that (10) is a monotone increasing function. So TC of ΔV_{GS} in (5) increases, then we can get another zero point of the V_{ref} curve with temperature, as shown in Fig. 2 (b)

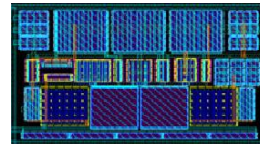
$$\Delta V_{GS} = V_{DS2} = n \cdot V_T \cdot \ln \left[\frac{S_1 \cdot (I_{D2} - I_{MN3})}{S_2 \cdot (I_{D1} - I_{MN3})} \right]$$



(a)



(b)



(c)

Fig. 1. (a) Proposed voltage reference architecture, (b) Structure of self-cascode composite transistor, (c) Layout of the proposed voltage reference circuit

$$= n \cdot V_T \cdot \ln \left[\frac{S_1 \cdot (I_{D1} + I_{OUT} - I_{MN3})}{S_2 \cdot (I_{D1} - I_{MN3})} \right] \quad (10)$$

$$\frac{\partial V_{ref}}{\partial T} = a_2 \frac{3}{T_0^2} T^2 - a_2 \frac{8}{T_0} T + (4a_2 - a_2 \ln(T_0) - a_1) + c(T) = 0 \quad (11)$$

Compared with (8), c in (11) is not constant but a function of T .

2.3 Output stage

Compared to references [1, 2, 3], the proposed circuits introduce a Wilson current mirror, consisting of Mp8 and Mn10, which is used for the increasing of PSRR, the simulation result is illustrated in Fig. 2 (e).

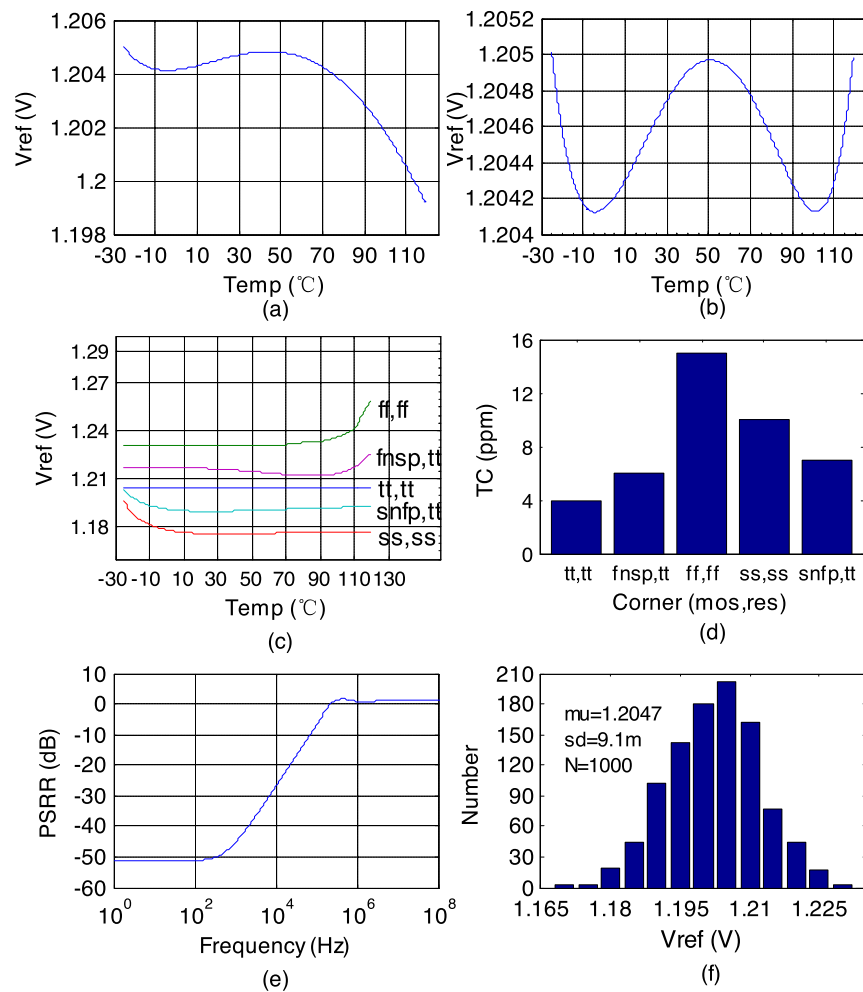


Fig. 2. (a) Second order compensated curve, (b) Higher-Order Curvature-Compensated Vref, (c) Output voltage (Vref) versus temperature for different process corner, (d) TC of Vref at different process corners, (e) PSRR versus frequency at room temperature, (f) Monte Carlo histogram of Vref (@27°C)[V]

Table I. Device size of this work

Device	Mp0	Mp1	Mp2	Mp3	Mp4	Mp5	Mp6	Mp7
Value(μ)	5/0.25	5/0.25	25/0.18	5/0.25	2.5/0.25	5/0.25	10.68/0.25	2.5/0.25
Device	R	Mn0	Mn1	Mn2	Mn3	Mn4/6/8	Mn5/7/9	
Value(μ)	2.3K Ω	5/5	5/5	2.5/1	15.5/0.18	50/0.25	5/0.25	

Table II. Comparison of reported CMOS voltage reference circuit

	This work	[1]	[2]	[3]	[5]
Process	0.18 μm	0.16 μm	0.35 μm	0.13 μm	0.5 μm
Temp range	-25~120 $^{\circ}\text{C}$	-40~135 $^{\circ}\text{C}$	-20~80 $^{\circ}\text{C}$	-40~85 $^{\circ}\text{C}$	-40~100 $^{\circ}\text{C}$
Vref	1.204V	0.944V	0.745V	1.473V	1.285V
Total current	17.25 μA	1.4 μA	2.4 μA	24.3 μA	25 μA
TC	4.6ppm/ $^{\circ}\text{C}$	30ppm/ $^{\circ}\text{C}$	15ppm/ $^{\circ}\text{C}$	25.3ppm/ $^{\circ}\text{C}$	7.2ppm/ $^{\circ}\text{C}$
PSRR	-51dB	-----	-45dB	-27 dB	-35~-69 dB
Chip area	0.0022mm ²	0.0025 mm ²	0.055 mm ²	0.01 mm ²	0.04 mm ²

3 Experimental results

This part shows all the simulation results of the circuit designed in SMIC 0.18 μm 1.8 V CMOS process. The DC voltage of the reference with temperature variations is shown in Fig. 2(b). At room temperature, the reference voltage is 1.204 V. And in the range of -25°C to 120°C , Vref varies 0.8 mV, with a TC of 4.6 ppm/ $^{\circ}\text{C}$.

Fig. 2(e) shows the plot of power supply rejection ratio versus frequency with a 1.8 V supply voltage. The proposed circuit achieves a -51 dB PSRR for frequencies below 1000 Hz.

Additionally, the circuit has been simulated at different process corners, as shown in Fig. 2(c) and Fig. 2(d). At room temperature, the worst temperature coefficient is 14.5 ppm/ $^{\circ}\text{C}$ at different process corners.

Finally, the Monte Carlo simulation is performed including mismatch and process variations. For one thousand samples, the mean value of Vref is 1.204 V and the standard deviation (σ) is 9.1 mV. This estimation of Vref represents for 2- σ requirement (99.2% of samples) a total variation of about ± 18.2 mV. Fig. 2(f) shows the histogram of Vref (@27 $^{\circ}\text{C}$). The layout is shown in Fig. 1(c)

Table II summarizes the characteristics of our circuit in comparison with its counterparts reported in [1, 2, 3, 5]. Our design is comparable to other circuits in power supply, PSRR, precision, and chip area.

4 Conclusions

A low-voltage low-power dissipation high-order curvature-compensated CMOS voltage reference consisting of subthreshold MOSFET circuits has been proposed and implemented in standard digital 0.18 μm CMOS process. Without using BJTs and employing only one resistor, the active chip area

is no more than $50 \times 36 \mu\text{m}^2$. The simulation results show that our design achieves typically a temperature performance of 4.6 ppm/°C in the range of -25 to 120°C with a power supply rejection ratio of the voltage reference of -51 dB. The supply current is about $17.25 \mu\text{A}$. It is adaptive for low-power devices such as mobile devices, implantable medical devices, and smart sensor networks.

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