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A 250 KS/s, 0.8 V ultra low power successive approximation register ADC using a Dynamic rail-to-rail comparator

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Abstract: A low voltage low power successive approximation register (SAR) analog-to-digital converter (ADC) based on a novel rail-to-rail comparator is proposed in this paper. The power consumption of the comparator is significantly reduced through dynamic operation while the speed is augmented by using an efficient regenerative latch. No biasing circuits are needed and there are no floating nodes in the comparator throughout the conversion process. The digital-to-analog converter (DAC) is formed from a binary array of MIM capacitors. The 250 KS/s ADC implemented in a 0.18 μm process consumes only 1.35 μW of power at a supply voltage of 0.8 V.

Keywords: rail-to-rail comparator, sample-and-hold, digital-to-analog converter, analog-to-digital converter

Classification: Integrated circuits

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1 Introduction

The proliferation of energy constrained systems such as micro-sensor networks, biomedical instrumentation and portable devices has introduced an increasing demand for analog-to-digital converters with resolutions between 8 and 12 bits, speeds of less than 1 MHz but extremely low power consumption. Alongside increasing battery lifetime, low power consumption also allows the use of ambient energy sources, such as solar and vibration. Reducing the supply voltage and circuit complexity are some of the most effective techniques to achieve a low figure-of-merit (FoM) which for Nyquist rate ADCs is given by

$$FoM = \frac{P}{2^{ENOB} f_s} \tag{1}$$

where P is the power consumption, $ENOB$ represents the effective number of bits and f_s is the sampling rate. Consequently, the successive approximation register ADC, has become increasingly very popular due to its low component count and ability to scale well with technology [1, 2, 3, 4, 5, 6].

A classical SAR ADC consists of a sample and hold (S/H) stage, digital-to-analog converter (DAC), a comparator and a control logic. Since the control logic is digital and the capacitor array can be formed using a passive capacitor array, the power consumption of the converter is determined to a large extend by the comparator. The advantage of using a passive capacitor array is that it provides inherent sample and hold. However, using the capacitor array for input sampling has some drawbacks. In low supply voltage environments, the number of boosted sampling switches is as high as the number of bits of the converter and the input capacitance depends on the size of the capacitor array. This increases the complexity and power consumption of the converter. To combat these issues a separate S/H stage can be used [1]. For maximum dynamic range, however, SAR converters with a separate S/H stage need a comparator that can take input signal swings from the lower to the higher supply rail: Input common mode range extends from rail to rail. Rail to rail comparators are especially important when a low supply voltage is used. A solution to this problem was provided in [2] but the comparator dissipates unnecessary energy and the positive feedback is less efficient.

In this paper, a low voltage low power SAR ADC is described based on a dynamic comparator with rail-to-rail input and improved positive feedback technique to speed up the comparison process. Two conventional SAR ADCs are briefly reviewed in Section 2, the proposed comparator is presented in Section 3. Simulation results of the SAR ADC are given in Section 4 and a conclusion is offered in Section 5.

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2 Conventional SAR ADCs

Fig. 1 (a) shows a commonly used SAR ADC structure in which there is no separate S/H stage since the capacitor array acts both as the S/H stage and the DAC. Fig. 1 (b) shows another topology in which there is a separate S/H stage and the capacitor array is used for digital to analog conversion only. Both structures, however, depend on the same operation principle: As shown in Fig. 1 (c), the input is sampled during the first clock cycle when sampling control signal, θ_{samp}, is high. After sampling, the control logic sets the most significant bit (MSB) to a high and the rest of the bits to low causing a change on the output of the DAC. After the comparator has settled, the control logic confirms the final result of the MSB and produces a new code that reconfigures the DAC. Each bit is determined in this way until all the bits

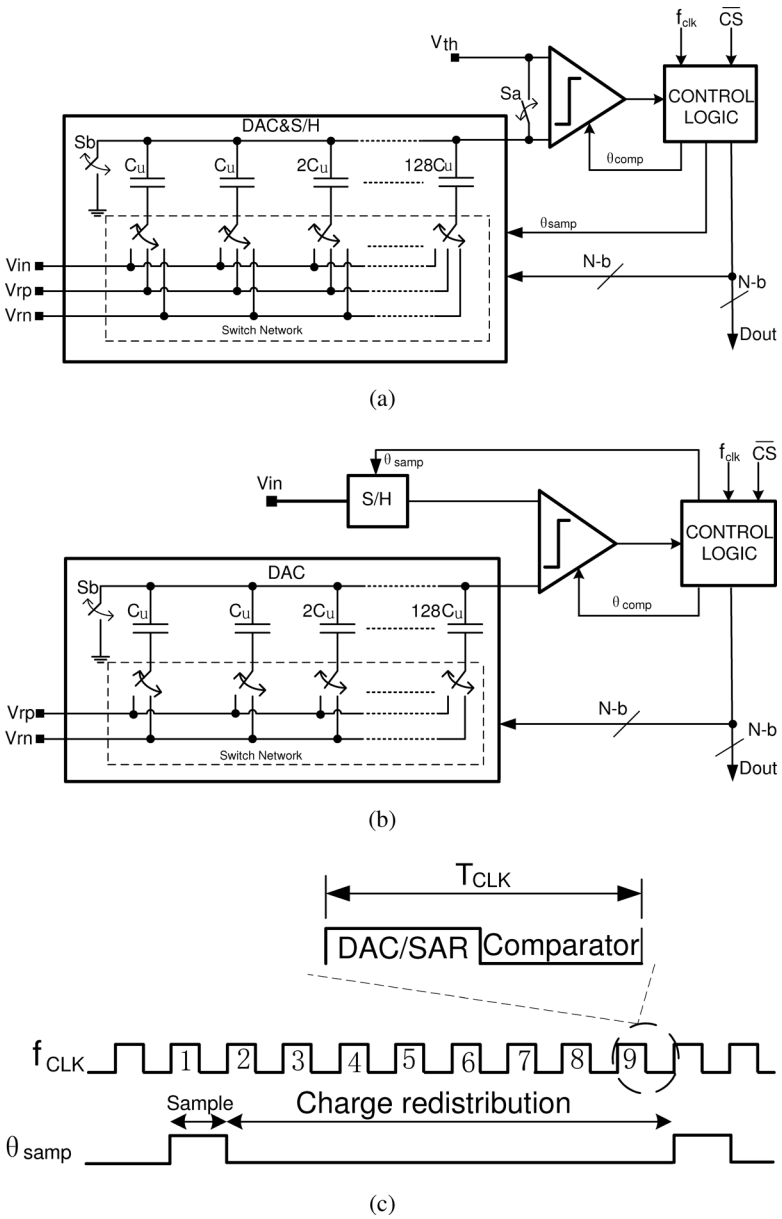

Fig. 1. SAR ADC (a) No Separate S/H (b) Separate S/H (c)Timing

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have been resolved. For an N-bit SAR ADC, the time for a single conversion is at least $(N+1)T_{CLK}$, where $T_{CLK} = 1/f_{CLK}$ is the period of the clocking signal CLK and f_{CLK} is the system frequency. Another similarity between the two structures is that, during charge redistribution, the first phase of each clock cycle is used for DAC settling and SAR delay while the second phase of the clock is allocated for the comparator settling. Therefore, the comparator is idle for half of the conversion time.

One advantage of using the structure in Fig. 1 (a) is that, the comparator is not required to have rail-to-rail inputs since the fixed switching threshold voltage V_{th} against which the DAC output voltage must be compared is sufficient to turn on the input transistor of the comparator. However, a stable and accurate V_{th} should be generated. Moreover, the switch network and control logic is complex since the number of input voltage sampling switches should be equal to the resolution of the ADC. This problem is exacerbated in low supply voltage environments where each switch is driven by a clock boosting stage. By using the structure in Fig. 1 (b) the number of switches is reduced to one irrespective of the converter resolution which greatly simplifies the design. Furthermore, the switching threshold voltage V_{th} is no longer needed. Nevertheless, to convert input voltages that extend to both supply rails, a rail-to-rail comparator is required [1]. Fig. 2 (a) shows a rail-to-rail comparator that was proposed in [2]. The comparator is a parallel combination of an n-type (N0, N1 and N2) and a p-type (P0, P1 and P2) source coupled pairs. Transistors N3, N4, P3 and P4 are load transistors. The current from the n-type pair is mirrored through P5 and P6 and summed with the current from the p-type pair at the drains of the latching transistors N3 and N4.

The operation of the rail-to-rail comparator has two phases: During the reset phase, RST is high and the drains of N3 and N4 are pulled to ground and the comparator outputs are also reset. The evaluation phase starts as soon as RST turns low. If the input voltages are close to the lower supply rail, the p-type pair provides sufficient current for the regeneration at the drains of N3 and N4. If the input voltages are close to the higher supply rail, the n-type pair provides sufficient current for the regeneration. Around the middle of the supply voltages, both p-type and n-type pairs provide the regeneration current. Therefore, the input common mode voltage range is extended to cover both power rails. Beside requiring biasing circuitry and output inverters with designated threshold voltages, the comparator in [2] consumes unnecessary power during the idle (reset) phase and the regeneration formed by only two NMOS transistors (N3 an N4) is not strong enough especially for high speed.

3 Proposed SAR ADC

Fig. 2 (b) shows the proposed dynamic rail-to-rail comparator. The n-type differential branch consists of N0, N1, N2, P3 and P4 while the p-type differential branch consists of P0, P1, P2, N3 and N4 and the rest of the circuit is

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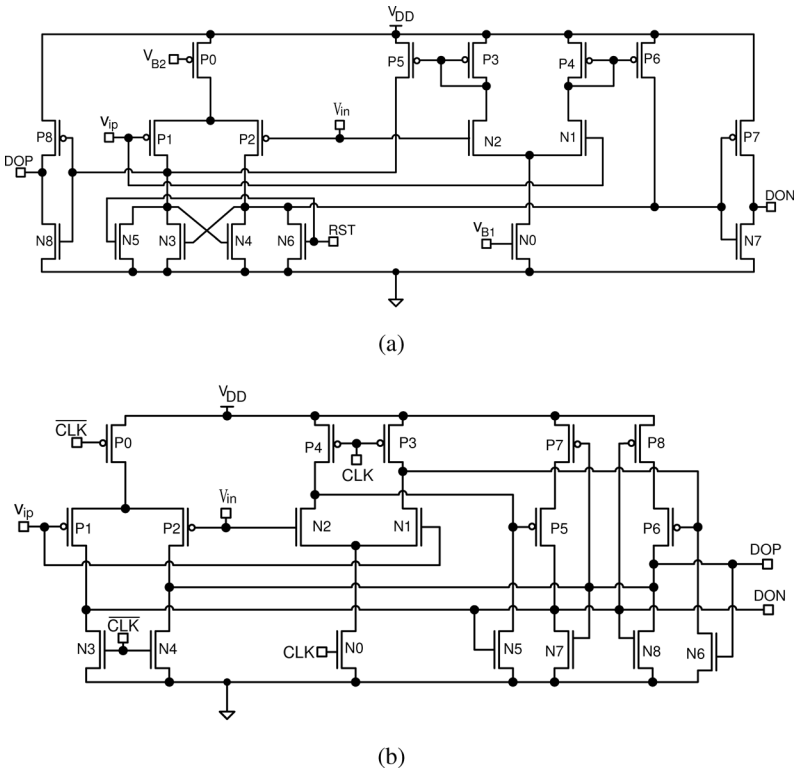

Fig. 2. Rail-to-rail comparator (a) Conventional (b) Proposed

the enhanced regenerative circuit. During the idle phase, CLK is low while its inverted form, $\overline{CLK}$, is high and P3, P4, N3 and N4 are switched on while N0 and P0 are switched off. During this phase, no current flows through the comparator. During the active phase when CLK turns high, the n-type differential branch starts to pull down the gate of P5 and P6 while the p-type pair starts to pull up the gates of N5 and N6. Depending on which input is higher, P5 or P6 turns on faster. A strong positive regeneration then pulls one of the outputs (DOP, DON) high and the other low. Full digital outputs are achieved without extra inverters. Unlike the structure in Fig. 2 (a), the proposed comparator does not consume any static power, no biasing is required, no special inverters are needed and the regeneration is faster since both NMOS and PMOS transistors are involved. The comparator can resolve input voltage differences as low as 150 μV in less than 5 ns. A maximum stack of three transistors is employed which can allow even lower supply voltages in more advanced technologies and no floating nodes, which could potentially cause errors, are present in the comparator. The dimensions of the input transistors N1, N2, P1, P2 were made large to mitigate potential input common-mode dependent offset.

4 Simulation Results

The comparator was applied in the implementation of a 250 KS/s SAR ADC in a 0.18 μm process. The power consumption of the comparator is 0.64 μW with the 0.8 V supply. The 8-bit DAC uses MIM capacitors and consumes

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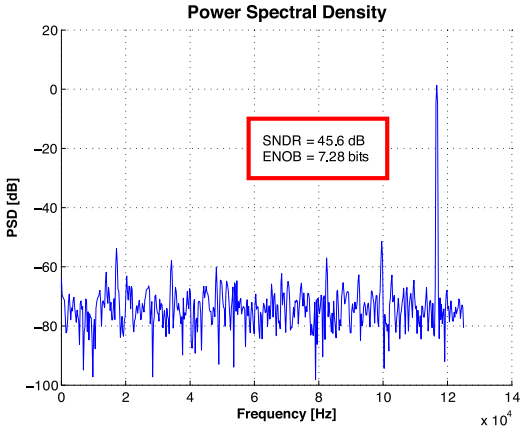
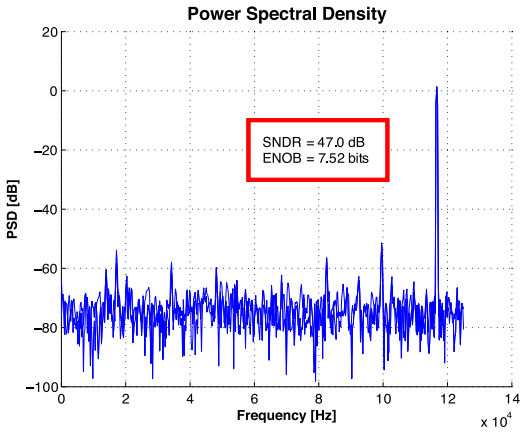


(a)



(b)

Fig. 3. Spectral output for $f_s = 250\,Ks/s$, $f_{in} = 116\,KS/s$ (a) $V_{DD} = 0.8\,V$ (b) $V_{DD} = 1\,V$

Table I. Performance Summary of Proposed SAR ADC

	[1]	[2]	[5]	[6]	Proposed
Technology (μm)	0.18	0.18	0.13	0.18	0.18
Supply (V)	0.5	0.9	1/0.5	1.8	0.8
Input swing/supply	0.25	1	1	N/A	1
Speed (KS/s)	4.1	200	100	50	250
Resolution (bits)	8	8	10	12	8
SNDR (dB)	43.3 (DC)	47.4 (DC)	57	N/A	45.6 (Nyq.)
P_{diss} (μW)	0.85	2.47	1	60	1.35
FoM (fJ/Conv.)	1600	65	17	300	34
Complexity	Low	Low	High	High	Low

a switching power of 0.45 μW while the control logic which is full custom designed takes the rest of the power. The FFT plot when operating the ADC at a sampling rate of 250 KS/s and input frequency of 116 KHz is shown for 0.8 V and 1 V in Fig. 3 (a) and Fig. 3 (b), respectively. At both supply voltages, the ENOB is higher than 7.2 bits. Table I gives a performance summary of the ADC comparing it with other designs. The FoM is twice that of [5] in which a 0.13 μm process has been used. As the improvement

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in CMOS technology lead to significant drop of the FoM, the FoM of this design in 0.13 μm process would be comparable to that of [5]. Meanwhile, the complexity of [5] is much higher in terms of the number of power supply voltages and extra decoding circuits required to support the thermometer codes.

5 Conclusion

The design and implementation of a low power successive approximation register ADC using a dynamic rail-to-rail comparator has been proposed. The efficient power management and strong regeneration of the comparator enable low power and fast operation. Due to the use of a separate sample and hold circuit and the absence of extra decoding circuits, the complexity of the ADC is significantly reduced. Simulation in a 0.18 μm process to verify the proposed techniques shows that, at a supply voltage of 0.8 V, the converter can operate at a sampling rate of 250 KS/s, power consumption of 1.35 μW with an ENOB of 7.28 bits making it a very good choice for applications requiring low power consumption.

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