ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.13, No.6, 1–9

A 128 Kb HfO_2 ReRAM with Novel Double-Reference and Dynamic-Tracking scheme for write yield improvement

Chengying Chen[1], Hongbin Sun[2], Haihua Shen[3], and Feng Zhang[1a)]

[1] *Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, 100029, CHN*

[2] *School of Electrical and Information Engineering, Xi'an Jiaotong University, Xi'an, Shaanxi,710049, CHN*

[3] *School of Computer and Control Engineering, University of Chinese Academy of Sciences, Beijing, 10049, CHN*

a) *zhangfeng_ime@ime.ac.cn*

Abstract: A 128 Kb HfO_2 Resistive Random Access Memory (ReRAM) chip is developed based on HHNEC 0.13 µm 1P8M CMOS process. ReRAM is suffering the write yield problem due to the tail-bit issues and large resistance variations at high temperature. In this paper a novel Double-Reference and Dynamic-Tracking Write (DR-DTW) scheme and a Dynamic read scheme are proposed to fix these issues. The experiment results show that the tail-bit issues are almost eliminated and the write yield is improved greatly compared with traditional write scheme.

Keywords: ReRAM, Double-Reference, Dynamic-Tracking, Dynamic read

Classification: Integrated circuits

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DOI: 10.1587/elex.13.20160061
Received January 25, 2016
Accepted February 10, 2016
Publicized February 26, 2016
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1 Introduction

In recent years with the advancement of VLSI semiconductor process, the integration, access rate and storage capability of nonvolatile memory make a great progress. As the mainstream, flash memory has encountered a bottleneck in the 32 nm process, to find a new storage mechanism to replace flash memory technology has become an inevitable trend in the development of memory. And among a variety of new memory technology, the Resistive Random Access Memory (ReRAM) has the advantages of simple structure, fast read and write speed, low manufacturing cost, low power consumption and compatibility with CMOS process [1, 2, 3, 4, 5]. So it is considered as an excellent memory for the replacement of flash memory technology [6, 7, 8, 9, 10].

Although the ReRAM is a promising memory technology for high-density and CMOS compatible application, it suffers the write yield problem due to the tail-bit issues as Fig. 1 shows. Since the ReRAM cell resistances have large variations, R_{on} (R_{off}) distribution would extend to high (low) resistance direction resulting in tail-bit issues, which may lead to write failure [11, 12].

DOI: 10.1587/elex.13.20160061
Received January 25, 2016
Accepted February 10, 2016
Publicized February 26, 2016
Copyedited March 25, 2016

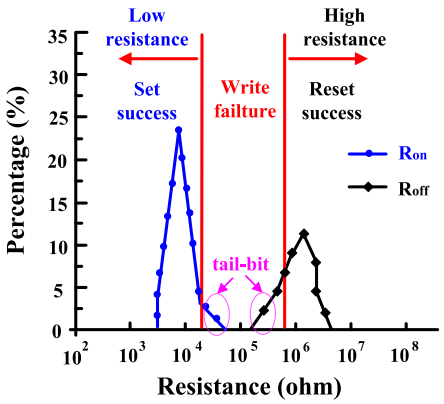

Fig. 1. Tail-bit issues

Since now several write schemes have been reported. Reference [13] presents a transition metal oxide ReRAM with Single Voltage Pulse (SVP). As the SVP is a constant set (reset) voltage, large resistance distribution makes the writing success rate of SVP is very low. In reference [14] the Ramped-Pulse series (RPS) is used as a write-verify-write method. In this method, the step voltage is used to realize the write operation, and the success rate is improved. But the reset operation usually needs several write cycles and a long write time. Reference [15] demonstrated an optimized scheme named Constant Signal Pulse Programming (CSPP). The main idea is that when the high resistance of reset does not reach the preset value, the circuit performs a same reset pulse until it successes. However, the problem of this scheme is that the same reset pulse is often not successful and the success rate of reset is still low.

Among these published literatures, the tail-bit issues and write yield problem during set (reset) to reset (set) are not solved yet. In this paper, we propose a double-reference and dynamic-tracking write (DR-DTW) scheme. Finally a 128 Kb HfO2 ReRAM chip is realized. By using this scheme, even with small R_{on}/R_{off} window, the high resistance and low resistance range will be distinguished. As a result the write yield is finally improved.

2 Double-reference and dynamic-tracking write scheme

Fig. 2 shows the architecture of the proposed double-reference and dynamic-tracking write scheme, which consists of judge module, writing bias generator, writing voltage generator, DR-DTW module and polarity selector. DR-DTW module is the core of this circuit. It monitors the resistance in real time and provides a feedback signal FB_N for judge module to control RPS voltage generated by writing bias generator. The input signal of this circuit comprises WEN, DATA, IN[4:0], Ref_low and Ref_high. WEN is the write enable signal. DATA is the set/reset control signal where “1” stands for set and “0” stands for reset. IN[4:0] is the 32-bit setting bias signal. Ref_low and Ref_high are low voltage threshold and high voltage threshold of comparators respectively.

DOI: 10.1587/elex.13.20160061
Received January 25, 2016
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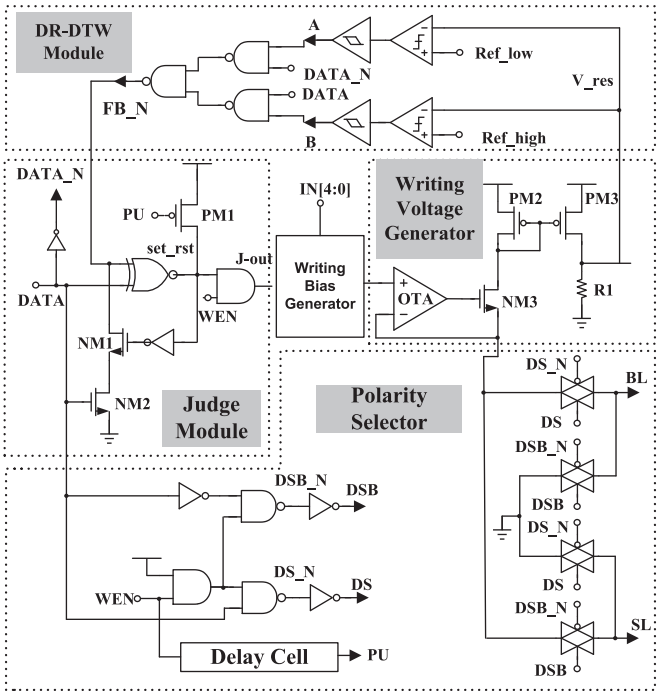

Fig. 2. Proposed double-reference and dynamic-tracking write scheme

Firstly, when double-reference and dynamic-tracking write circuit starts working, WEN is set to "1". And PU is the delay signal of WEN which is still "0" and turns on the PMOS transistor PM1 in a short time. Then J-out becomes "1" and makes writing bias generator provide RPS voltage for set or reset. After PM1 is off, the set_rst will depend on the output of XNOR gate whose inputs are DATA and FB_N. When performing a set operation, DATA is "1", and FB_N changes from "0" to "1". While set is done, the RPS voltage stimulus should be turn off. Because DATA is "1" in this time and FB_N is pulled down to "0", set_rst is "0". So NM1 and NM2 are turned on to lock FB_N as "0". And J-out changes to "0" to turn off the writing bias generator. The writing bias generator includes a resistive voltage divider and a multiplexer. There are 32 levels from power supply to ground that are controlled by IN[4:0] to generate a RPS voltage. The transconductance amplifier (OTA) and NM3 form a regulator to keep the RPS voltage constant. PM2, PM3 and R1 constitute a current mirror to generate V_res that is proportional to the resistance voltage through R1. Then the V_res is input to two comparators and compared with Ref_low and Ref_high. As shown in Fig. 3, when V_res is smaller than Ref_low, two comparators output "00" which means resistance is low. And when V_res is greater than Ref_high, two comparators output "11" which means resistance is high. While comparators output "10", we consider the resistance as invalid resistance. So the double-reference scheme can eliminate the tail-bit problem effectively and improve the write yield. The compared results are hold by two Schmitt triggers and are transferred by several logic gates to form the feedback signal FB_N. The polarity selector is composed of six logic gates and four transfer gates. It determines whether the RPS voltage is applied on BL or SL according to DATA and WEN.

DOI: 10.1587/elex.13.20160061
Received January 25, 2016
Accepted February 10, 2016
Publicized February 26, 2016
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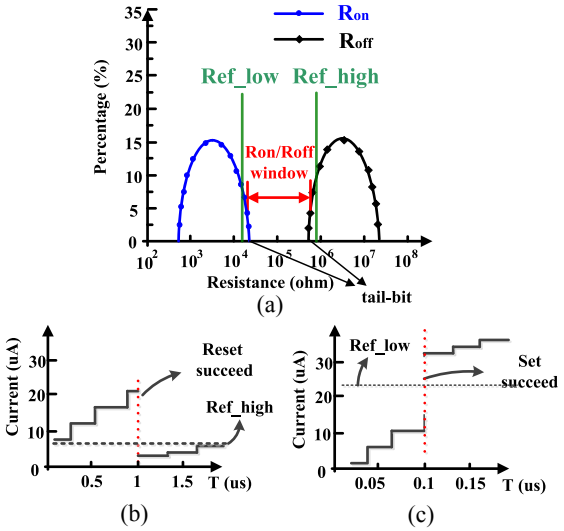

Fig. 3. Double-reference scheme (a) Basis of double-reference (b) Reset write voltage compared with Ref_high (c) Set write voltage compared with Ref_low

The work flow chart of the writing scheme is shown in Fig. 4.

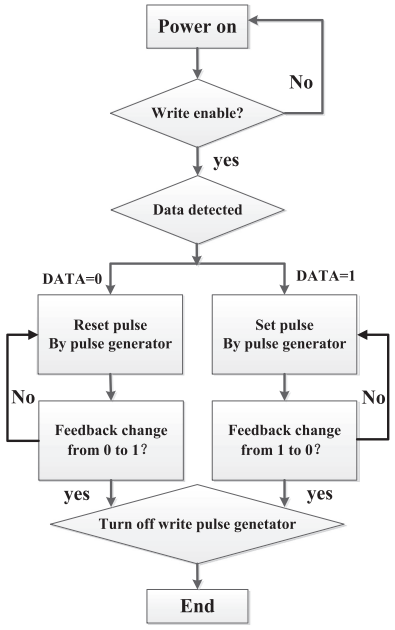

Fig. 4. The work flow chart of the writing driver

3 Dynamic read scheme

When the temperature rises, the high resistance in ReRAM cell will drift to low resistance region. So when the read operation is performed, due to the fixed reference voltage as in transitional circuit, the reading error may be caused by this drifting. In order to fix this error, a reference resistor must be designed to track the ReRAM resistance changes in real-time to maintain sufficient sense margin of read operation at high temperature. And the reference resistor should satisfy (1) and makes as far as possible equal to $1/2(R_{on} + R_{off})$

$$R_{on} < R_{ref} < R_{off} \tag{1}$$

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Received January 25, 2016
Accepted February 10, 2016
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Copyedited March 25, 2016

As a result we use the RRAM memory cell in series to achieve the resistance of the dynamic reference resistor. As R_{off} = 100k, R_{on} = 10k, it needs five resistance units to constitutes the reference resistance. Finally the dynamic reference resistance structure is shown in Fig. 5.

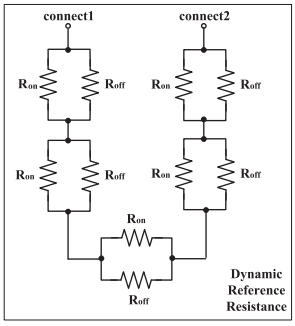

Fig. 5. Dynamic equivalent resistance structure

So the equivalent dynamic reference resistor is:

$$R_{eq} = 5\bullet(R_{on} \;//\; R_{off}) = 5\bullet 1000/110 \approx 45.5k \tag{2}$$

This dynamic reference resistor guarantees its value between R_{on} and R_{off}, which is also about half of R_{on} and R_{off}. Even in high temperature conditions, when the high resistance drifts to the low resistance region, the reference resistor can still be located between the low resistance and high resistance, so as to ensure the correctness of the read results. As shown in Fig. 6, the differential current mode sense amplifier circuit is composed of cross-coupled transistors PM1/PM2, NM1/NM2, input transistors NM3/NM4 and current source NM5 [16, 17, 18]. The principle is that the voltage of the 0.3 V is added to the ReRAM resistor and the dynamic reference resistor respectively through source follower, and both current charges the capacitors C1 and C2 to form readout voltage and reference voltage. The following circuit compares two voltage values and the corresponding data is read out. Clk1 and clk2 are two phases and non-overlap clock. In clk1 phase, the switches S1a and S1b are closed, and the sense amplifier outputs readout voltage and dynamic reference voltage; In clk2 phase, the switches S2a and S2b are closed, the differential output voltages are balanced through C1 and C2 to reset the sense amplifier.

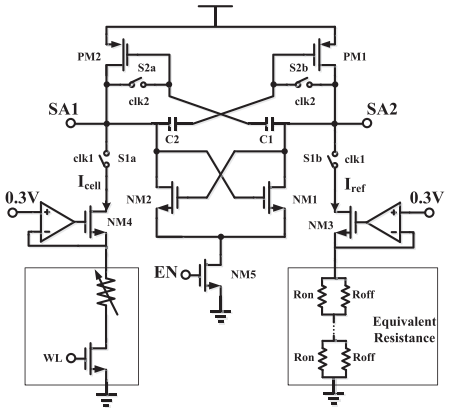

Fig. 6. Current mode sense amplifier

DOI: 10.1587/elex.13.20160061
Received January 25, 2016
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Copyedited March 25, 2016

Based on 500 samples Monte Carlo simulation at 27° and 125°, the simulation result of read circuit is shown in Fig. 7. For typical R_{on} being 10k and R_{off} being 100k at 27°, when temperature rises to 125° and high resistance drifts to low resistance region, the dynamic reference voltage moves toward R_{on} voltage, which is almost at the middle of read voltage between R_{on} and R_{off}. That maintains enough sense margins for accurate read operation.

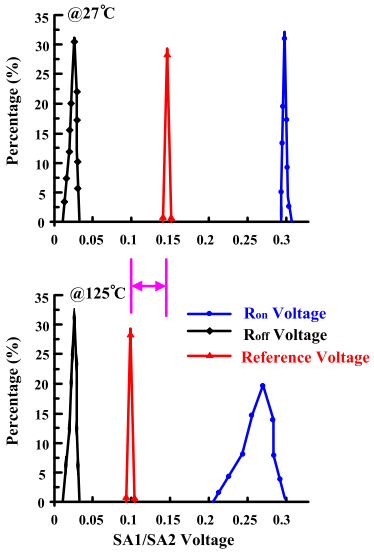

Fig. 7. 500 samples Monte Carlo simulation results of read operation

4 Experiment result

The proposed double-reference and dynamic-tracking write scheme and dynamic read scheme have been designed for a 128 Kb ReRAM chip based on HHNEC 0.13 µm 1P8M CMOS process. And the chip microphotograph is shown in Fig. 8. The 64k ECC ReRAM is used to correct the random access error.

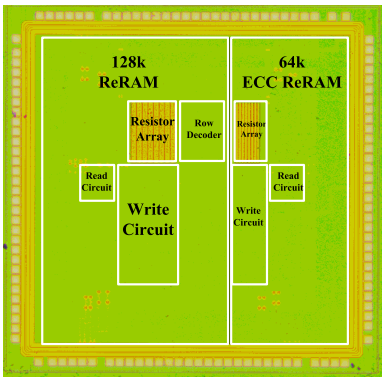

Fig. 8. ReRAM chip microphotograph

The experiment results demonstrate the effectiveness of our proposed method. Write results of two chips are demonstrated in Fig. 9. During set to reset, thanks to tail-bit elimination, the write yield is improved greatly. The high resistances are above 100k and the low resistances are about 10k. In Fig. 10, compared with SVP and RPS, even with high (low) resistance distribution extension problems, the tail-bit issues can be overcome and our DR-DTW write yield improves from 17% and 61.5% to nearly 100% respectively. As the results shows, although the high

DOI: 10.1587/elex.13.20160061
Received January 25, 2016
Accepted February 10, 2016
Publicized February 26, 2016
Copyedited March 25, 2016

resistance and low resistance of ReRAM may drift with temperature, using time and other factors, our proposed scheme can accurately track these changes and complete precise write and read operation with high memory reliability.

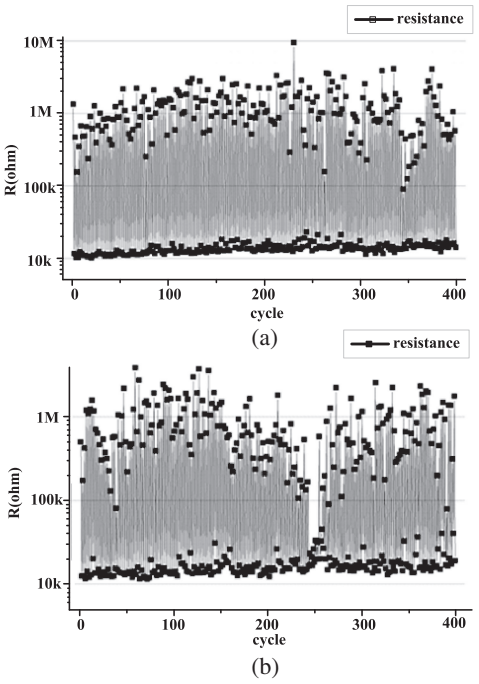

Fig. 9. 200-cycles write results of two chips with DR-DTW write scheme (a) 200-cycles write results of chip one and (b) 200-cycles write results of chip two

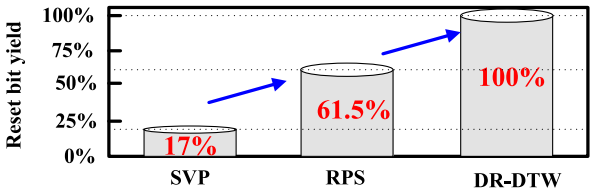

Fig. 10. DR-DTW write yield compared with SVP and RPS

The parameters and performance summary of the ReRAM chip with proposed DR-DTW write scheme are given in Table I. The performance comparisons with

Table I. Comparison with previous work

parameters	This work	[8]	[9]
Process	CMOS 0.13 μm	CMOS 0.18 μm	CMOS 0.13 μm
Storage media	HfO_2	TMO	CuxSiyO
Capacity	128 Kb	—	1 Mb
Supply Power	1.8 V/5 V	3 V	1.2 V/3.3 V
Write scheme	DR-DTW	SVP	RPS
Write yield	Nearly 100%	17%	61.5%

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published ReRAM are also listed. The circuit of our design has the highest write yield.

5 Conclusion

In this paper we propose a double-reference and dynamic-tracking write scheme and dynamic read scheme to improve write yield and voltage reference variation at high temperature for ReRAM respectively. Using these write and read scheme a HHNEC 0.13 μm 128 Kb ReRAM chip is realized. The experiment results demonstrate the tail-bit issues are almost eliminated and the write yield is improved greatly compared with traditional SVP and RPS write scheme. And the dynamic read scheme can resist the reference voltage variation effectively.

Acknowledgments

This work was supported by the National High Technology Research and Development Program of China (No. 2011AA010403 and No. 2011AA010405), the National Natural Science Foundation of China (No. 61474134), the National Natural Science Foundation of China (No. 61173001) and Open Project of Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics of Chinese Academy of Sciences.

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