

# A parallel power amplifier with load impedance transformation for optimized low power performance

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**Abstract:** This paper presents analytic expressions for T-type chain matching network synthesis of the power amplifier (PA) to enhance the performance at low output powers via a load impedance adjustment. Here, a parallel power amplifier for WCDMA B1 (1920–1980 MHz) based on an InGaP/GaAs hetero-junction bipolar transistor (HBT) is utilized, which has a fully integrated matching network on a printed circuit board (PCB). As a result, the power amplifier shows a 38.7% power added efficiency (PAE), and a –37 dBc adjacent channel leakage power ratio (ACLR) at 27.5 dBm output during high power mode operation, and 17.6% PAE with a 22 mA quiescent current and a –40.7 dBc at a back-off output power of 17 dBm during low power mode.

**Keywords:** chain matching networks, load impedance transformation, low power efficiency and linearity, parallel power amplifier, WCDMA

**Classification:** Wireless circuits and devices

## References

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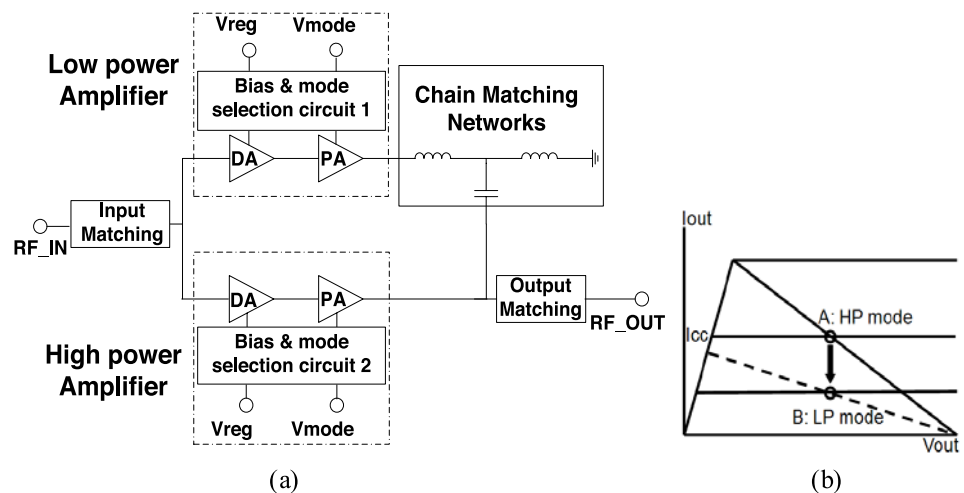
## 1 Introduction

Due to the fact that battery consumption is directly related to operation time, one of the main challenges in mobile phone or wireless device design is increasing talk time. As power amplifiers consume most of the current within mobile devices, much effort has been exerted in improving the efficiency of power amplifiers through various design techniques.

Utilizing optimized bias point and load impedance, power amplifiers for mobile devices in CDMA and WCDMA systems must be designed at full output power to meet critical system requirements such as efficiency, gain, and linearity. However, since such amplifiers operate mostly at low output power levels, efficiency is worsening at backed off lower output power due to unnecessary current consumption [1].

Bias current reduction is a simple method in improving efficiency in general [2], however efficiency enhancement is limited at low power levels. Although dynamic supply voltage control represents an effective method [3], such a method requires larger chip areas and extra cost due to the necessity of additional components such as a DC-DC converter.

For a more simple and cost effective method, a parallel PA can be applied in conjunction with a chain-matching network [4]. However, since low and high PAs are connected each other, a targeted load impedance for low or high output power is affected during each amplifier's operation and determining the values of chain matching components to get the load impedances requires iterative experiment. A straightforward implementation that satisfies all specifications for commercial applications has yet to be developed due to the necessity of chain matching networks to operate in both low and high power modes. In fact, even through high efficiency was reported at low power operation in [4], the PA has to be optimized to set a new load impedance showing much higher linearity in terms of low adjacent channel



**Fig. 1.** (a) Simplified schematic of a parallel power amplifier with the chain-matching network (b) the load line with bias point for high power mode (HP mode) and low power mode (LP mode).

leakage power ratio (ACLR) during practical applications. In this paper, we suggest a synthesizing technique with detailed equations and analytic expression, not mentioned in [4], to find components inserted between high and low power amplifiers and enhance the efficiency and linearity during low output power level while satisfying all performance requirement of considering a mobile system. Finally, the performance of a PA measured from a 1950 MHz WCDMA signal will demonstrate its practical applications.

## 2 Circuit design

Fig. 1 (a) presents the simplified schematic of a parallel power amplifier combining a low and high power amplifier using chain matching networks. The bias and mode selection circuit determines high or low power mode operation while controlling low or high bias point level. Either high PA or low PA is selectively turned on, while the other is off. As such, the targeted load impedance for the low power amplifier should be presented at the low power amplifier collector via a chain matching network and an output matching network.

Fig. 1 (b) shows the bias current and load line characteristics at different power amplifier operations for understanding the efficiency improvement in the parallel power amplifier. If the high power level is needed, high power-generating amplifier operates under the high bias current level such as point A with steep load line. When low power mode is selected, the point A moves to point B with low bias current and the load impedance becomes higher. Since bias point and load impedance are properly transformed while changing the high power mode to low power mode in the parallel power amplifier, the efficiency can be increased with high gain and linearity at low power level. The load impedance modified for each mode can be possible through chain matching networks. However, if chain matching components are not well determined, power leaked into low power amplifier at high power mode makes gain and ACLR performances worse and vice versa. For this reason, implementing the chain matching network for making load impedance without performance reduction is not a simple work and should be exactly analyzed.

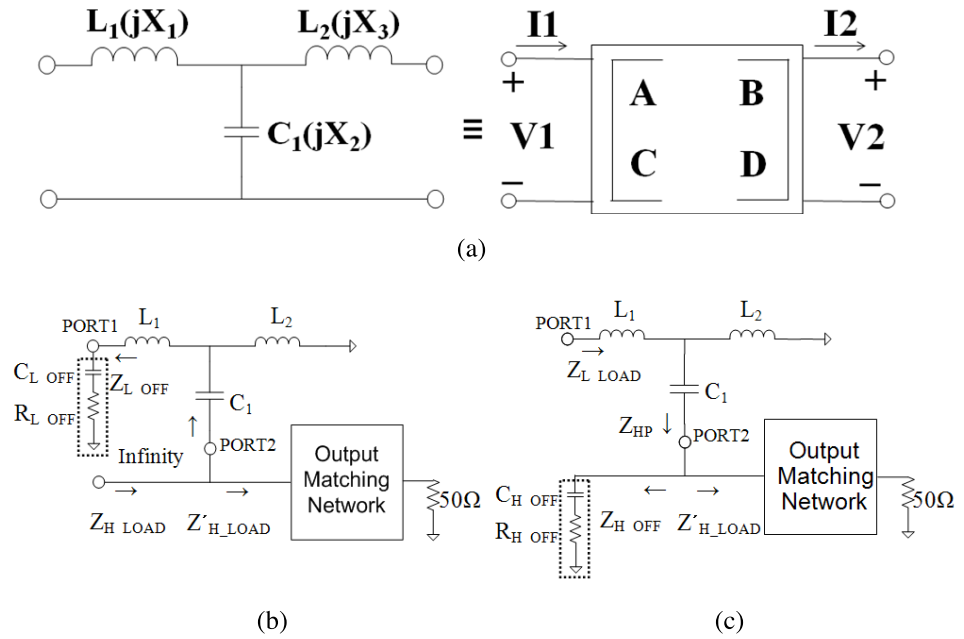
For the first step to synthesize the chain matching networks, Fig. 2 (a) illustrates a T-type chain matching network with ABCD representation, which determines the load impedance transformation between low and high power amplifiers. In the figure,  $L_1$  and  $C_1$  are connected to the low and high power amplifier collector, respectively, and the supply voltage for the low power amplifier can be connected through the  $L_2$  inductor. Initially, in determining components, the ABCD parameters are expressed as

$$A = 1 + Z_1/Z_3 = 1 + X_1/X_3 \quad (1)$$

$$B = Z_1 + Z_2 + Z_1Z_2/Z_3 = j(X_1 + X_2 + X_1X_2/X_3) \quad (2)$$

$$C = 1/Z_3 = 1/jX_3 \quad (3)$$

$$D = 1 + Z_2/Z_3 = 1 + X_2/X_3. \quad (4)$$



**Fig. 2.** (a) Chain matching circuit. (b) An equivalent circuit at HPM. (c) An equivalent circuit at LPM.

The ABCD matrix is defined in terms of the currents and voltages as shown Fig. 2 (a) and the following:

$$V_1 = AV_2 + BI_2, \quad (5)$$

$$I_1 = CV_2 + DI_2. \quad (6)$$

Fig. 2 (b) and (c) show the equivalent circuits during low and high power modes of operation. Targeted load impedances,  $Z_{H\_LOAD}$  and  $Z_{L\_LOAD}$ , are already known by measurements of single-ended or conventional low and high PAs for optimized PA's performances such as gain and ACLR to satisfy practical application's system requirement, and off state impedances for low and high PAs,  $Z_{H\_OFF}$  and  $Z_{L\_OFF}$ , are also measured to determine the components of the chain matching network. Ports 1 and 2 are defined by the disabled PA as off state impedance nodes. To determine the analytical expressions for synthesizing the chain matching networks for the targeted load impedances, boundary conditions for the low and high power modes should be carefully defined as follows:

- Impedance associated with the low power amplifier at port 2,  $Z_{PORT2}$ , should be infinite in ideal case during high power mode (HPM) selection.
- Impedance at port 2,  $Z_{HP}$ , should be transformed into the load impedance of the low power mode during low power mode (LPM) selection.

At HPM, the off state impedance of the low power amplifier ( $Z_{L\_OFF}$ ) should be transformed to infinity at port 2 by the chain matching networks,

resulting in minimum power leaked into the low power amplifier which makes linearity and gain worsening. In terms of impedance, it is expressed to the target load impedance of the high power amplifier ( $Z_{H\_LOAD}$ ) corresponding to the load impedance of the output matching network ( $Z'_{H\_LOAD}$ ). From this condition, the following relations are determined:

$$\begin{aligned} Z_{L\_OFF} &= V_1 / -I_1 = (AZ_{PORT2} + B) / (CZ_{PORT2} + D) \\ &= A/C = R_{L\_OFF} + jX_{L\_OFF} \end{aligned} \quad (7)$$

and

$$Z_{H\_LOAD} = Z'_{H\_LOAD} = R_{H\_LOAD} + jX_{H\_LOAD}, \quad (8)$$

where

$$Z_{PORT2} = V_2 / -I_2 = \infty.$$

At LPM, the load impedance for the low power amplifier ( $Z_{L\_LOAD}$ ) should be obtained via the chain matching network with  $Z_{HP}$ , where  $Z_{HP}$  is the parallel combination of the off state impedance of the high power amplifier ( $Z_{H\_OFF}$ ) and impedance of the output matching network ( $Z'_{H\_LOAD}$ ).

$$\begin{aligned} Z_{HP} &= V_2 / I_2 = Z_{H\_OFF} // Z'_{H\_LOAD} = R_{HP} + jX_{HP}, \\ Z_{L\_LOAD} &= V_1 / I_1 = (AZ_{HP} + B) / (CZ_{HP} + D) = R_{L\_LOAD} + jX_{L\_LOAD}. \end{aligned} \quad (9)$$

$$(10)$$

From (7) to (10),  $X_1$ ,  $X_2$ , and  $X_3$  are calculated as

$$X_1 = -X_{L\_OFF} \pm (X_{L\_OFF}^2 - \beta)^{1/2}, \quad (11)$$

$$X_2 = \alpha - X_{HP} + X_{L\_OFF} + X_1, \quad (12)$$

$$X_3 = -X_{L\_OFF} - X_1, \quad (13)$$

where

$$\begin{aligned} \alpha &= (-X_{L\_OFF}R_{HP} - R_{HP}X_{L\_LOAD}) / R_{L\_LOAD}, \\ \beta &= (\alpha + X_{L\_OFF})X_{L\_OFF} - R_{HP}X_{L\_LOAD} + X_{L\_LOAD} \alpha \end{aligned}$$

Therefore, the T-type chain matching components,  $X_1$ ,  $X_2$ , and  $X_3$ , are uniquely determined once the off state impedances and target load impedance for the low and high power modes of operation are known.

### 3 Measurement results

The parallel power amplifier module is fabricated using a 2  $\mu$ m InGaP/GaAs hetero-junction bipolar transistor (HBT) process. All matching components for the power amplifier including a capacitor (C1) are integrated on a single chip, two inductors (L1 and L2) within the chain matching network being implemented using off chip components. After the off state impedances for each power amplifier are measured ( $Z_{L\_OFF} = 1.5 - j38 \Omega$  and  $Z_{H\_OFF} = 0.43 - j9.86 \Omega$ ), the required reactance for the T-type chain matching network can be determined as shown in Eqs. (11)–(13). Note that the surface

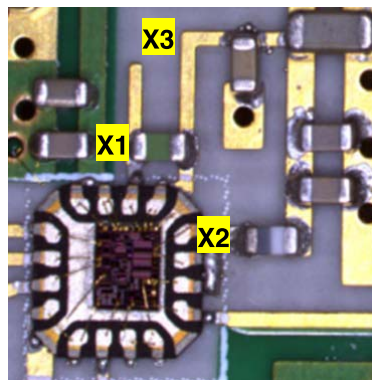
**Table I.** (a) Analytic and real values of chain matching network (at  $f = 1.95$  GHz) (b) Targeted, simulated and measured load impedances for the high and low power modes (at  $f = 1.95$  GHz).

	X1	X2	X3
Analytic value	$j22.02\Omega$ (1.79nH)	$-j13.9\Omega$ (5.9pF)	$j15.97\Omega$ (1.3nH)
Real value	1.4nH (SMD:1nH, bonding wire:0.4nH)	7.3pF	1.1nH (M-line: 280 x 2950 $\mu\text{m}^2$ )

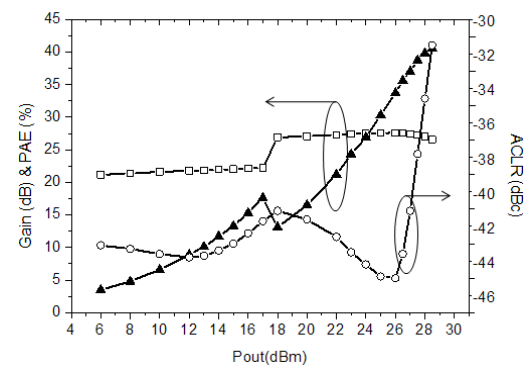
(a)

	Targeted load Impedance( $\Omega$ )	Simulated load impedance( $\Omega$ )	Measured load impedance( $\Omega$ )
High power mode	$4.4 + j1$	$4.32 + j0.97$	$4.42 + j0.48$
Low power mode	$25 + j5.00$	$25 + j1.00$	$30.73 + 7.14$

(b)



(a)



(b)

**Fig. 3.** (a) Photograph of parallel power amplifier on PCB (b) performance results.

mount device (SMD) inductors, bonding wires and metal trace lines on the printed circuit board (PCB) are included in the calculation of the overall  $X_1$ ,  $X_2$ , and  $X_3$  reactance as shown in Table I(a). Because of parasitic impedance from a QFN Package and loss of the real components, the difference between analytic and real values occurs but is not large. Using the determined analytic values, the load impedances are simulated and then measured to compare to the targeted load impedances and well matched as shown in Table I(b). The finally measured load impedances for high power and low power amplifiers are obtained via the chain matching network and are similar with the targeted load impedances. For optimized performance, the parallel power amplifier has been measured at a  $V_{cc}$  of 3.4 V and 2.7 V  $V_{reg}$  with a 0 V  $V_{mode}$  for HPM and a 3.4 V  $V_{cc}$  and 2.8 V  $V_{reg}$  with 2.8 V  $V_{mode}$  for LPM. Power amplifier performances are measured with quadrature phase shift keying (QPSK) modulated signals with a WCDMA channel bandwidth

of 3.84 MHz at 1950 MHz. Fig. 3 (b) reveals the resultant gain, power added efficiency (PAE), and ACLR for both high and low power operations with switching at a 17 dBm output power. The gain is 27.2 dB at 27.5 dBm  $P_{out}$  under HPM and 22.2 dB at 17 dBm under LPM. The high power amplifier PAE is 38.7% at 27.5 dBm  $P_{out}$  and low power amplifier PAE is 17.6% at 17 dBm  $P_{out}$ . In addition, the measured ACLR is  $-37$  dBc at 27.5 dBm (HPM) with a 5 MHz offset and  $-40.7$  dBc at 17 dBm  $P_{out}$  (LPM) which shows enough margins to be applied in practical WCDMA handsets.

#### 4 Conclusion

In this paper, a parallel power amplifier was introduced that includes chain matching network synthesis in order to enhance the overall efficiency and linearity. Chain-matching component values were derived using simple equations, reliable implementation then being possible by controlling the load impedances in order to reduce unnecessary DC power consumption.

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