ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.8, 1–7

A self-biasing class-E power amplifier for 5-GHz constant envelope modulation system*

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Abstract: This paper describes the design of 5-GHz fully integrated self-biasing power amplifier (PA) for wireless transmitter applications in a 0.18-μm CMOS technology. The proposed class-E PA employs the cascode topology with a self-biasing technique to reduce device stress. Three cascaded class-D driver amplifiers are used to actualize the sharp switching at the class-E power stage. All device components are integrated on chip and the chip area is $1.0\times1.3\,\mathrm{mm}^2$. The measurement results indicate that the PA delivers 16.4 dBm output power and 35.4% power-added efficiency with 2.3 V power supply voltage into a 50 Ω load.

Keywords: power amplifier, class-E, self-biasing, CMOS, power-added efficiency, fully integrated

Classification: Integrated circuits

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*This paper is based on the proceedings of [1]. ©IEEE2012

DOI: 10.1587/elex.10.20130174
Received March 14, 2013
Accepted March 19, 2013
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1 Introduction

Recently, more and more devices have been utilizing a function of wireless communication. However, in mobile devices, the short battery life is still a significant problem. Since a power amplifier (PA) consumes largest power in RF front end, the PA must be high efficient to give the battery a longer life. Hence, a class-E PA has been focused attention in many applications. However, class-E PAs can only be applied for constant envelope modulation systems such as Bluetooth and GSM. On the other hand, a linear modulation system such as OFDM for WLAN applies a class-A or AB in order to high linearity in high input range. However, instead of the linear modulation system, a constant envelope modulation system for WLAN at 5 GHz band has been being developed in recent years, and the development of a 5-GHz band class-E PA has been needed [2].

In general, a class-E PA needs a driver amplifier, which provides sufficient input power with the PA to switch a transistor. However, if the transmit power of the PA is low, the overall power-added efficiency (*PAE*) will degrades due to the power consumption of the driver amplifier. In order to avoid the degradation, large power gain of the PA and small power consumption of the driver amplifier are required. They can be actualized by increasing the supply voltage of the PA. However, in CMOS process, it is difficult to increase the supply voltage because the allowable voltage of the transistor is small.

In a class-E PA, a squared-wave signal is desirable for an input signal because it can reduce the switching loss at the transistor. However, a class-AB amplifier which usually used for a driver amplifier can outputs sinusoidal wave only. Therefore, in order to obtain much higher *PAE*, a driver amplifier which can outputs the square-wave signal is required.

This paper describes a 5-GHz single-ended class-E PA using a 0.18-μm CMOS process. The proposed PA employs the self-biasing cascode topology to increase the supply voltage. Cascaded class-D driver amplifiers are used

DOI: 10.1587/elex.10.20130174
Received March 14, 2013
Accepted March 19, 2013
Published April 25, 2013

to provide the square-wave signal with the PA. In addition, all components are integrated on a chip.

2 Circuit design

Schematic of the proposed class-E PA is shown in Fig. 1. The designed PA can be divided into two stages, driver stage and power stage, respectively.

The driver stage consists of three cascaded class-D amplifiers. Each input DC voltage of the class-D amplifiers is biased to output DC voltages with feedback resistors, which are shown as R_1, R_2 and R_3 in Fig. 1. These feedback resistors can provide stable DC bias voltage to the class-D amplifiers and they can reduce DC current consumption compared with a bias technique with dividing resistors [3]. The driver stage needs to be optimized at 5 GHz in order to obtain required power gain with minimum power consumption. First, the number of the stages is optimized by using the analysis results of ADS. As the result, a three-stage driver is optimum because the power gain of a two-stage driver is too small and the power consumption of a four-stage driver is too large. Then, the sizes of the transistors are optimized. As the result, gate widths of each transistor from M_1 to M_6 are selected so as to minimize power consumption of the driver stage with obtaining sufficient driving power to the class-E stage. The gate width of M_1 and M_2, which are an NMOS and a PMOS used in the first stage, are 16 μm and 26 μm, respectively, and then, those of the second stage and the third stage are twice and four times larger than the first stage, respectively, in order to transmit sharp square-wave signal with minimum loss.

In general, a class-E PA needs an output matching network, which transforms from a 50-Ω load resistance to an optimal impedance. Because the output power is inversely proportional to the load impedance, small impedance is needed to increase the power. However, the insertion loss of the matching network becomes large as the transformation ratio increases so that the *PAE* of the PA will be degraded. To prevent this matter, in our proposed PA, we increase the supply voltage and use a small-transformation-ratio output

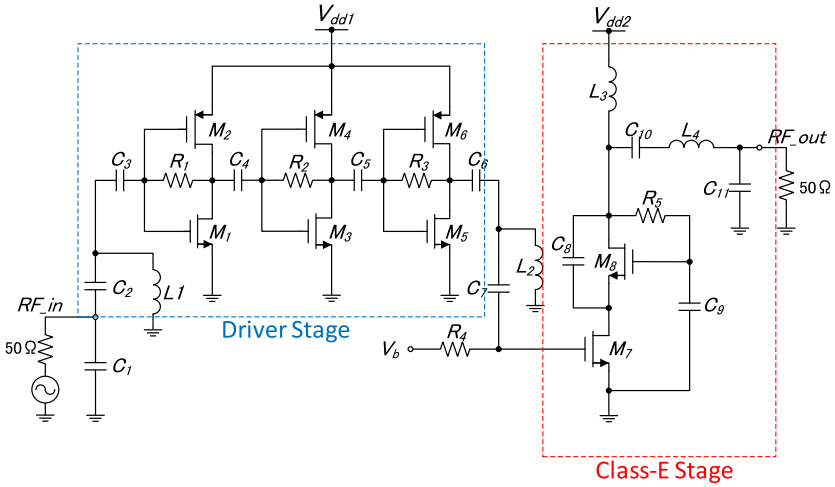

Fig. 1. Schematic of the proposed class-E PA.

DOI: 10.1587/elex.10.20130174
Received March 14, 2013
Accepted March 19, 2013
Published April 25, 2013

matching network, which consists of L_4 and C_{11}, instead of using a large-transformation-ratio output matching network.

In conventional CMOS PAs, the cascode topology is used to reduce the stress of transistors, and the DC voltage at gate of the common gate (CG) transistor is fixed at supply voltage. However, in this topology, it is difficult to increase the supply voltage because the voltage between drain and gate of CG transistor is larger than that of common source (CS) transistor. Therefore, self-biasing cascode technique composed of R_5 and C_9 is employed to reduce the peak voltage between drain and gate of M_8. This technique enables supply voltage to be increased and higher output power and PAE can be delivered [4]. R_5 and C_9 are selected to be the same the peak voltage between drain and gate of M_8 and that of M_7. Where, gate widths of M_7 and M_8 are set to 832 μm and 736 μm, respectively, in order to reduce the on-resistance. However, the parasitic capacitance increases with larger gate width. Then, the switching characteristic becomes dull. Here, C_8 is inserted to compensate the parasitic capacitance. This capacitor is equivalently transformed to a negative capacitor by the miller effect and inserted between drain of M_7 and the ground [5]. Therefore, the parasitic capacitance between drain and the ground of M_7 can be reduced and the switching characteristic can be improved.

Input matching network, which consists of a shunt capacitor C_1, a series capacitor C_2 and a shunt inductor L_1, is designed to transform from the input impedance of the driver amplifiers to 50 Ω. The 50 Ω output resistance is transformed by means of low-pass L-C matching circuit, L_4 and C_{11}. The load impedance is chosen so as to obtain the highest PAE.

The driver stage and the class-E stage are connected to each other through an inter-stage matching network. The network is obliged to have some inductors because of the input capacitance of the class-E stage. But, an inductor has larger loss at 5 GHz than the frequency where conventional class-E PAs are operated. Therefore, the number of inductors has to be minimized. We used a T-type inter-stage matching network which is realized by C_6, C_7 and L_2. The shunt inductor, L_2, is optimized to obtain the maximum PAE at 5 GHz.

3 Simulation and measurement results

The proposed class-E PA has been fabricated in a standard 0.18-μm CMOS technology. Fig. 2 shows the photomicrograph of the proposed class-E PA. The die area including pads, which are contacted to G-S-G and DC probes, is $1.0\times1.3\,\mathrm{mm}^2$.

Fig. 3 shows the simulated waveform of drain voltage and drain current of M_8. Where, V_{dd1}, V_{dd2}, V_b and input power are 1.8 V, 2.3 V, 0.7 V and -5 dBm, respectively. As can be seen in Fig. 3, the voltage is almost zero while the transistor is at ON state. On the other hand, while the transistor is at OFF state, the current is non-zero due to the parasitic capacitance. However, the voltage and current are not maximum level at the same time.

DOI: 10.1587/elex.10.20130174
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Accepted March 19, 2013
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Therefore, the power dissipation or the product of drain voltage and current are minimized and high efficiency can be obtained.

The measured and simulated output power (P_{out}) and PAE at 5.0 GHz are shown in Fig. 4 (a). Where, bias voltages, V_{dd1} and V_{dd2} and V_b, are 1.8 V, 2.3 V, 0.7 V, respectively. It can be seen that the proposed PA delivers the maximum output power of 16.4 dBm with 35.4% PAE. Compared with the simulation results, the measurement results are declined at overall input power due to the contact resistances of the DC probes. In addition, the parasitic inductance at the source of CS MOSFET, which had not been taken into account during the simulation, causes the negative feedback and decreases the power gain and the PAE.

Fig. 4 (b) shows the measured P_{out} and PAE versus supply voltage of the power stage (V_{dd2}) for a fixed input power of −4 dBm. It can be seen that the P_{out} increases proportional to the V_{dd2}, when the supply voltage is swept from 1.5 V to 2.5 V. On the other hand, PAE is saturated when V_{dd2} increases to 2.5 V.

The measured P_{out} and PAE versus frequency at the input power of −4 dBm is shown in Fig. 4 (c). It is observed that the largest P_{out} and the

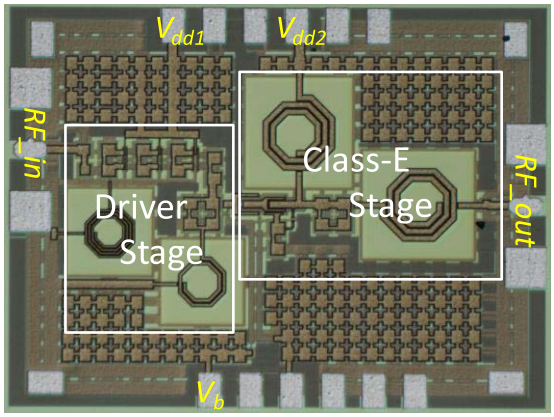

Fig. 2. Photomicrograph of the proposed class-E PA.

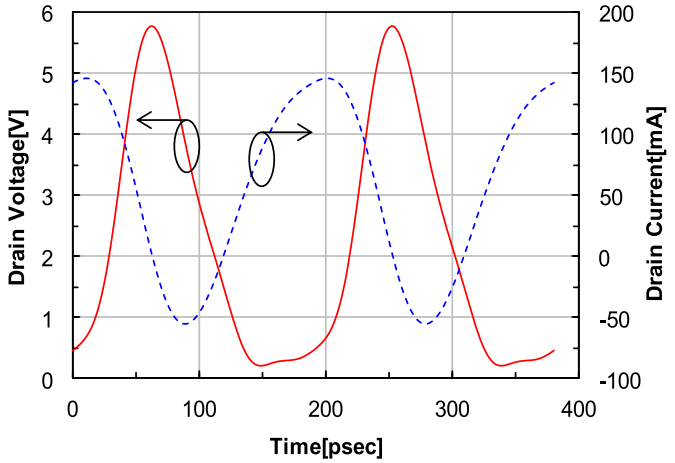

Fig. 3. Simulated time domain signal of drain voltage and drain current of M_8.

DOI: 10.1587/elex.10.20130174
Received March 14, 2013
Accepted March 19, 2013
Published April 25, 2013

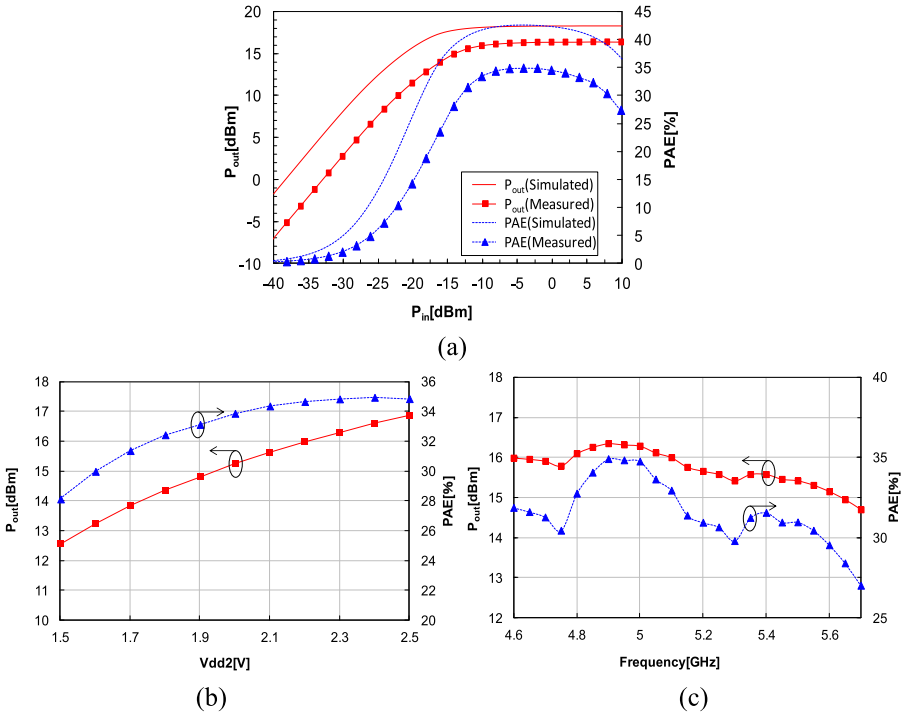

Fig. 4. (a) Measured and simulated output power (P_{out}) and PAE versus input power (P_{in}), (b) Measured P_{out} and PAE versus supply voltage of the power stage (V_{dd2}) and (c) Measured P_{out} and PAE versus frequency.

Table I. Performance comparisons of the reported CMOS class-E PAs.

Reference	Technology[μm]	Frequency[GHz]	P_{out}[dBm]	PAE[%]	Area[mm^2]
[6]	0.18	2.4	19.2	27.8	0.37
[7]	0.18	2.35	11	44.5	1.7
[8]	0.18	2.4	20	43.6	2.24
This work	0.18	5.0	16.4	35.4	1.3

highest PAE can be obtained at the center frequency of 4.9 GHz. Furthermore, High PAE of more than 30% can be obtained at the frequency range of from 4.75 GHz to 5.25 GHz.

Table I presents the comparison of performances of the reported CMOS class-E PAs and this work. From TABLE I, the proposed class-E PA can operate at the highest frequency in these PAs with high efficiency approximately equal to the previously reported class-E PAs.

4 Conclusion

A 5-GHz fully integrated class-E PA in a 0.18-μm CMOS process is proposed. The proposed PA is the first class-E PA for the 5-GHz constant envelope modulation system. All circuit components have been integrated on a chip. The self-biasing cascode topology is utilized to reduce device stress and to increase supply voltage. Three cascaded class-D driver amplifiers are

DOI: 10.1587/elex.10.20130174
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integrated with the power stage to switch the transistors effectively. The proposed PA achieves 35.4% maximum *PAE* and 16.4-dBm saturated output power for measurement. The degradation of the power gain and *PAE* can be improved by modifying the layout so as to reduce the parasitic inductance at the source.

Acknowledgments

This work was partly supported by a grant of Regional Innovation Cluster Program (Global Type 2nd Stage) from Ministry of Education, Culture, Sports, Science and Technology (MEXT) and a Grant-in-Aid for KAKENHI (Wakate-B and Kiban-B) from JSPS. This work was also partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with CADENCE Corporation and Agilent Corporation.

DOI: 10.1587/elex.10.20130174
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