ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.11, No.12, 1–5

Rail to rail CMOS complementary input stage with only one active differential pair at a time

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Abstract: A simple scheme for rail to rail op-amp operation is introduced. The input stage uses complementary differential pairs but only one pair is active at a time. It uses very compact control circuitry. Experimental verification is provided from a test chip prototype in 0.5 µm CMOS technology.

Keywords: analog integrated circuits, CMOS integrated circuits, amplifiers, low-voltage low power design

Classification: Integrated circuits

References

[1] R. Hogervorst and J. H. Huijsing: *Design of Low-Voltage, Low Power Operational Amplifier Cells* (Kluwer, 1996).

[2] M. R. Valero, S. Celma, N. Medrano and B. Calvo: IEEE Trans. Circuits Syst. II **59** [99] (2012). DOI:10.1109/TCSII.2012.2213361

[3] W. M. C. Sansen: *Analog Design Essentials* (Springer Dordrecht, The Netherlands, 2006) 301. ISBN 0-387-25746-2.

1 Introduction

Input stages with complementary differential pairs (CDP) operating in parallel, as shown in Fig. 1, are commonly used to ensure operation with rail-to-rail (R2R) input common-mode signals [1, 2]. A quite comprehensive survey of the most common R2R techniques reported in literature can be found in [3]. In CDP-based Op-Amps extra circuitry is needed in order to keep the total transconductance gain (g_m) constant since in the middle region of the input common mode range (ICMR) both input pairs are active whereas close to the rails only one of the input pairs is active [1]. As a result, the transconductance g_m of the input stage and the gain bandwidth product and phase margin of the op-amp can vary over the ICMR.

DOI: 10.1587/elex.11.20140392
Received April 25, 2014
Accepted May 21, 2014
Publicized June 4, 2014
Copyedited June 25, 2014

In most of the approaches with CDPs with MOS transistors operating in strong inversion the g_m control circuit is relatively complex and has impact on power consumption [1, 3]. Besides, in most of these techniques, such as in the g_m control by electronic Zener, square root current control, etc. [1], part of the total current of the pairs is 'divert' in order to maintain a constant g_m, thus deteriorating the power efficiency. Additionally, in regions of the ICMR where both differential pairs (DP) are active but one of them does not have enough headroom to maintain its tail current source in saturation, the CMRR and PSRR of the op-amp are severely degraded.

In this paper we propose a simple R2R scheme with CDPs that have only one of the DPs active at a time and whose tail current source remains in saturation over the ICMR. This is achieved with very simple switching circuitry that requires very small additional power dissipation. A gm control circuitry is not required.

This paper is organized as follows: In section 2 we describe the scheme. In section 3 we discuss simulation and experimental results of a fabricated test chip prototype and section 4 provides conclusions.

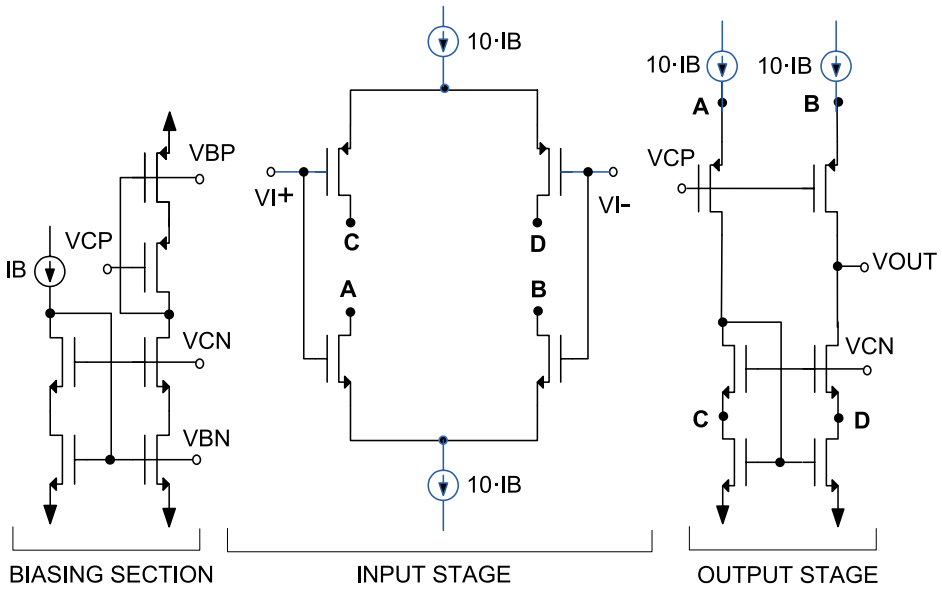

Fig. 1. Classical rail-to-rail amplifier with complementary pairs input stage (g_m control circuitry not shown).

2 Proposed scheme

Fig. 2 shows the proposed R2R input stage, which has been used to implement a R2R folded cascoded Op-Amp. The same output stage and biasing section of the classical amplifier in Fig. 1 has been chosen for a proper comparison.

The input stage of Fig. 2 uses current sensing replica DPs formed by M_{1SP}, M_{2SP}, M_{BSP} and M_{1SN}, M_{2SN}, M_{BSN}, which are scaled down by a factor 5. This, in order to decrease power consumption. Their tail currents sources have a value $2I_b$ while the main DPs formed by M_{1P}, M_{2P}, M_{BP} and M_{1N}, M_{2N}, M_{BN}

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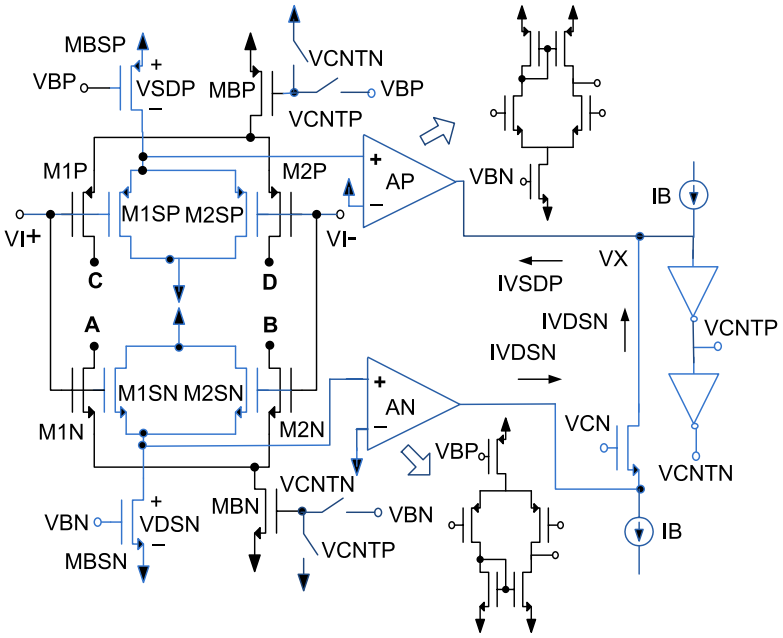

Fig. 2. Proposed complementary pairs input stage that has only one active differential pair. The control circuit (in blue) generates control signals V_{CNTN} and V_{CNTP} that maintain only the DPs whose tail current source has the largest $|V_{DS}|$. The biasing and output sections are the same as shown in Fig. 1

respectively have tail currents with value 10Ib. The drain-source voltages of the replica tail current sources are measured by amplifiers A_N and A_P. These are implemented using differential pairs with an active mirror load (see Fig. 2) and with bias current $2I_b$.

These amplifiers generate output currents I_{VDSN} and I_{VSDP} that are proportional to the drain-source voltage of M_{BSN}, the tail current source of the replica NMOS and to the source-drain voltage of M_{BSP} the PMOS replica tail current respectively. These currents are subtracted at node V_x and generate a signal voltage $V_x = (I_{Vdsn} - I_{Vsdp}) \bullet R_x$ (where $R_x \sim r_o$ is the impedance at node X). This voltage is transformed into rail (digital) control voltages V_{CNTN} and V_{CNTP} by two CMOS inverters. V_{CNTN} goes high (V_{DD}) if the drain source voltage of M_{BSN} is higher than the source-drain voltage of M_{BSP} otherwise V_{CNT} voltage goes low (V_{SS}). V_{CNTN} and V_{CNTP} are used to turn on only the main differential pair (NMOS or PMOS) whose tail current source has the largest $|V_{DS}|$.

Notice that in this implementation the tail transistor of the DP that is active has a large $|V_{DS}| > V_{DD} - V_{SS} - V_{GS}$ and operates in deep strong inversion. For this reason and as opposed to most other approaches with CDPs the Op-Amp has a high CMRR and PSRR over the entire CMIR. Including the power dissipation of amplifiers A_N and A_P the circuit implementation of Fig. 2 has slightly less static power dissipation as two main DPs that remain active with a bias current source $10I_b$ each $P_d = (V_{DD} - V_{SS}) \bullet 19I_b$. This is 10Ib in the active DP, 2Ib in each amplifier A_P and A_N, 2Ib in

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each current sensing DP and Ib in the cascode transistor (This is lower than that of a conventional CDP without g_m control circuit $P_d = (V_{DD} - V_{SS}) \bullet 20I_b$. In the circuit of Fig. 2 g_m remains constant over the ICMR since the NMOS and PMOS complementary DPs have by design have the same nominal g_m.

3 Simulation and experimental results

The folded cascoded Op-Amp with complementary pairs input stage of Fig. 2 that has only one active differential pair was simulated and fabricated using NMOS and PMOS unit transistors with sizes 30 µm/1 µm and 75 µm/1 µm in the control section. Transistors in the main DP and the output section were scaled up by a factor 5. The circuit was fabricated in 0.5 µm CMOS technology and both simulated and tested with a bias current $I_b = 50\,\mu A$ and supply voltages $V_{DD} = 1.8\,V$ and $V_{SS} = -1.8\,V$ and a load capacitance $C_L = 13\,pF$.

Fig. 3 shows the experimental input and output waveforms for a $3.4\,V_{pp}$ 1 kHz triangular input signal with the op-amp working as a voltage follower. The magnitude of the input signals is 0.2 V short of R2R amplitude since the output stage is cascoded.

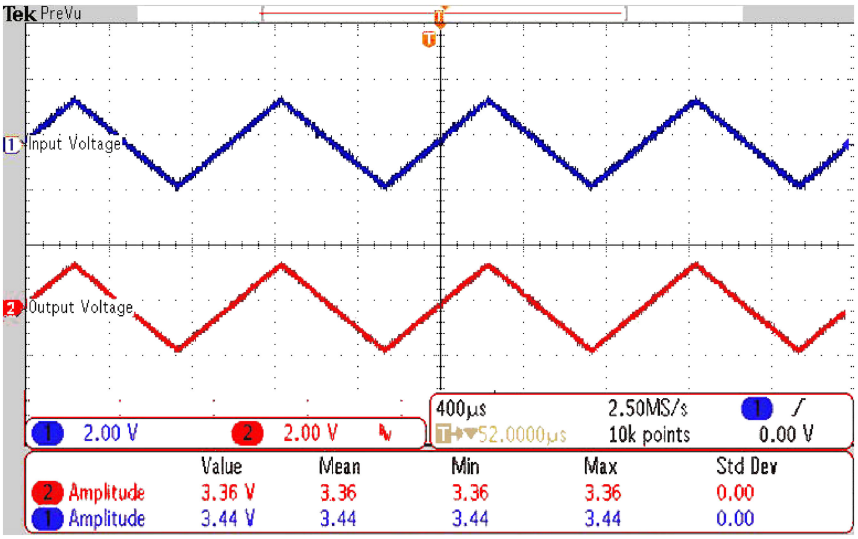

Fig. 3. Experimental input (top) and output (bottom) waveforms for a 3.4 Vpp 1 kHz triangular input signal with op-amp operating as voltage follower.

Table I summarizes simulated and experimental results of Op-amp parameters which are in close agreement. It can be seen that the BW as voltage follower remains approximately constant within the ICMR. This verifies that g_m also remains constant over the entire ICMR.

4 Conclusion

A simple approach to alternatively switch DPs in R2R complementary input stages was introduced. It avoids the transition region where both DPs are

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Table I. Experimental and Simulation Parameters

Parameter	Simulated	Measured	Units
Open-Loop Gain	66.69 @ DC	66.7 @ DC	dB
Open loop Bandwidth	16.3	13.33	KHz
CMRR	113 @ DC, & ICMV = 0 V 114 @ DC & ICMV = −1.7 V 114 @ DC & ICMV+ = 1.7 V	106 @ DC & ICMV = 0 V 99.5 @ DC & ICMV = −1.7 99.8 @ DC & ICMV = 1.7 V	dB
Unit-Gain freq	29	23	MHz
CMRR @ unit-gain freq	37.9 @ 29 MHz & ICMV = 0 38.3 @ 29 MHz & ICMV−1.7 V 35.6 @ 29 MHz & ICMV = 1.7 V	41.15 @ 23 MHz & ICMV = 0 V 40.0 @ 23 MHz & ICMV = −1.7 V 32.5 @ 23 MHz & ICMV = 1.7 V	dB
PSRR	139 @ DC Positive rail 27 @ 29 MHz Positive rail 115 @ DC, Negative rail 20 @ 29 MHz, Negative rail	127 @ DC, Positive rail 8 @ 23 MHz, Positive rail 114 @ DC, Negative rail 13.7 @ 23 MHz, Negative rail	dB
Phase margin	71	95	°
BW of OpAmp as Voltage Follower with C_L = 13 pF	27&ICMV = 1.6 V 27&ICMV = 1.2 V 27&ICMV = 0.8 V 27&ICMV = 0.4 V 27&ICMV = 0 V 27&ICMV = −0.4 V 27&ICMV = −0.8 V 27&ICMV = −1.2 V 27&ICMV = −1.6 V	22&ICMV = 1.6 V 22&ICMV = 1.2 V 22&ICMV = 0.8 V 22&ICMV = 0.4 V 22&ICMV = 0 V 22&ICMV = −0.4 V 22&ICMV = −0.8 V 22&ICMV = −1.2 V 22&ICMV = −1.6 V	MHz
Gain margin	19.1	-	dB

active and for this reason a g_m control circuit is not required. A constant g_m and CMRR over the entire ICMR was verified experimentally.

Acknowledgments

This work was supported by FPU fellowship program from the MICINN to M. R. Valero, MICINN-FEDER (TEC2009-09175) and MINECO-FEDER (TEC2012-30802).

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