

A new method of spur reduction in phase truncation for DDS

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Abstract: DDS (Direct digital synthesizer) is widely used for frequency synthesis. The factors that contribute to spurious signals are analyzed. Adding a random signal to DDS system was used for spurious reduction formerly. Those methods assuredly reduce the spurs while the noise floor of signals is worsened. A new spurious reduction technique based on two DDS is proposed. The first DDS generates the conventional sine signal. The other DDS produces the error signal which compensates for the phase truncation error in traditional DDS system. A spurious reduction circuit has been developed. The experimental result indicates that the spurious signal due to phase truncation can be reduced 8 dBc at least.

Keywords: direct digital synthesizer (DDS), phase truncation, spurious reduction, error compensation

Classification: Microwave and millimeter wave devices, circuits, and systems

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1 Introduction

DDS is a new frequency synthesis technique which is the most widely used in frequency synthesizers, especially in fast agile frequency synthesizer systems. DDS has the advantage of high frequency resolution, low phase noise, fast agile frequency, and phase controllability compared with PLL frequency synthesizers.

Because of phase truncation, DAC quantization, and DAC nonlinearity in DDS systems, there are large numbers of spurious signals distributed in the Nyquist band. It is difficult to filter the spurious signals arisen by phase truncation in some applications because different frequency words will result in different spurious signal frequency position and power. It narrows the applications of DDS. It is a key technique that how to reduce spurious signals arisen by phase truncation. Some methods have been proposed for spurious reduction [1, 2]. These methods require that random noise to be fed into the phase accumulator. By this way the periodicity of phase truncation can be broken. Then the spurious signals will be de-correlated into noise and will be reduced. Spurious signal can also be reduced by feeding random signals into the phase accumulator and DAC simultaneously [3]. The noise fed into DDS is independent of the periodicity of phase truncation. Those methods assuredly reduce the spurs, but at the same time the noise floor at DDS output spectrum is worsened.

In this paper, we propose a novel method for reducing spurious signals caused by phase truncation using the phase truncation error compensation technique, which is based on two DDS. One DDS acts as a conventional DDS. The other DDS generates the error information truncated by the conventional DDS. The compensation error is combined with the conventional DDS output signal after digital-to-analog conversion and attenuation.

2 DDS spurs fundament

The DDS is shown in simplified form in Fig. 1 [4]. The DDS consists of the following basic blocks: phase accumulator, sine look up table and digital-to-analog converter. The phase accumulator consists of an N -bit phase register which stores the N -bit accumulated phase value. At each system clock the frequency word is added to the phase accumulator. Only the upper P -bit

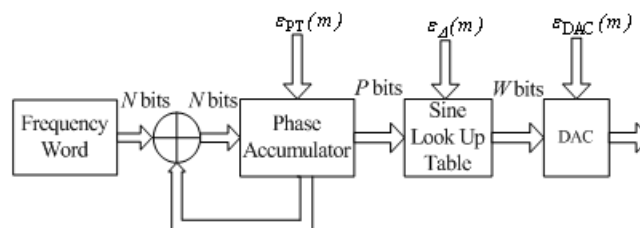


Fig. 1. Simplified block scheme of DDS

value of phase accumulator is transferred to sine look up table. Usually, N is

much larger than P to achieve high frequency resolution. The lower $(N-P)$ -bit value is truncated, which results in phase truncation error $\varepsilon_{PT}(m)$. During the process of phase-to-amplitude conversion, quantization error $\varepsilon_{\Delta}(m)$ is imported because of the limited resolution of quantization (W bits). The W -bit value from sine look up table is delivered to DAC. In nature, a DAC is a nonlinear device, which is the source of harmonics, aliasing content, and clock feedthrough represented by $\varepsilon_{DAC}(m)$ in all. In conclusion, DDS spurs mostly arise from phase truncation, amplitude quantization and DAC nonlinearity. The phase truncation spurs depending on frequency are the most difficult to be filtered in some cases. Spurious reduction for phase truncation is only considered here. Supposed that FTW represents the frequency word of DDS and f_C represents the system clock of DDS, the output signal frequency is given by:

$$F_{OUT} = \frac{FTW}{2^N} f_C \quad (1)$$

As described above spurious signals are mixed with the desired signal. Here phase truncation error and DAC quantization error are considered. As the accumulator sequence proceeds, the value of the accumulator will eventually return to the original tuning word value and the value in phase accumulator will repeat. The period of the sequence is given by

$$PRT = \frac{2^N}{GCD(2^N, FTW)} \quad (2)$$

Here, $GCD(2^N, FTW)$ is the Greatest Common Divisor of both 2^N and FTW . According to the sampling theory, there will be PRT discrete spurs in the output spectrum.

3 New spurious reduction method

The performance of DDS will be degraded because of the phase truncation spurs which are difficult to be filtered in some cases. New technique against the phase truncation spurs is expected. FTW represents frequency word as described above. Based on the consideration of the phase truncation, the DDS output signal can be expressed as:

$$y(m) = \sin\left\{\frac{2\pi}{2^N}[m * FTW - \text{Rem}(m * FTW, 2^{N-P})]\right\} \quad (3)$$

Where $\text{Rem}(m * FTW, 2^{N-P})$ is the residue of $m * FTW$ and 2^{N-P} . Supposed that DAC's resolution is W bits and equal quantization is selected in the sine look up table, formula (3) can be rewritten as:

$$y(m) = \text{Round}\left\{2^W * \sin\left[\frac{2\pi}{2^N}(m * FTW - \text{Rem}(m * FTW, 2^{N-P}))\right]\right\} / 2^W \quad (4)$$

Where $\text{Round}(\dots)$ functions rounding to the nearest whole number. Formula (4) can be expanded as:

$$y(m) = \text{Round}\left\{2^W * \cos\left[\frac{2\pi}{2^N} * \text{Rem}(m * FTW, 2^{N-P})\right] * \sin\left[\frac{2\pi * m * FTW}{2^N}\right] - 2^W * \cos\left[\frac{2\pi * m * FTW}{2^N}\right] * \sin\left[\frac{2\pi}{2^N} * \text{Rem}(m * FTW, 2^{N-P})\right]\right\} / 2^W \quad (5)$$

Where $\text{Rem}(m * FTW, 2^{N-P}) < 2^N$ so we can have:

$$\cos\left[\frac{2\pi}{2^N} * \text{Rem}(m * FTW, 2^{N-P})\right] \approx 1 \quad (6)$$

$$\sin\left[\frac{2\pi}{2^N} * \text{Rem}(m * FTW, 2^{N-P})\right] \approx \frac{2\pi}{2^N} * \text{Rem}(m * FTW, 2^{N-P}) \quad (7)$$

Substituting from (6) and (7), (5) may be approximated as:

$$y(m) \approx \text{Round}\left[2^W * \sin\left(\frac{2\pi * m * FTW}{2^N}\right)\right] / 2^W - \frac{2\pi}{2^P} * \text{Round}\left[2^W * \cos\left(\frac{2\pi * m * FTW}{2^N}\right) * \frac{\text{Rem}(m * FTW, 2^{N-P})}{2^{N-P}}\right] / 2^W \quad (8)$$

It is evident that the first item of (8) represents the DDS output signal without the phase truncation. The second item is the error due to the phase truncation which is smaller than the first item. We can find another signal $y'(m)$ which is expressed as follows:

$$y'(m) = \text{Round}\left[2^W * \sin\left(\frac{2\pi * m * FTW}{2^N}\right)\right] / 2^W \approx y(m) + \frac{2\pi}{2^P} \left[2^W * \cos\left(\frac{2\pi * m * FTW}{2^N}\right) * \frac{\text{Rem}(m * FTW, 2^{N-P})}{2^{N-P}}\right] / 2^W \quad (9)$$

We can see that signal $y'(m)$ has no phase truncation error. The signal $y'(m)$ is what we expected. The first item of (9) can be achieved by a conventional DDS and the second item of (9) can be achieved by an improved DDS. The signal $y'(m)$ can be got by combining the two DDS with a power combiner. The implement scheme is shown in Fig. 2. The DDS cores are implemented

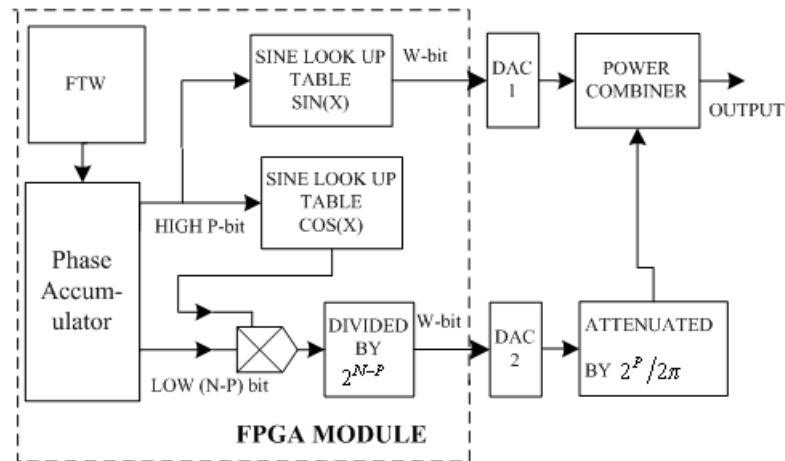


Fig. 2. The implement scheme of spurious reduction

in a FPGA. The upper P -bit value from the phase accumulator is divided into two branches. The first branch is transferred to sine look up table and then DAC 1. It generates the conventional DDS signal. The second branch is transferred to cosine look up table. The cosine value is multiplied by the lower $(N-P)$ -bit value of the phase accumulator. The multiplication product is divided by 2^{N-P} and then transferred to DAC 2. The analog signal

from DAC 2 is attenuated by $2^P/2\pi$ with an attenuator. The second branch generates phase truncation error which is truncated by the conventional DDS. The phase truncation error is combined with the conventional DDS signal by a power combiner. The combiner is with the features of 2-way and 0-degree. The output signal of the combiner is the desired signal $y'(m)$ with phase truncation compensation.

The spurious reduction method has been simulated with Matlab. Here assume that $N = 32$, $P = 15$, $W = 12$, and $FTW = 402669568$. According to (2) the period of phase sequence is 262144. Nonlinearity of DAC is not in consideration and the combiner is ideal. The output spectrum of the conventional DDS and the output spectrum of the compensated DDS are simulated for comparison. The output spectrum of the conventional DDS is shown in Fig. 3 (a). The worst spur in Fig. 3 (a) is about 90 dBc below desired signal.

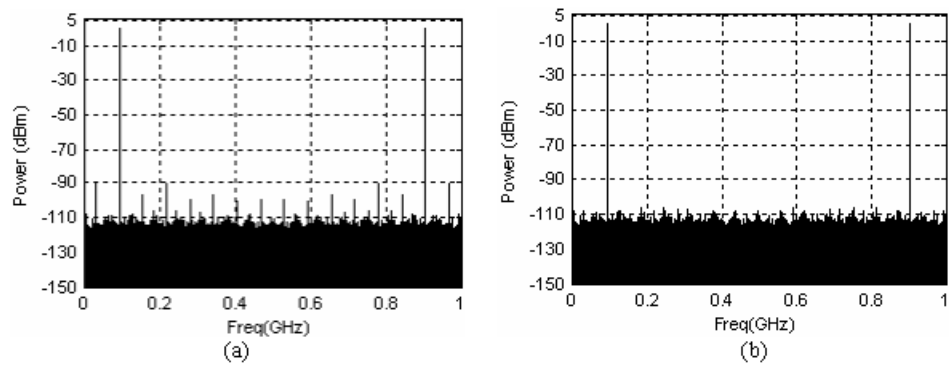


Fig. 3. (a) The output spectrum of conventional DDS (b) The output spectrum of compensated DDS

The spurs level above noise floor and below the desired signal are all sourced from phase truncation. The output spectrum of the compensated DDS is shown in Fig. 3 (b). The worst spur in Fig. 3 (b) is about 105 dBc below the desired signal. The spurious suppression of the compensated DDS can be improved by about 15 dBc compared with that of the conventional DDS.

4 Experiment results

The earlier computer simulation of spurious reduction didn't reveal nonlinearity of DDS and other real factors. It is necessary to do an experiment to verify the accuracy of the method. In this experiment Virtex-4 from Xilinx is introduced to implement DDS core with the system clock of 500 MHz [5]. The sample rate of DAC(AD9736 from Analog Devices) is 1 GSa/s. The fully differential LVDS DDR (Double Data Rate) interface fulfills data transfer between FPGA and AD9736. The updating rate of data from FPGA is 1 GSa/s. The combiner ADP-2-1 comes from Mini-circuits. The attenuator made up of lumped elements must be designed carefully. The attenuation value can be determined by:

$$L = 20 \log \frac{2\pi}{2^P} = -74.345 \text{ dB} \quad (10)$$

The phase relationship of the two DDS can be realized by means of modifying the phase value in the compensating DDS core.

The tested spectrum of conventional DDS output signal of the first branch is shown in Fig. 4(a). The frequency of the desired signal is about 94 MHz with the power of 5.33 dBm. In addition, there are three harmonics and one

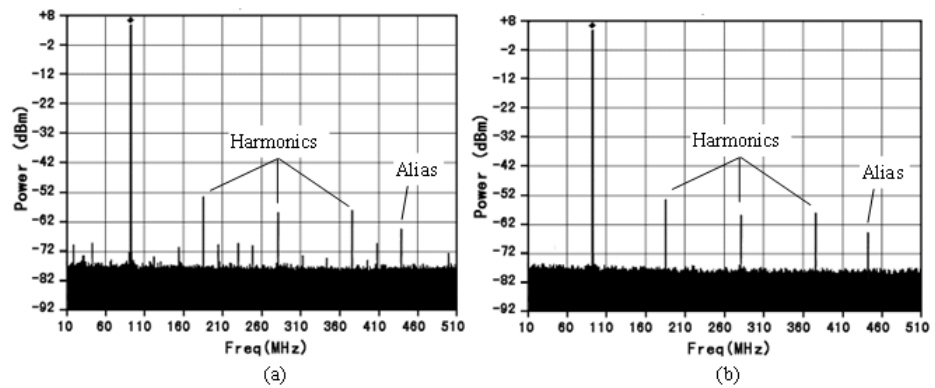


Fig. 4. (a) The tested spectrum of conventional DDS output (b) The tested spectrum of compensated DDS output signal

alias. The power of them is relatively high. The rest spectrum lines above noise floor are spurs associated with the phase truncation. Generally, the spurs associated with phase truncation may expand at any position of the Nyquist band. The position and power of the spurs are variable along with the signal frequency. So the spurs associated with the phase truncation are more serious than harmonic, alias, and amplitude quantization error. They are more difficult to be filtered in some cases. In Fig. 4(a) the capacity of spurious suppression associated with phase truncation is about 67 dBc. The tested spectrum of the compensated DDS output signal is shown in Fig. 4(b). The spurious reduction method has no effect on the desired signal, harmonics and alias. The capacity of spurious suppression associated with phase truncation is 75 dBc at least. The actual spurs will not be seen because the limited resolution bandwidth of spectrum analyzer used. Compared with the spurious suppression of the conventional DDS, the spurious suppression of the compensated DDS is improved by 8 dBc at least.

5 Conclusion

A method of compensating for phase truncation error in DDS is proposed, which can improve the spurious suppression effectively. The experiment result indicates that the spurious signal due to phase truncation can be reduced by 8 dBc at least. Compared with traditional spurious reduction methods, the merit of this method is that there is no extra fed noise.