

# A study on the self turn-on phenomenon of power MOSFET induced by the turn-off operation of body diodes

Tsuyoshi Funaki<sup>a)</sup>

*Osaka University, Div. of Electrical, Electronic and Information Eng.*

*Graduate School of Engineering, Suita, Osaka 565–0871, Japan*

*a) [funaki@eei.eng.osaka-u.ac.jp](mailto:funaki@eei.eng.osaka-u.ac.jp)*

**Abstract:** SiC power devices generally operate with fast switching. The fast switching operation in power conversion circuits suffer from the self turn-on phenomenon of a power MOSFET in which the gate voltage is induced to fluctuate by the turn-on operation of the MOSFET on the other side in the bridge circuit. The self turn-on results in a large power loss, when the fluctuating gate voltage exceeds the threshold gate voltage. This paper analytically discusses the self turn-on phenomenon of the MOSFET related to the turn-off operation of its body diode, which is initiated by the turn-on operation of the MOSFET on the other side in the bridge. This analysis was evaluated experimentally.

**Keywords:** self turn-on, gate voltage fluctuation, power MOSFET, body diode

**Classification:** Electron devices, circuits, and systems

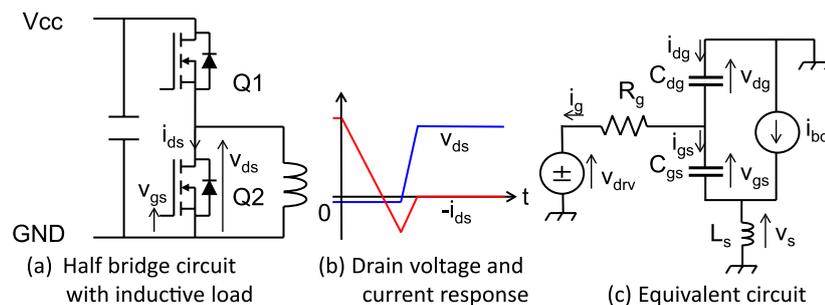
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## 1 Introduction

Fast switching power devices are required for high frequency switching to miniaturize the passive components in a power conversion circuit. SiC Schottky barrier diode and MOSFET realize fast switching operation in high voltage power conversion circuits [1]. Fast high voltage switching and/or large current induces Electromagnetic compatibility (EMC) difficulties stemming from high  $dv/dt$  and  $di/dt$  [2]. The fast switching operation of one MOSFET in the bridge circuit is known to induce gate voltage fluctuations in the MOSFET on the other side. This phenomenon, when the voltage fluctuation exceeds threshold gate voltage, that results in transient partially conducting conditions is called “self turn-on.” The partial conduction in self turn-on causes large conduction losses, stemming from high dc bus voltage [3]. The larger  $dv/dt$ , which is imposed on MOSFET, generates larger conduction losses in self turn-on [4]. The condition of self turn-on to the applied  $dv/dt$  on MOSFET has been analytically evaluated [5]. Minimizing gate resistance of the gate drive circuit, adding capacitance between the gate and the source terminal, superimposing bias voltage on the gate for off state mitigates the self turn-on phenomenon [6]. The mutual interaction between parasitic inductance in the source terminal of MOSFET and the body diode turn-off also induces gate voltage fluctuation [7]. This paper analytically derives the gate voltage behavior associated with the turn-off operation of the body diode in MOSFET, which is initiated by the turn-on operation of the other MOSFET in the bridge. The gate voltage behavior is experimentally evaluated in a test circuit.

## 2 Analytical derivation of gate voltage behavior in MOSFET



**Fig. 1.** Test circuit and equivalent circuit for analyzing gate voltage fluctuation.

Fig. 1(a) shows the configuration of a half bridge circuit with inductive load. In this section, we study the gate voltage behavior of Q2 in the body diode turn-off operation associated with the turn-on of the MOSFET Q1 that is on the other side in the bridge. The terminal capacitance of the semiconductor device has a nonlinear voltage dependency. However, for the simplicity of analysis and derivation of analytical solution, this analysis treats the terminal capacitance as a time invariant linear component. The following study treats

the channel blocking condition in MOSFET Q2 by applying an off gate voltage from a gate drive circuit, when the reverse current conducts through the body diode while MOSFET Q1 turns-on. This corresponds with the diode turn-off operation in a diode clamp inductive circuit. The drain voltage and the current outlines are illustrated in Fig. 1(b). The body diode current decreases and undershoots in turn-off. The drain voltage begins to build up with the depletion of the semiconductor layer when the undershot current reaches its peak value. The turn-off process of body diode was accomplished through these reverse recovery processes. Here, we focus on the period where the forward direction body diode current decreases and reverses.

The equivalent MOSFET and gate drive circuits for the body diode turn-off are illustrated in Fig. 1(c). The decaying body diode current, which is induced by the turn-on operation of the MOSFET on the other side in the bridge, is expressed by the current source  $i_{bd}$ .  $L_s$  denotes the parasitic inductance at the source terminal, which cannot be neglected for large  $di/dt$ . The transfer function from input current source  $i_{bd}$  to output voltage  $v_{gs}$  is derived as follows.

The differential equations for the terminal capacitance and parasitic inductances are Laplace transformed as seen in Eq. (1).

$$\left. \begin{aligned} I_{dg} &= C_{dg}sV_{dg} \\ I_{gs} &= C_{gs}sV_{gs} \\ V_s &= L_s s(I_{gs} + I_{bd}) \end{aligned} \right\} \quad (1)$$

Eq. (2) is obtained by KVL.

$$R_g I_g = V_{gs} + V_s \quad (2)$$

The drain-source voltage  $V_{ds}$  is almost constant during this period. The following approximations are then applied.

$$sV_{ds} = sV_{gs} + sV_{dg} = 0 \quad (3)$$

Finally, the transfer function  $G(s)$  is derived as Eq. (4).

$$G(s) = \frac{V_{gs}}{I_{bd}} = \frac{-L_s s}{L_s C_{gs} s^2 - R_g(C_{dg} + C_{gs})s + 1} \quad (4)$$

Here, the decaying body diode current is modeled with a ramp function  $i_{bd}(t) = k_c t$  ( $k_c > 0, i_{bd}(0) < 0$ ), i.e., the body diode current is expressed as Eq. (5).

$$I_{bd} = \frac{k_c}{s^2} \quad (5)$$

The gate voltage  $V_{gs}$  is then obtained as Eq. (6).

$$V_{gs} = \frac{-k_c L_s}{L_s C_{gs} s^2 - R_g(C_{dg} + C_{gs})s + 1} \frac{1}{s} \quad (6)$$

Here, the gate voltage response comprises a step and second order system response. Eq. (6) is expanded to a partial fraction as Eq. (7).

$$V_{gs} = \frac{k_c L_s}{2} \left\{ \frac{1 + \frac{A\sqrt{B}}{B}}{s - \frac{A-\sqrt{B}}{2C_{gs}L_s}} + \frac{1 - \frac{A\sqrt{B}}{B}}{s - \frac{A+\sqrt{B}}{2C_{gs}L_s}} - \frac{2}{s} \right\} \quad (7)$$

Where,  $A = R_g(C_{dg} + C_{gs})$  and  $B = A^2 - 4C_{gs}L_s$ .

The time response of gate voltage is derived as Eq. (8) by inverse Laplace transformation.

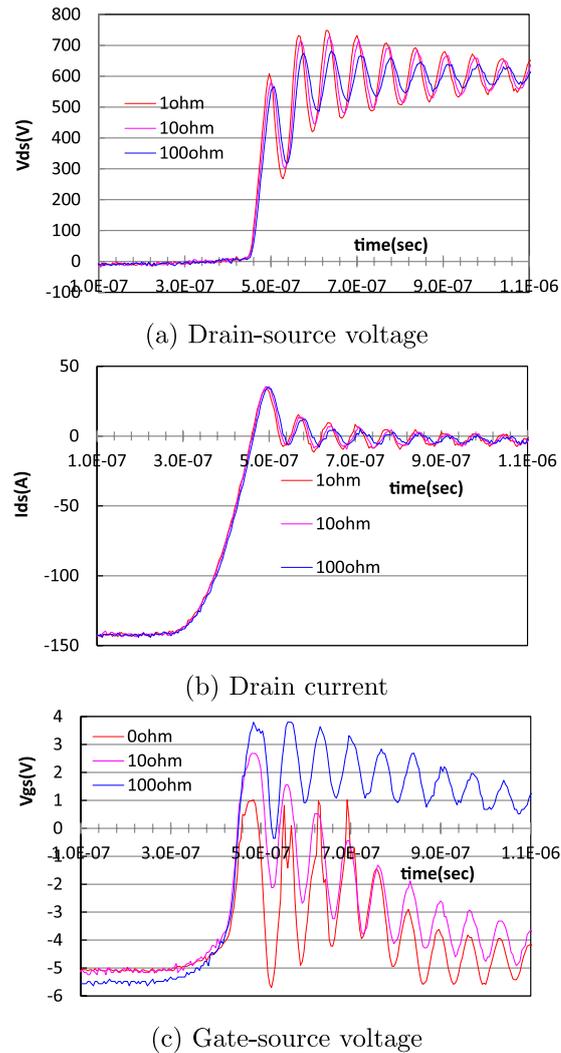
$$v_{gs} = \frac{k_c L_s}{2} \left\{ \left( 1 + \frac{A\sqrt{B}}{B} \right) e^{\frac{A-\sqrt{B}}{2C_{gs}L_s}t} + \left( 1 - \frac{A\sqrt{B}}{B} \right) e^{\frac{A+\sqrt{B}}{2C_{gs}L_s}t} - 2 \right\} + const \quad (8)$$

When the real part of the exponent in Eq. (8) is positive, the gate voltage increases exponentially with time. Moreover, when the discriminant  $B$  is positive, the time constant in the exponent becomes positive and monotonically increases. Alternately, when the discriminant  $B$  is negative, the gate voltage oscillates. The exponent time constant  $\frac{A-\sqrt{B}}{2C_{gs}L_s}$  becomes large for large parasitic inductance at the source terminal, small gate resistance, and small gate-drain capacitance, which mitigates the gate voltage rise. Although, the coefficient of gate voltage rise is proportionate to the current slew rate  $k_c$  and parasitic inductance  $L_s$ , the gate resistance has no influence on this coefficient. This differs for drain voltage applications [5], where gate resistance dominantly affects gate voltage behavior.

### 3 Experiment

This section experimentally evaluates gate voltage response as well as the influence of gate resistance and  $di/dt$  in the body diode turn-off for the off state of MOSFET by applying negative bias voltage to the gate. The test circuit in Fig. 1(a) was designed to evaluate the gate voltage behavior of MOSFET Q2 for the MOSFET Q1 switching operation. The full SiC power module (BSM180D12, 1200 V, 180 A, ROHM) was evaluated for high voltage and large current fast switching operation. The double pulse method used for the evaluation is generally employed to characterize the reverse recovery phenomenon of diodes. The gate drive circuit applied negative bias voltage to the gate via gate resistance during the off period. Figs. 2 and 3 show the drain voltage, drain current, and gate voltage response in Q2.

Fig. 2 indicates the experimental results for different gate resistance in Q2. The drain voltage of MOSFET Q2 in Fig. 2(a) is kept constant at  $-2$  V at the onset of the body diode turn-off that is shown around  $t = 3.0 \times 10^{-7}$  s in Fig. 2(b). The drain voltage begins to build up when drain current reaches approximately 0 A (around  $t = 4.5 \times 10^{-7}$  s). On the other hand, the gate voltage built up exponentially in synchronization with the decrease of drain current, as given in Eq. (8). That is, the gate voltage exponentially builds up, but there is an insensible difference to the gate resistance, as recognized in Eq. (8). A difference in peak gate voltage was found with the gate voltage resistance. The drain voltage already begins to build up when the gate voltage gives the peak value. Therefore, the difference is recognized as the gate resistance effect in the gate voltage behavior to the applied drain voltage [5]. Furthermore, the gate voltage recovers to the off-gate voltage after reaching the peak, and is in accordance with the time constant, which is dependent on the gate resistance value.

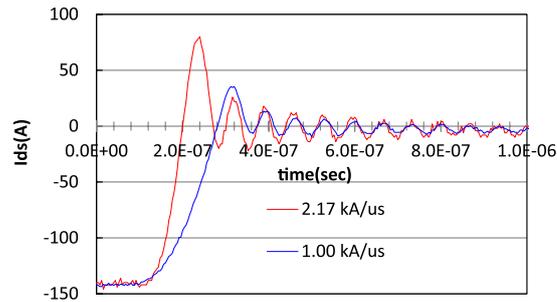


**Fig. 2.** Response of SiC MOSFET to the body diode turn-off (gate resistance).

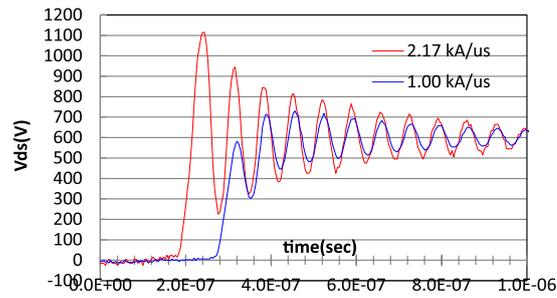
Fig. 3 presents the experimental results for the different switching speeds ( $di/dt = 1.00 \text{ kA}/\mu\text{s}$  and  $2.17 \text{ kA}/\mu\text{s}$ ). The gate resistance of Q1 was changed to regulate  $di/dt$  body diode turn-off Q2. The gate voltage rise given in Eq. (8) was proportionate to the slew rate of the drain current  $k_c$ , which emerges as the difference in the built-up gradient of gate voltage in Fig. 3(c) for  $V_{gs} < -3.5 \text{ V}$ . The steep gate voltage build up for  $V_{gs} \geq -3.5 \text{ V}$  was attributed to the application of high  $dv/dt$  of drain voltage, as shown in Fig. 3(a). The higher  $dv/dt$  of fast switching also results in a steeper gate voltage rise and a higher peak gate voltage. Therefore, we can conclude that the mutual interaction of source inductance and the body diode turn-off current affects the early stage of gate voltage fluctuation. However, the trailing peak gate voltage is dominated by the applied  $dv/dt$  of the drain voltage.

#### 4 Conclusion

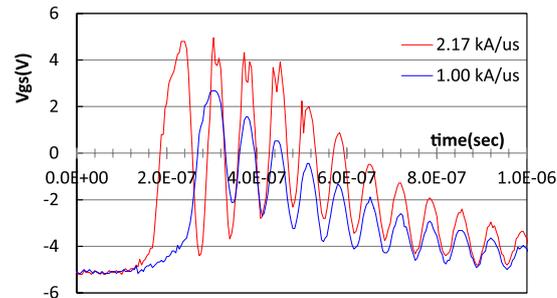
This paper discussed the gate voltage behavior of MOSFET associated with a fast switching operation of the SiC power device. An analysis formula for gate



(a) Drain-source voltage



(b) Drain current



(c) Gate-source voltage

**Fig. 3.** Response of SiC MOSFET to the body diode turn-off ( $di_{ds}/dt$ ).

voltage was derived for the channel blocking state for the body diode turn-off in MOSFET. The slew rate of current and parasitic inductance in the source terminal affects the gate voltage rise when body diode turns-off and the influence of gate resistance is low. The gate voltage behaviors of SiC MOSFET were experimentally evaluated and confirmed. However, the peak value of the gate voltage rise was dominated by the  $dv/dt$  of the applied drain voltage in the test circuit. That is, the fabricated test circuit had sufficiently low source inductance to cause gate voltage rise in the turn-off operation of the body diode in MOSFET.

### Acknowledgments

This research is partially supported by the JSPS FIRST Program, JST super cluster program, and NEDO strategic energy saving technology innovation program.