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Recent progress and prospects of terahertz CMOS

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Abstract: Recent progress and prospects of terahertz CMOS integrated circuits is reviewed. The development of terahertz CMOS is somewhat different from the conventional digital and RF CMOS evolution, in that it is not fueled as much by technology scaling. Rather, the key enablers are progress in high-frequency device characterization and modeling techniques and also in design techniques near transistor's active operation limit, f_{max}.

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1 Introduction

CMOS 60-GHz Wi-Fi products are nearing mass production, and 5G (fifth-generation) cellular network is also another platform where millimeter-wave CMOS products are likely to play a vital role [1]. Development of 77-GHz and 79-GHz CMOS radar front end has also been very active. For the above-mentioned frequency bands, the target applications have long been clear, and the well-motivated development of CMOS millimeter-wave front end has generally been successful. This success owes very much to the device performance improvement by means of miniaturization.

At frequencies above 100 GHz, target applications are not as obvious yet. Nevertheless, research into integrated circuits covering these 'terahertz' frequencies is becoming active these days. One important aspect of terahertz CMOS is that its development is not as tightly linked with CMOS technology advancement by miniaturization. The latter is an ongoing effort but is geared toward digital circuits, not extreme frequencies. State-of-the-art CMOS processes can even be a suboptimal choice for terahertz circuits for two reasons. One is because of the fact that passive components cannot be made smaller by migrating to a more advanced process. While digital circuits can enjoy cost reduction due to device and interconnect geometry shrinking, terahertz circuits will inevitably include multistage amplifiers with many passive components that occupy a large die area, implying undue increase in the costs. The other is that the better current drivability of the MOSFET due to reduced channel length does not necessarily lead to commensurately higher unity-power-gain frequency, f_{max}. Here the power gain is either the maximum available gain or Mason's unilateral gain [2]. As a result, 65-nm CMOS is often used for terahertz circuits for offering reasonable balance between performance and cost. But if device performance improvement isn't there to help, what is it that is enabling CMOS designers to tackle terahertz circuit development? The key enablers are recent progress in high-frequency device characterization and modeling and also in design techniques near transistor's active operation limit, f_{max}. In the following, we review these aspects of terahertz CMOS research in recent years.

2 Device characterization and modeling

2.1 De-embedding

Predictive circuit simulation is possible only if accurate device models are available. A device model is, at best, as accurate as the measurement data from which it is built. It is, therefore, very important that measurement data are reliable. Making measurements at high frequencies involves de-embedding of device characteristics from raw measurement data. At terahertz frequencies, not only does measurement uncertainty increase, also possible excitation of spurious electromagnetic modes can complicate the interpretation of measurement results. Many popular methods of de-embedding and models of pads used at low-GHz frequencies are inadequate at such high frequencies. Instead, the thru-reflect-line (TRL) algorithm is commonly used for characterizing transmission lines and also for subsequent de-embedding. It was recently shown that the lengths of line standards used in TRL have a great impact on the reliability of the extracted propagation constant, γ, of the line and de-embedding [3]. A typical longest line length that can be accommodated on a typical CMOS die of, say, 4 mm × 4 mm would be around 3 mm. The phase constant β can be extracted reliably from a line of that length, but the attenuation constant α can show erratic behavior above 200 GHz that is difficult to predict by electromagnetic (EM) simulation. On the other hand, if the longest line is as long as 8 mm, not only the phase constant but also the attenuation constant agree reasonably well with EM simulation up to 300 GHz. This is a recent finding that significantly improved reliability of transmission line characterization and device de-embedding [3].

2.2   Nonlinear transistor model

Device characterization at high frequencies is done primarily by measurement of scattering matrices or S parameters with a vector network analyzer (VNA). S parameters are linear responses of a device at the measurement frequency. Large-signal network analyzers that measure harmonic as well as fundamental responses are also available for low-GHz frequencies [4]. X-Parameters are one such proprietary framework for frequency-domain nonlinear measurement and simulation [5]. However, harmonic responses cannot currently be measured at terahertz frequencies. For one thing, the usable frequency ranges of terahertz waveguides are too narrow for harmonics to be handled. Typical measurement-based (as opposed to frequency-extrapolated) terahertz device models are small-signal models built from S parameters. But obviously, small-signal models are inadequate for simulating power amplifiers, oscillators and mixers. Actually, predictive nonlinear circuit simulation is a challenge at lower frequencies too. But millimeter-wave circuits operating below 100 GHz can be realized by overdesign even if the predictive ability of simulation is poor. On the other hand, at terahertz frequencies, transistor's gain is so limited and passive components are so lossy that there is very little room for overdesign. There, therefore, is much greater demand for accurate large-signal models. Study of nonlinear microwave characterization and modeling of transistors has focused mainly on compound semiconductor devices and high-voltage MOSFETs such as LDMOS (laterally-diffused MOS) FETs [6, 7]. The primary focus of highly miniaturized MOSFET modeling, on the other hand, has been compact and scalable models for digital circuits. Rather different approaches were taken to the modeling of microwave transistors and digital MOSFETs. Considerable effort remains to be put forth at adapting microwave-transistor modeling techniques to MOSFET modeling. Parasitic resistances at gate, source and drain measured at dc are not necessarily equal to those extracted from high-frequency measurements. Such seeming discrepancy must be appropriately characterized and modeled for fully predictive circuit simulation at different time scales [8].

2.3   Electromagnetic field simulation

Terahertz circuit design cannot be done with circuit simulation alone. EM field simulation is a must for predictive design. The free-space EM wavelength at 100 GHz is only 3 mm. The on-chip wavelength of around 1.5 mm (or shorter at higher frequencies) cannot be neglected even on a small chip, and circuits must be treated as distributed. The common layout parasitic extraction (LPE) used in RF circuit simulation ignores inductance and is inadequate for terahertz circuit simulation. EM field simulation is needed to design various passive millimeter-wave components as well as transmission lines. Just as predictive circuit simulation requires accurate device models, predictive EM field simulation requires accurate information about process parameters, including material parameters, layer thicknesses, and cross-sectional geometry of interconnects. CMOS foundries provide nominal values of most of these parameters. But permittivities of dielectrics they provide are usually frequency-independent real values. The assumption of frequency independence is not unreasonable, but the lack of information about dielectric loss is a problem. To perform EM simulation with reasonable predictive

power, material parameters (dielectric permittivities and metal conductivities) must be evaluated by measurement. The measurement data that can be used for this purpose are S parameters measured with a VNA. Several dielectric materials are used in modern CMOS interconnect layers. Since the designer must follow the restrictive CMOS design rules, it is not possible to design test structures that reveal material parameters of each individual material. The test structures should be chosen appropriately so that measured characteristics could be related straightforwardly to material parameters. Transmission lines used in TRL are ideally suited to this purpose because the extracted propagation constant directly reflects effective material parameters. These are effective parameters because multiple materials are involved and also actual geometrical parameters are not known exactly. By measuring a few different types of transmission line, effective material parameters can be estimated fairly reliably [9, 10].

3 Terahertz CMOS circuit design

3.1 Gain boosting in amplifiers

Terahertz circuits operate at frequencies that are much closer to MOSFET's f_{max} than usual. Typical RF and millimeter-wave circuits operate at below $f_{max}/4$ [11], whereas terahertz circuits often have to operate at around $f_{max}/2$ or higher. A common local feedback technique for gain boosting is to insert a positive reactance between the gate and drain of a MOSFET. This technique, known as neutralization, was originally proposed to cancel the unwanted internal feedback in a transistor and unilateralize the amplifier [12, 13]. The positive reactance can be realized most easily in a differential amplifier with a cross-coupled capacitor pair because the cross-coupled capacitance is, in differential mode, equivalent to negative capacitance [14]. It is known that by adopting cross-coupled feedback capacitance larger than the gate-drain capacitance, the gain can become higher than the unilateral gain. Essentially the same feedback can be achieved in single-ended amplifiers by transmission-line feedback [15]. That these apparently different feedback configurations are essentially the same can be seen within the framework of a general theory [16].

3.2 High-frequency generation

Near-f_{max} or above-f_{max} frequency generation requires frequency multiplication. An N-stage ring oscillator can generate Nth harmonic. The case of $N = 2$ is known as the push-push oscillator [17], and its output power is relatively large. The larger the value of N, the smaller the output power of the Nth harmonic. In CMOS terahertz circuits, the use of $N = 3$ (triple-push oscillator) is common. Since the output power of a single oscillator is small, power-combining techniques are often applied. When outputs from multiple oscillators are to be combined in parallel, the output signals must be in phase. One way to accomplish the mutual synchronization is to use injection locking [18]. Power combining can also be done spatially by appropriately disposing multiple terahertz sources and antennas, thereby avoiding power loss in power-combining passive components [19]. A loop of coupled and mutually injection-locked oscillator was recently proposed. A low phase noise of $-92\,dBc/Hz$ at 1-MHz offset from a 100-GHz carrier frequency was reported [20].

As indicated in these examples, significant progress has been made in making output power higher and phase noise lower.

3.3 On-chip power-line decoupling, planar circuits and antennas

Power-line decoupling for millimeter-wave circuits is much more challenging than for RF circuits because of the much wider operation frequency range. The use of decoupling capacitors can be problematic due to their low self-resonance frequency. A better alternative is to use as power lines a specially designed transmission line having extremely low characteristic impedance [21]. It was recently demonstrated that such a power line's input impedance does stay as low as $1\,\Omega$ up to $170\,\text{GHz}$ and below $2\,\Omega$ up to $325\,\text{GHz}$ [22, 23].

In millimeter-wave CMOS circuits, baluns and other coupled- or uncoupled-transmission line-based components are used, as well as ordinary capacitors and inductors. In addition, as the frequency becomes higher, more extensive use is made of planar circuit components and techniques. For example, mixed use of slotlines and microstrips, a known technique in microwave printed circuit boards (PCBs), is now made in CMOS integrated circuits [24]. The use of hollow waveguides in integrated circuits is also being investigated [25]. Research on such unconventional techniques is very active. On-chip antennas are also becoming increasingly common. CMOS on-chip antennas tend to be significantly lossier than off-chip antennas due to the presence of silicon substrate. However, it is difficult to realize low-loss wired connection to off-chip components at terahertz frequencies, and on-chip antennas are used to solve that problem [26, 27].

3.4 Transceivers

Combination of various terahertz techniques sketched above culminated in CMOS transceivers operating at carrier frequencies of $100\,\text{GHz}$ or higher. For example, Wang et al. reported a 210-GHz transceiver in 32-nm SOI CMOS [27]. Park et al. demonstrated a 260-GHz transceiver in 65-nm CMOS [26]. Chen et al. proposed and demonstrated an orthogonal-modulation transceiver architecture in 40-nm CMOS that allows the use of frequency multipliers by separating I and Q channels. The transmitter has separate I- and Q-channel antennas, and orthogonally modulated signal is synthesized spatially along the propagation path [28]. A QPSK transmitter architecture that uses a tripler to modulated signals was proposed in [29]. When frequency multiplication is applied to orthogonally modulated signals, the signal constellation gets corrupted in general, causing difficulty in modulation/demodulation and low signal-to-noise ratio. But in the case of frequency tripling applied to a QPSK-modulated signal, the signal constellation undergoes a transformation but the result is still a QPSK constellation, thereby simplifying the transceiver design.

4 Outlook

Throughout the history of CMOS RF circuit evolution, device performance improvement due to technology scaling or device miniaturization contributed so much to circuit performance improvement that, arguably, the excellence of design

hasn't played as important a role in shaping the long-term trend of continued performance growth. But now that it is becoming more and more difficult to enjoy the fruit of miniaturization as far as raising the operation frequency is concerned, design techniques built upon firm circuit theoretic, electromagnetic, or algorithmic foundations is assuming greater importance. The recent efforts at realizing terahertz CMOS circuits near f_{max}, reviewed above, can be seen as a reflection of the qualitative shift in technological trend: a departure from device-performance-powered design. And that departure will contribute to keeping the technological trend at a higher level, the continued exponential growth (Moore's law and its direct and indirect corollaries).

The demand for possible main terahertz applications of ultra-high-speed communication, sensing and imaging, which require high-performance digital blocks, could grow to a point where mass production with a state-of-the-art CMOS process is desirable. Even if so, given the fact that the growth of CMOS f_{max} is slowing down, the development of near-f_{max} design technology will remain important in the foreseeable future. CMOS millimeter-wave circuits have been developed based mainly on the traditional lumped-circuit design approach with some distributed or electromagnetic corrections. But there are a wealth of design concepts developed by microwave and antenna engineers, still unexplored yet broadly applicable to CMOS terahertz design. Collaborative efforts by CMOS designers and microwave and antenna engineers will most certainly accelerate the development and unearthing of full potential and impacts of terahertz CMOS.

Acknowledgments

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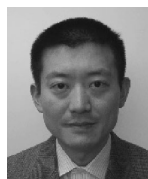
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