

A highly sensitive wide-range weak current detection circuit for implantable glucose monitoring

Xi Tan, Sizheng Chen, Xiao Yan, Yibo Fan, Hao Min,
and Junyu Wang^{a)}

State Key Lab of ASIC & Systems, Fudan University,

Shanghai 201203, People's Republic of China

a) junyuwang@fudan.edu.cn

Abstract: A highly sensitive weak current detection circuit for implantable glucose monitoring is presented. The circuit consists of a current splitter, an integrator, a sampling/holding (S/H) circuit, and an 8-bit successive approximation register (SAR) analog-to-digital convertor (ADC). T-switches, source voltage shifting and correlated double sampling (CDS) technology are adopted to reduce the effects of leakage currents, charge injection, dc offset and low-frequency 1/f noise. The work range is divided into 5 sub-ranges to reduce the complexity and power consumption of current detection. The chip was fabricated with 0.13 μm CMOS technology. Test results show that the circuit can detect weak signal from 10 fA to 1 nA with 1.5 V supply and 7.2 μW power consumption. The tested leakage current of the design is 4 fA.

Keywords: implantable, weak current measurement, SAR ADC, correlated double sampling

Classification: Integrated circuits

References

- [1] J. Brauker: *Diabetes Technol. Ther.* **11** (2009) 25. DOI:10.1089/dia.2008.0137
- [2] C. Yang, Y. Huang, B. Hassler, R. Worden and A. Mason: *IEEE Trans. Biomed. Circuits Syst.* **3** (2009) 160. DOI:10.1109/TBCAS.2009.2015650
- [3] M. M. Ahmadi and G. A. Jullien: *IEEE Trans. Biomed. Circuits Syst.* **3** (2009) 169. DOI:10.1109/TBCAS.2009.2016844
- [4] R. Steadman, G. Vogtmeier, A. Kemna, S. E. I. Quossai and B. J. Hosticka: *IEEE J. Solid-State Circuits* **41** (2006) 1615. DOI:10.1109/JSSC.2006.873679
- [5] V. Shenoy, S. Jung, Y. Yoon, Y. Park, H. Kim and H. Chung: *IEEE Sensors J.* **14** (2014) 1591. DOI:10.1109/JSEN.2014.2300475
- [6] D. Kim, B. Goldstein, W. Tang, F. Sigworth and E. Culurciello: *IEEE Trans. Biomed. Circuits Syst.* **7** (2013) 52. DOI:10.1109/TBCAS.2012.2192273
- [7] L. Zhang and Z. Yu: *IEEE International Conference on Electronics, Circuits and Systems (ICECS)* (2007) 1304. DOI:10.1109/ICECS.2007.4511237
- [8] S. Guan, J. Gu, Z. Shen, J. Wang, Y. Huang and A. Mason: *IEEE Biomedical Circuits and Systems Conference* (2011) 193. DOI:10.1109/BioCAS.2011.6107760
- [9] H. M. Jafari, K. Abdelhalim, L. Soleymani, E. H. Sargent, S. O. Kelley and R.

- Genov: IEEE J. Solid-State Circuits **49** (2014) 1223. DOI:10.1109/JSSC.2014.2312571
- [10] L. Junjie and J. Holleman: Custom Integrated Circuits Conference (2012) 1. DOI:10.1109/CICC.2012.6330668
- [11] M. Stanacevic, K. Murari and A. Rege: IEEE Trans. Biomed. Circuits Syst. **1** (2007) 63. DOI:10.1109/TBCAS.2007.893176
- [12] K. Ishida and K. Kanda: IEEE J. Solid-State Circuits **41** (2006) 859. DOI: 10.1109/JSSC.2006.870761

1 Introduction

Different from the traditional finger prick test, wireless implantable glucose detection can make it feasible to continuously monitor glucose level [1]. The Faradic current of an amperometrical enzymatic sensor can be estimated by [2]:

$$I = AnF\Gamma T \quad (1)$$

where A is the electrode area, n is the number of electrons involved in the reaction, F is Faraday's constant, Γ is the surface coverage density of the enzyme, and T is the turnover rate. Since the area of a glucose sensor may vary by several orders of magnitude when using a conventional electrode of millimeters and a microelectrode of tens of microns in diameters, the area of a glucose sensor may vary by several orders of magnitude, thus the detection circuit needs to adapt to the sensor by having a wide detection range [3]. Therefore, a highly sensitive wide-range weak current detection circuit is necessary for implantable glucose monitoring.

Weak current can be handled by circuits of different types, such as current to frequency/time convertor [3], current-mode amplifier (I-to-I) [4], resistive feedback [5], and capacitive feedback [6]. Current to frequency/time convertor can reduce the complexity and power dissipation, but it is normally used to measure current larger than several nano-amperes. A current-mode pre-amplifier can achieve a dynamic range of 20 bits and consume 1 nA of DC quiescent current [7]; but the sensitivity is within the range of several pico-amperes because of larger offset and the noise of MOSFETs working in subthreshold region.

In this work, a switched capacitor (SC) circuit with five integrating sub-ranges is proposed to realize wide-range current detection. Noise of the circuits and non-ideal effects of switches are taken into account during the weak current detection. T-switches and source voltage shifting technology are used to reduce the effects of leakage currents, charge injection. CDS technology is adopted to reduce DC offset and low-frequency $1/f$ noise.

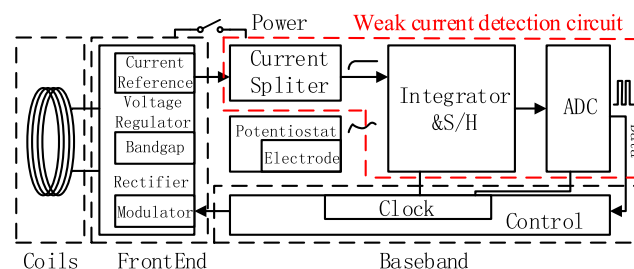


Fig. 1. Architecture of the wireless implantable RFID tag.

2 System architecture

The weak current detection circuit is a part of a wireless implantable radio frequency identification (RFID) tag working in 13.56 MHz frequency [8], as shown in Fig. 1. The tag receives energy through interactions between the reader antenna and the tag antenna. The radio-frequency (RF) frontend and the analog frontend of the sensor tag rectify the power from the reader and generate the reference voltage for the current detection circuit. The baseband processes the RFID protocol and coordinates working modules in the tag.

As shown in Fig. 2, the glucose sensor readout circuit is composed of a potentiostat, three sensor electrodes and weak current detection circuit. The potentiostat generates a desired potential difference between the working electrode (WE) and the reference electrode (RE) for the redox reaction by injecting the proper amount of current into the counter electrode (CE) [3]. The weak current detection circuit consists of a current splitter, an integrator, an S/H circuit and an 8-bit SAR ADC. In this work, an on-chip current splitter is implemented for calibration and testing purpose. The current splitter can produce current from several femto-amperes to one nano-ampere. With this current splitter, the weak current detection test can be completed in an internal on-chip environment and thus refrain from the disadvantages of using off-chip current sources.

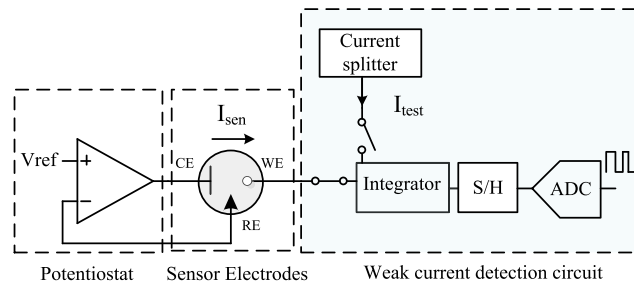


Fig. 2. Block diagram of the glucose sensor readout circuit.

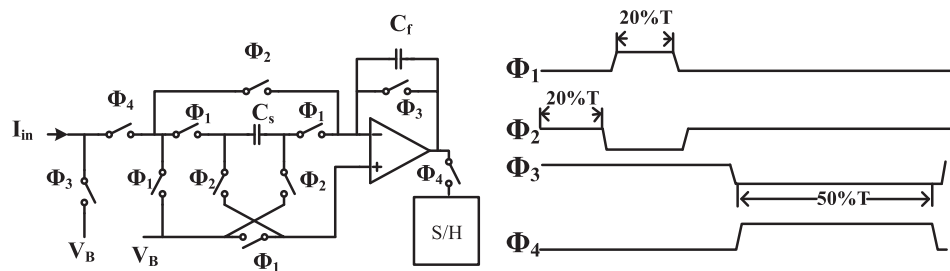


Fig. 3. Schemes of integrator circuit and clock signal

3 Circuit implementation

3.1 Integrator

The integrator is comprised of a pre-amp for integration and 11 switches for CDS controlling, as shown in Fig. 3. I_{in} represents the current acquired from the glucose sensor or from the current splitter. The switches are controlled by the clocks Φ_1 , Φ_2 ,

Φ_3 and Φ_4 . Two-phase non-overlapping clocks are designed to release the charge injection effect.

Under the control of switches, the integrator works in the reset state or the integration state. In the reset state, the $1/f$ noise and offset of the op-amp are sampled by C_s . The C_s is then flipped over and connected to the equivalent voltage and offset as the noise. As a result, the noise and the offset are eliminated. In the integration state, the C_f is charged by current under measure. Let the integrating period be T and the duty cycle be 50%, the output voltage of the circuit is:

$$V_{out} = \frac{I_{sen}}{C_f} \times \frac{T}{2} \quad (2)$$

To reduce power consumption and complexity of the circuit, instead of using a very high-resolution ADC, the integrator is designed to work in 5 sub-ranges with different values of T : 10 fA–100 fA, 100 fA–1 pA, 1 pA–10 pA, 10 pA–100 pA, and 100 pA–1 nA. For example, with $T = 2$ s, current range of 10 fA–100 fA is amplified and transformed to 0.1–1 V at the output port of integrator. A selection circuit has been designed to detect signals within different sub-ranges.

In the reset state, since the sensor and the integrator is disconnected, the noise sources can be depicted as:

$$\overline{V_{n,OUT}^2} = \overline{V_{n,amp}^2} + kT/C_f \quad (3)$$

where $V_{n,amp}$ is the input-referred noise of the amplifier including $1/f$ noise and thermal noise. kT/C_f represents switch resistance's thermal noise which accumulates on the integrating capacitor (C_f). Because a larger C_f induces less kT/C_f noise but needs a longer integrating period, it consumes more power. A 200 fF C_f is selected considering the tradeoffs. Note that $1/f$ noise of the amplifier is reduced by the CDS module before the integration stage.

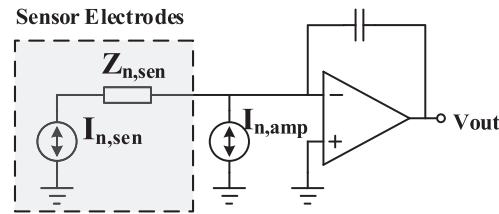


Fig. 4. Equivalent noise model of sensor and the integrator

In the integration stage, the noise of the sensor must be considered in the noise equivalent circuit, as shown in Fig. 4. $I_{n,sen}$ represents the noise current of sensor, $I_{n,amp}$ represents the input-referred noise current of the amplifier, and $Z_{n,sen}$ represents the simplified impedance of the sensor. The integrated noise on the C_f can be calculated through:

$$\overline{I_{n,IN}^2} = \overline{I_{n,sen}^2} + \overline{I_{n,amp}^2} \quad (4)$$

$$\overline{I_{n,sen}^2} = 2 \cdot q \cdot I_{sen} \quad (5)$$

$$\overline{I_{n,amp}^2} = 4kT\gamma \cdot 2g_{m,IN} + 2 \frac{K}{C_{ox} \cdot f} \frac{g_{m,IN}^2}{W_{IN}L_{IN}} \quad (6)$$

The $I_{n,sen}$ mainly includes shot noise which is proportional to the sensor current. The $I_{n,amp}$ consists of $1/f$ noise and thermal noise. Two large $W * L$ input MOSFETs in the pre-amp are used to reduce both $1/f$ noise and thermal noise.

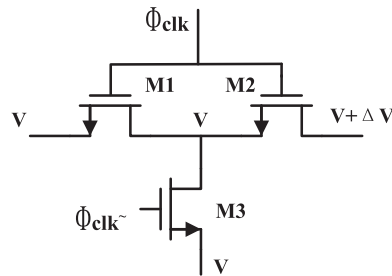


Fig. 5. Schematic of T-switch

A T-switch, as shown in Fig. 5, between the negative input port and the output port of the pre-amp is used to minimize the leakage currents in the MOSFET switch. The T-switch is necessary since the drain-to-source leakage current of a normal MOSFET switch working in weak inversion can be larger than the detected current during the “off” state with a large drain/source voltage [12]. Simulation results show that the drain-to-source leakage current of the designed T-switch can be as low as sub-fA. Furthermore, the width of the MOSFETs used in the T-switch is minimized to reduce the reverse leakage area of the source and drain. The reverse diode leakage current of every drain or source diffusion is several aA which is negligible for the detection circuit.

3.2 S/H circuit

Since the output waveform of the integrator is a triangular wave and cannot be sampled by the ADC directly, an S/H circuit is added between the integrator and the ADC, as shown in Fig. 4. CDS technology is also adopted in the S/H module to reduce the $1/f$ noise and the DC offset of the amplifier. The clock signal is described in Fig. 6.

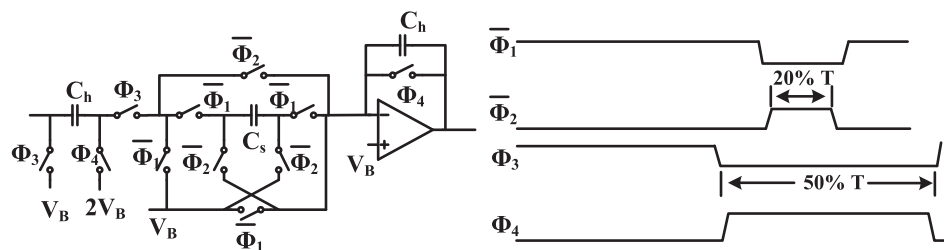


Fig. 6. Schemes of S/H circuit and clock signal

3.3 SAR ADC

The SAR ADC consists of sample-and-hold (S/H) switches, a binary-weighted DAC, a dynamic comparator and a successive approximation register logic con-

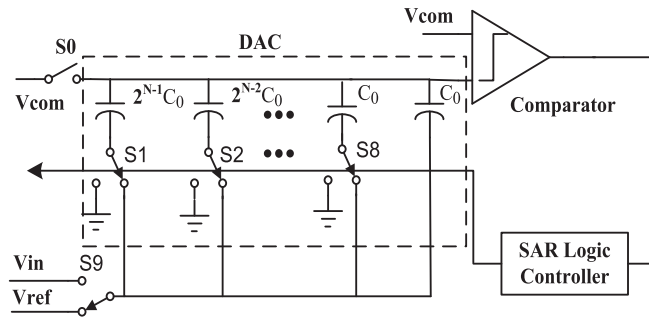


Fig. 7. Architecture of SAR ADC.

troller, as shown in Fig. 7. All switches in the ADC are implemented by passive complementary NMOS and PMOS which meet the accuracy needs for 8-bit resolution. In the SAR ADC, all the circuit components are implemented as single-ended structures instead of fully-differential structures, in order to save power.

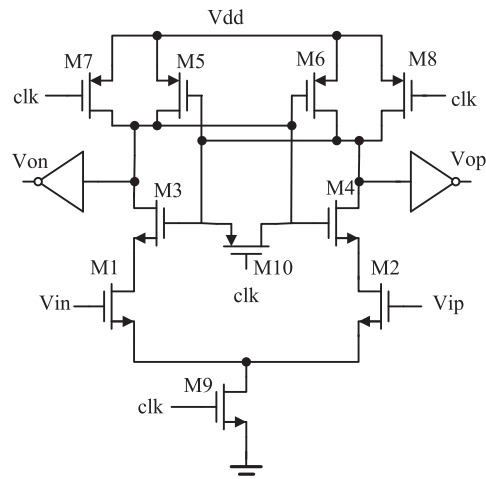


Fig. 8. Dynamic comparator circuit.

A proposed low-power and low-offset dynamic comparator is implemented in this work, as shown in Fig. 8. A dynamic comparator consumes no static current and very little dynamic power. The comparator has two operation phases: the reset phase and the comparison phase. When clock is at the low level, the comparator is in the reset phase. The nodes Vop and Von are reset to ground. The comparator consumes no static power because that the tail NMOS M9 is off. M10 is inverted to avoid hysteresis of the previous clock period. When clock is at the high level, the comparator is in the comparison phase. The node voltages of M3 and M4's drain get lower at unequal rates because of the differential stimulus input signals Vip and Vin. Then the positive feedback M4–M6 evaluates the distinction of node voltages of M3 and M4's drain and latches the comparator. When the output of comparator is stable, no DC current flows from Vdd to ground.

The DAC in the SAR ADC is as shown in Fig. 7. Switches S0–S9 are controlled by the signals generated by the SAR logic controller and the binary-

weighted capacitor is constructed from unit capacitor C_0 . The value of the C_0 should be balanced between power, area, noise and mismatch.

The binary-weighted switched-capacitor array consumes little power and occupies small silicon area. On the other hand, it suffers from larger DNL and INL errors by nature. In this work, a metal-insulator-metal (MIM) unit capacitor of 40 fF is implemented to reduce power consumption and mismatch. In this situation, thermal noise kT/C of the capacitor array has very little effect on the resolution of the DAC.

4 Test result

The implantable current detection circuit was fabricated in $0.13\text{ }\mu\text{m}$ CMOS technology. The size of the chip is $1.2 \times 1.8\text{ mm}^2$, as shown in Fig. 9.

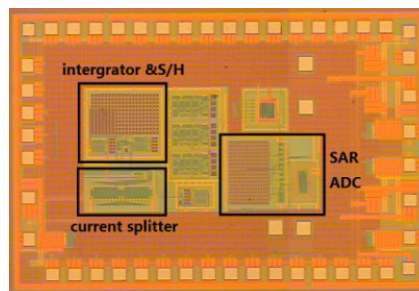
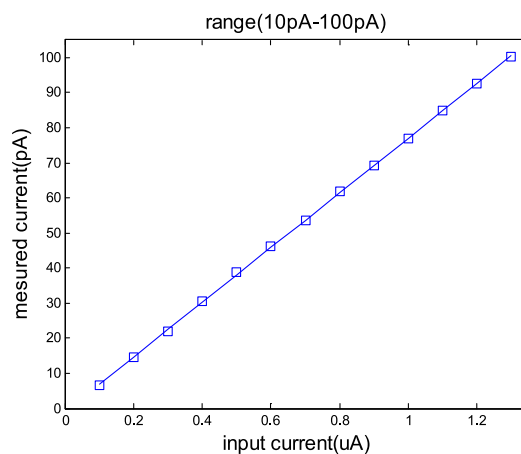


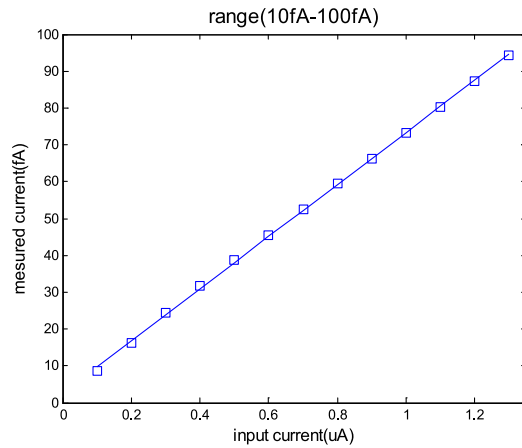
Fig. 9. Die micrograph of the weak current detection circuit.

4.1 Current splitter and integrator test

An accurate off-chip reference current flows into the on-chip current splitter which produces five sub-range weak currents. The current measurement circuit can work in two modes: the calibration mode and the measurement mode. The measured currents in the sub-range of 10 pA–100 pA and 10 fA–100 fA are shown in Fig. 10(a) and (b).



(a) 10pA-100pA branch



(b) 10fA-100fA branch

Fig. 10. Measured current of two branches of the Current Splitter vs. input reference currents: (a) 10 pA–100 pA branch, (b) 10 fA–100 fA branch.

When the reference current of the current splitter is fixed, test results show that the output current of the last four branches is progressively attenuated by about 10, as shown in Fig. 11. When changing the input reference current from 0.2 μA to 1 μA with a step of 0.1 μA , the measurement results show that the splitter and readout circuit keep good linearity, as shown in Fig. 8.

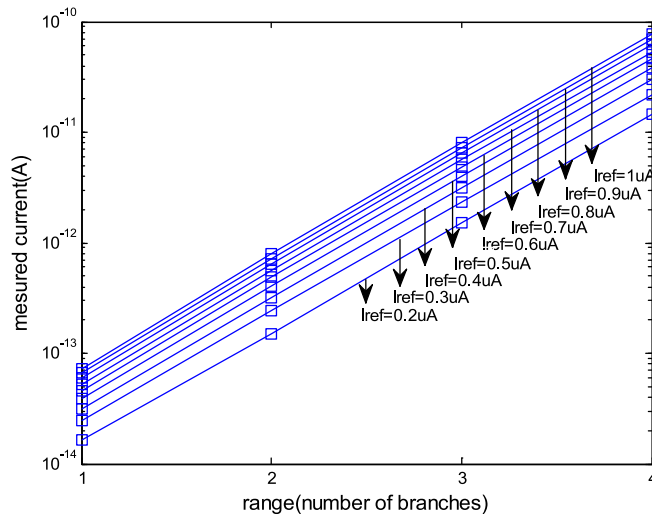


Fig. 11. Measured current of different branched with same input reference input current.

4.2 SAR ADC test

A full scale 9.37 kHz sinusoidal wave spectrum measured at 100 kHz sampling rate is shown in Fig. 12. The signal-to-noise distortion ratio (SNDR) is 49.2 dB and the spurious free dynamic range (SFDR) is 63 dB. In addition, the effective number of bit (ENOB) is 7.8 bits.

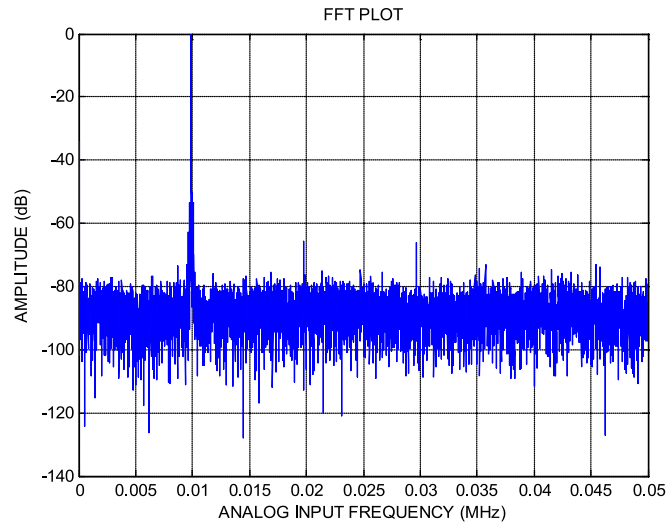
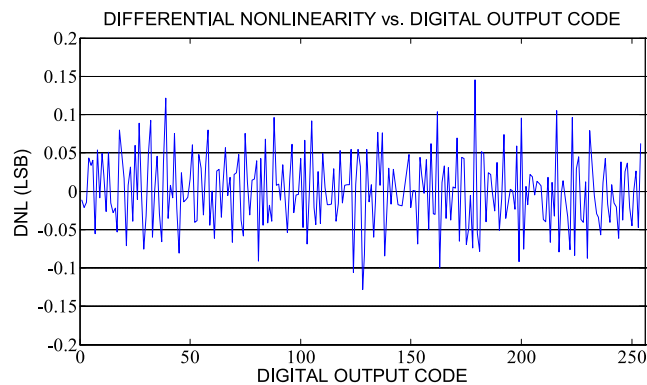
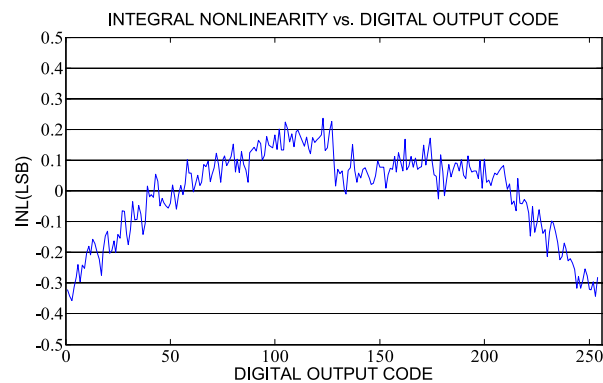


Fig. 12. Measured output spectrum of SAR ADC with full-scale 9.37 kHz sinusoidal input waveform.

Fig. 13(a) and (b) illustrate the measured differential nonlinearity (DNL) and the integral nonlinearity (INL). The input signal with 377 Hz and 1.2 V_{pp} sinusoidal wave is fed into the SAR ADC with the sampling rate of 100 kHz. The measured results show that DNL is in the range of $-0.15/+0.15$ LSB whereas the INL is within $-0.35/+0.23$ LSB. The performance of this work is compared to other reported implementations (Table I).



(a) DNL



(b) INL

Fig. 13. Measured DNL and INL of the SAR ADC: (a) DNL, (b) INL.

Table I. Comparison of weak current detection circuit

	This work	[9]	[10]	[11]
Technology	0.13 μm	0.13 μm	90 nm	0.5 μm
Detection range	10 fA~1 nA	8.6 pA ~ 350 nA	75 fA ~ 200 pA	-100 nA ~ 100 nA
Min. current	4 fA	8.6 pA	75 fA	50 fA
Sample rate	100 KS/s	10 KS/s	2 KS/s	250 KS/s
Power	7.2 μW	42 μW	147 μW	11.42 μW

5 Conclusion

A highly sensitive wide-range weak current detection circuit used for a wireless implantable RFID tag is proposed and manufactured in 0.13 μm CMOS technology. Five integrating sub-ranges are designed in the switched-capacitor (SC) integrator to extend the work range with low complexity and cost. CDS technology is used to reduce noise and offset of the pre-amp. An on-chip test based on an embedded current splitter shows that the detection circuit has a good linearity from 10 fA to 1 nA and consumes 7.2 μW . The tested leakage current of the design is 4 fA. The detection range can be tailored to the current output range of implantable glucose sensors by choosing appropriate sub-range integrators.

Acknowledgments

This work has been supported by the National Science & Technology Pillar Program of China (2015BAK36B01), the National Natural Science Funds of China (61076022, 61211140046) and the Shanghai Pujiang Program.