

Importance of Si surface flatness to realize high-performance Si devices utilizing ultrathin films with new material system

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Abstract: The importance of Si surface flatness on metal-oxide-semiconductor field-effect transistor (MOSFET) characteristics with ultrathin hafnium oxynitride (HfON) high-k gate insulator formed by electron cyclotron resonance (ECR) plasma sputtering was described. The surface roughness of Si substrate was reduced by Ar/4.9%H₂ annealing utilizing conventional rapid thermal annealing (RTA) system. Si surface root-mean-square (RMS) roughness was well controlled by changing the annealing temperature from 700 to 1000°C. Si surface RMS roughness after 1000°C/1 hr annealing was 0.078 nm for Si(100) and 0.082 nm for Si(110), respectively. Clear dependence of electrical characteristics of MOS diodes such as equivalent oxide thickness (EOT) and leakage current on the surface RMS roughness of Si(100) and Si(110) was observed, and the electrical characteristics were remarkably improved by decreasing of surface RMS roughness. The MOSFET characteristics with HfON gate insulator fabricated on Si(100) substrates after flattening process were also improved.

Keywords: new materials, high-k, HfON, Si surface flatness, Ar/4.9%H₂ anneal, ECR plasma sputtering

Classification: Electron devices, circuits, and systems

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1 Introduction

The metal-oxide-semiconductor field-effect transistors (MOSFETs) have been aggressively scaled down to 50 nm or beyond [1, 2]. With the device scaling, for example, thinner gate insulator will be required such as less than 0.5 nm of equivalent oxide thickness (EOT) or below [1]. In order to realize the adequate scaled device, various new materials have been introduced in the scaled MOSFETs [2, 3]. Fig. 1 shows a schematic cross-section of n-channel MOSFET. Conventional SiO₂ (relative dielectric constant: $\epsilon_r = 3.9$) gate insulator will be replaced by high dielectric constant (high-k) materials ($\epsilon_r > 3.9$, e.g. HfO₂, La₂O₃, Al₂O₃ etc.) to make the EOT smaller with

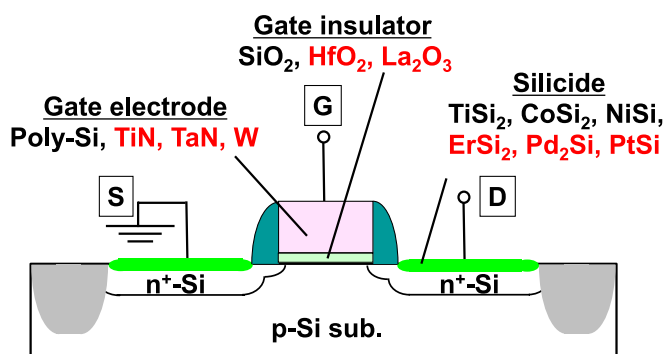


Fig. 1. New materials in scaled MOSFETs.

increase of physical thickness compared that of SiO_2 to decrease the gate leakage current [3, 4, 5, 6]. Metal gate electrodes (e.g. TiN, TaN, W, Pt, Ir etc.) will be introduced instead of heavily doped poly-Si gate electrode to suppress the depletion which leads to the increase of EOT [3, 7]. Various metal gate/high-k gate stack structures have been reported so far, and ultra-thin EOT of 0.2 nm has been achieved [4]. In order to reduce the contact resistivity at the source/drain (S/D) regions, silicide materials which have low Schottky barrier height, both for n-Si and p-Si, should be introduced instead of conventional NiSi (e.g. YSi_2 , ErSi_2 , YbSi_2 , Pd_2Si , PtSi etc.) [8, 9, 10, 11, 12, 13]. The dopant segregation process at the silicide/Si interface is also useful to reduce the contact resistivity [14, 15]. The contact resistivity of $10^{-9} \Omega \text{ cm}^2$ or below has been reported utilizing ErSi_2 for n-Si and Pd_2Si for p-Si [16]. Further improvement of MOSFET performances would be achieved by using the investigated technologies.

One of the most important issue to introduce new materials into the MOSFETs is the thin film formation. The film thickness becomes thinner especially for the gate insulator so that the surface roughness of Si substrate and also gate insulator should be decreased to improve the electrical characteristics. In international technology roadmap for semiconductors (ITRS), EOT below 0.5 nm is required in 2026 [1]. Therefore, high-k materials should be introduced instead of conventional SiO_2 gate insulator. Many institutions have reported so far the Si surface flattening process [17, 18, 19, 20], and MOSFETs with atomically flat interface at Si/gate insulator show higher performances than those with conventional devices [21, 22, 23, 24]. The 1/f noise in MOSFETs with Si/high-k gate stacks has also been reported [25, 26]. However, there have been few report for the influence of Si surface roughness on the high-k gate insulator formation.

In this paper, recent results for the influence of Si surface roughness on electrical characteristics of hafnium oxynitride (HfON) high-k gate insulator are described as one of the example for the introduction of new materials into Si-MOSFETs. Si(100) and Si(110) surface flattening process utilizing Ar/4.9% H_2 annealing is described in Section 2. The electrical characteristics of MOS diodes with HfON thin films formed by electron-cyclotron-resonance (ECR) plasma sputtering on Si(100) and Si(110) substrates are described in

Section 3. The effect of Si surface flattening on MOSFET characteristics fabricated on Si(100) substrate with HfON gate insulator is described in Section 4. Finally, the paper is concluded in Section 5.

2 Si(100) and Si(110) surface roughness reduction by Ar/4.9%H₂ annealing for 3-dimensional gate structures

In this section, surface roughness reduction of Si(100) and Si(110) substrates utilizing Ar/4.9%H₂ forming gas annealing with conventional rapid thermal annealing (RTA) system is discussed. The role of the H₂ in the forming gas is mainly to suppress unintentional oxidation caused by the residual oxygen in the RTA system, and also the enhancement of surface migration. In the scaled MOSFETs, 3-dimensional (3D) gate structures such as FinFETs would be introduced [2]. For the 3D gate structures, not only the Si(100) surface but the other surface orientation such as Si(110) would be used to improve the device characteristics. Therefore, the surface flattening process for various surface orientations is necessary to be investigated. For the surface flattening of 3D structures, flattening by the thermal oxidation process is not able to be applied [17]. The flattening by the annealing in pure Ar or H₂ ambient requires a special pumping system or a secure system [18, 19]. Therefore, Ar/4.9%H₂ annealing was investigated utilizing a conventional RTA system.

The flattening process is as follows [27]. Si(100) and Si(110) (p-type) substrates were cleaned by sulfuric peroxide mixture (SPM), diluted hydrofluoric acid (DHF) and rinse in ultra-pure water (ORGANO I). Then, the substrates were annealed in the RTA (ULVAC VHC-P610) system with Ar/4.9%H₂ ambient (1 SLM) at 700–1000 °C for 1 hr. The Si surface roughness was observed by non-contact mode atomic force microscopy (AFM, Park systems Xe-100, scan size: 3 × 3 μm²). Fig. 2 shows the Si surface root-mean-square (RMS) roughness dependence on the Si annealing temperature. As shown in Fig. 2, in case of Si(100), the RMS was 0.2 nm for the surface of w/o annealing, and it was decreased to 0.078 nm after 1000 °C annealing. Interestingly, the surface roughness of Si(110) was also decreased from 0.22 nm (w/o) to 0.082 nm (1000 °C) as well as Si(100). Si(110) surface is known as easy to be rough especially by the wet process. In Fig. 2, the RMS roughness of Si(110) w/o annealing was high compared to Si(100). This is probably caused by the influence of wafer cleaning processes. However, the surface roughness was able to be decreased by the Ar/4.9%H₂ annealing even for the Si(110) surface. This flattening process is promising especially for the 3D gate structures. Furthermore, it was found that the RMS roughness of Si surface was linearly decreased with the annealing temperature. Therefore, it is able to control the surface RMS roughness by changing the annealing temperature.

Fig. 3 shows annealing temperature dependences on the RMS, average roughness (R_a) and maximum roughness (R_{max}) of the Si(100) surface. As shown in Fig. 3, not only the RMS but the R_a and R_{max} were well decreased with annealing temperature. It should be noticed that the large R_{max} of 1.3 nm obtained for the as-cleaned Si(100) surface was significantly decreased, and it

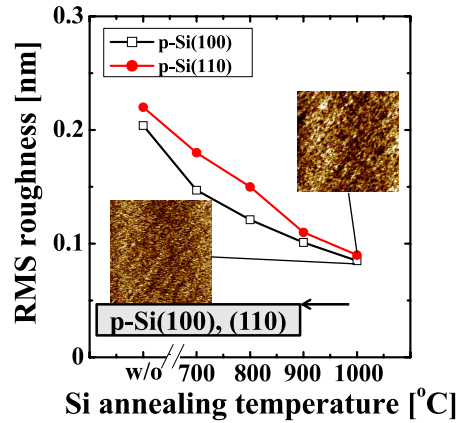


Fig. 2. Comparison of Si(100) and Si(110) RMS roughness dependence on Si annealing temperature. Annealing duration was 1 hr. AFM images of Si(100) and Si(110) after 1000 °C Ar/4.9% H_2 annealing were shown as insets. The scan size is $3 \times 3 \mu m^2$.

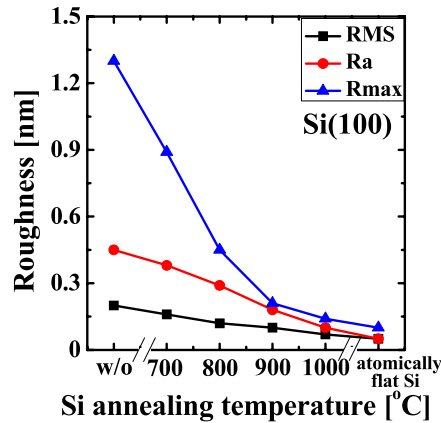


Fig. 3. RMS, R_a and R_{max} of Si(100) surface dependences on Si annealing temperature. Annealing duration was 1 hr. The scan size is $3 \times 3 \mu m^2$.

became close to the R_a in case the annealing temperature was 900–1000 °C. R_a value seems to strongly depends on the R_{max} so that the R_a value was large compared to RMS for the Si(100) surfaces annealed at 800 °C or below, while it became close to the RMS value by the annealing at 900–1000 °C. On the other hand, the RMS value seems to be linearly decreased with the annealing temperature as shown in Fig. 2 and Fig. 3. Therefore, RMS is a suitable parameter to evaluate the surface roughness dependence on the electrical characteristics of the devices. The roughness values obtained by 1000 °C annealing are close to the atomically flat surface although the RMS value is slightly high compared to the value of atomically flat Si (RMS: 0.047 nm) which was provided by Tohoku University [20].

In the next section, the surface RMS roughness dependence on the HfON thin film formation will be described.

3 Importance of Si surface flatness for the electrical characteristics of MOS diode with high-k HfON thin films

Among the various high-k materials, Hf-based high-k dielectric [4, 28, 29, 30] especially for hafnium oxynitride (HfON) is one of the most promising candidate material [31, 32, 33, 34]. In this section, the dependence of Si(100) and Si(110) surface roughness on the electrical characteristics of HfON gate insulator is described [27]. HfON gate insulator was formed by Ar/O₂ plasma oxidation of HfN film to suppress the interfacial layer (IL) formation. After the Si surface flattening process mentioned in Section 2, HfN (2 nm, Hf:N = 1:1) layer was deposited at room temperature (RT) by ECR plasma sputtering (0.17 Pa, Ar/N₂: 20/1 sccm, μ -wave/RF: 500/500 W). In order to form HfON gate insulator, *in-situ* ECR Ar/O₂ plasma oxidation (0.1 Pa, Ar/O₂: 10/4 sccm, μ -wave: 300 W, RT) was carried out. After the *in-situ* plasma oxidation, 600 °C silicon-wafer-covering post deposition annealing (SWC-PDA) was carried out for 1 min in N₂ ambient (30 SLM) [27]. The HfON thickness and atomic concentrations were approximately 3.8 nm and Hf:O:N = 3:6:1, respectively. Finally, Al electrodes were formed by thermal evaporation. The electrical characteristics of fabricated MOS diode were evaluated by capacitance-voltage (C-V, Agilent 4284A) and current density-voltage (J-V, Agilent 5156C) measurements. The physical thickness and atomic concentrations of the films were evaluated by ellipsometer (JASCO, ELC300) and x-ray photoelectron microscopy (XPS, ULVAC PHI5000), respectively.

Fig. 4 shows the surface RMS roughness of HfON formed on Si(100) and Si(110) substrates dependence on Si annealing temperature. The HfON surface roughness was also found to strongly depend on Si surface roughness. The RMS roughness of 0.16 nm (w/o) decreased to 0.06 nm after 1000 °C annealing in case of Si(100), and 0.18 nm (w/o) decreased to 0.07 nm in case of Si(110). The surface of HfON films was relatively flat even after 600 °C PDA both on

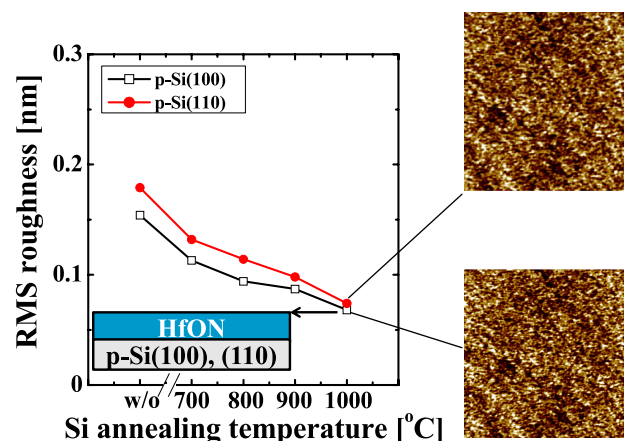


Fig. 4. Comparison of HfON RMS roughness dependence on Si annealing temperature. Annealing duration was 1 hr. AFM images of HfON formed on Si(100) and Si(110) after 1000 °C Ar/4.9% H₂ annealing were shown. The scan size is 3 × 3 μ m².

Si(100) and Si(110). The RMS roughness of HfON surface became smaller compared to Si surface probably caused by the surface migration during the HfN deposition and/or PDA. From the C-V and J-V characteristics of the Al/HfON/p-Si(100) MOS diodes [not shown], it is found that the EOT and leakage current density was remarkably decreased by the Si surface roughness reduction. Flat-band voltage shift (ΔV_{FB}) and the hysteresis width in C-V characteristics also became small. The improvement of electrical characteristics is attributed to the Si surface roughness reduction. In order to evaluate the dependence of electrical characteristics on Si surface roughness, typical parameters extracted from C-V and J-V characteristics are plotted as a function of Si surface RMS roughness.

Figs. 5(a)–5(c) show the EOT, J_g (at V_{FB} -1 V) and density of interface states (D_{it}) (extracted by Terman method) dependences on Si surface RMS roughness, respectively. It is found that EOT, J_g and D_{it} show clear dependences on Si surface RMS roughness not only for Si(100) but for Si(110) substrates. As shown in Figs. 5(a) and 5(b), EOT and J_g were remarkably decreased by Ar/4.9% H_2 (1000 °C) flattening process to 0.79 nm ($\epsilon_r = 19$) and 3.5×10^{-3} A/cm² for Si(100), and 0.82 nm ($\epsilon_r = 18$) and 7.8×10^{-3} A/cm² for

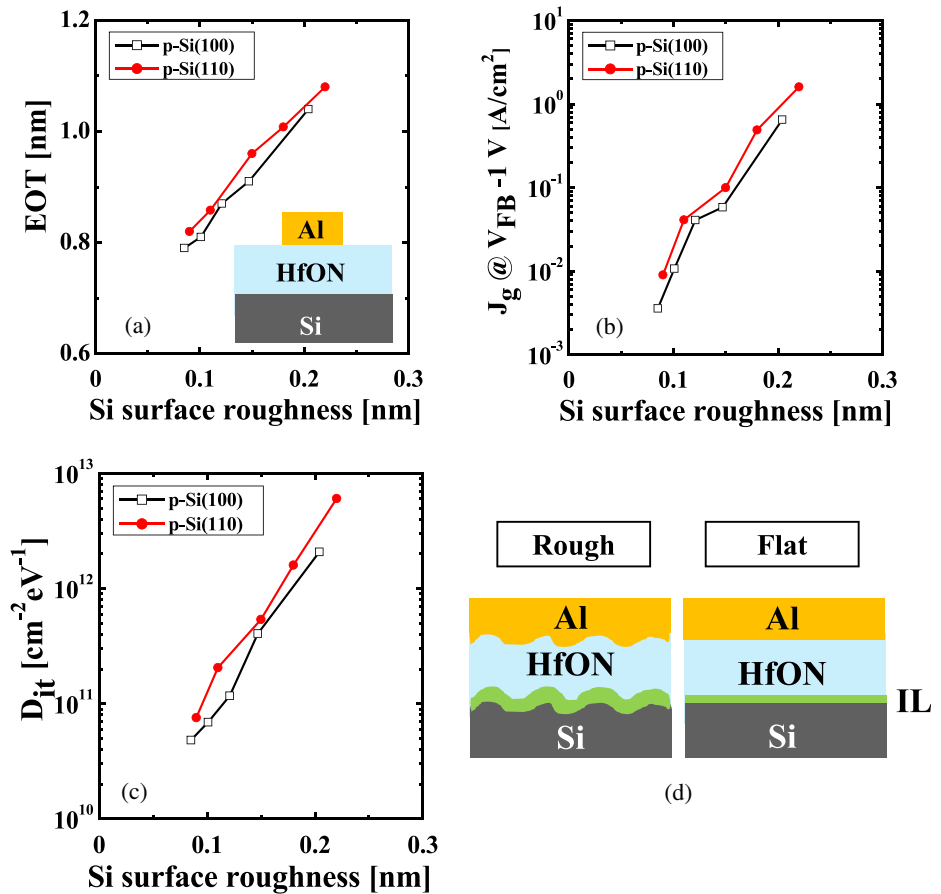


Fig. 5. (a) EOT (inset is a schematic cross-section of the fabricated MOS diodes), (b) J_g (at V_{FB} -1 V) and (c) D_{it} dependences on Si surface RMS roughness. (d) Schematic cross-sections for comparison of HfON formation on rough and flat Si substrates.

Si(110), respectively. D_{it} was also significantly decreased from $1.8 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ to $4.7 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ for Si(100), and from $7.4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ to $6.9 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ (Fig. 5(c)). The obtained characteristics are promising for the 3D gate structures with various Si surface orientations [35].

Fig. 5(d) shows schematic cross-sections of Al/HfON/Si MOS diodes with rough and flat Si surfaces. When the Si surface roughness is large, thicker IL, which is HfSiON with relatively low dielectric constant, is formed during the Ar/O₂ plasma oxidation and/or PDA processes because the rough Si surface is easy to be oxidized by the existence of various surface orientations. When the Si surface is relatively flat, thick IL formation is suppressed as shown in Fig. 5(d) which led to the thinner EOT. The IL thickness dependence on the Si surface roughness was confirmed by ellipsometry.

As mentioned above, ΔV_{FB} in C-V became large when the Si surface RMS roughness is large. This result suggested that the fixed-charge density at the HfON/Si interface region strongly depends on the Si surface roughness. The quality of the unintentionally formed IL is not good enough. The HfON layer formed on the rough Si surface was also degraded. Therefore, D_{it} and leakage current were decreased by the reduction of Si surface roughness. From these results, Si surface RMS roughness is considered to be one of the key parameter to evaluate the electrical characteristics although the surface roughness was controlled by the annealing temperature in this study.

Fig. 6 shows the time dependent dielectric breakdown (TDDB) characteristics (Weibull plot) evaluated by the constant voltage stress (CVS) method for the fabricated Al/HfON/Si MOS diodes [36]. The stress voltage was $V_{FB}-1 \text{ V}$. The results clearly show that the TDDB characteristics formed on Si(100) and Si(110) strongly depend on the Si surface roughness. Steep Weibull slopes (β) were obtained by reduction of Si surface roughness. As shown in Fig. 6, β was extracted as 1.18 and 1.02 in case of w/o annealed Si(100) and Si(110), while those were 2.69 and 2.38 in case of 1000 °C annealed Si(100) and Si(110), respectively. The reliability of HfON thin films was also significantly improved by the reduction of Si surface roughness.

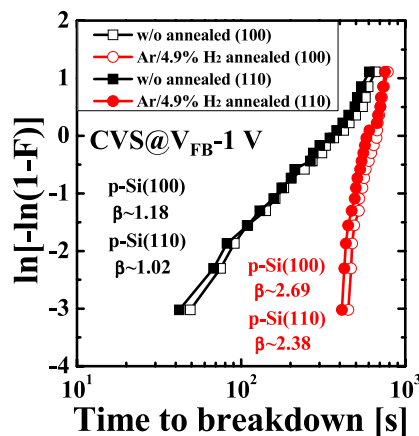


Fig. 6. TDDB characteristics evaluated by CVS method. The stress voltage was $V_{FB}-1 \text{ V}$.

4 Remarkable improvement of device characteristics for MOSFET with HfON gate insulator utilizing Si surface flattening process

In this section, the influence of Si surface roughness on the MOSFET characteristics is described [37, 38, 39]. The nMOSFETs with HfON gate insulator were fabricated on p-Si(100) substrates by typical gate-last process as follows [38, 39]. After the isolation of active region by local oxidation of Si (LOCOS) process, the channel stopper was formed below field oxide (BF_3 , 100 keV, $1 \times 10^{14} \text{ cm}^{-2}$). Then, Si surface flattening process (1000 °C/1 hr, Ar/4.9% H_2) was carried out followed by the S/D ion implantation (PH_3 , 20 keV, $5 \times 10^{15} \text{ cm}^{-2}$). The HfON gate insulator was formed in a same manner as described in Section 3. Finally, contact hole was patterned followed by the Al electrode formation. The gate length (L) and gate width (W) of MOSFETs fabricated in this study were 10 μm and 90 μm , respectively. The fabricated nMOSFETs were characterized by drain current-drain voltage (I_D - V_D), drain current-gate voltage (I_D - V_G), and 1/f noise measurements.

Fig. 7 shows a schematic cross-section, plane-view and I_D - V_D characteristics of the fabricated nMOSFETs. As shown in Fig. 7(c), current drivability was significantly increased for the MOSFET utilizing Si surface flattening process (Ar/4.9% annealed at 1000 °C) compared to that of the device without flattening process. The saturation mobility (μ_{sat}) was increased from 56 $\text{cm}^2/(\text{Vs})$ to 85 $\text{cm}^2/(\text{Vs})$ at same effective electric field ($V_G/EOT = 10 \text{ MV/cm}$), respectively. This is because the surface roughness scattering is a dominant mechanism for mobility degradation at high electric field region [40]. This result suggested that the flattening process used in this study was effective to improve the electrical characteristics of MOSFETs fabricated with several device fabrication processes, such as ion implantation etc., after the flattening process. Actually, the Si surface RMS roughness before the HfON gate insulator formation was confirmed as same as the RMS value after the flattening process especially for the channel region. Another effect of the reduction of Si surface roughness is suppression of IL formation. As described in Section 3,

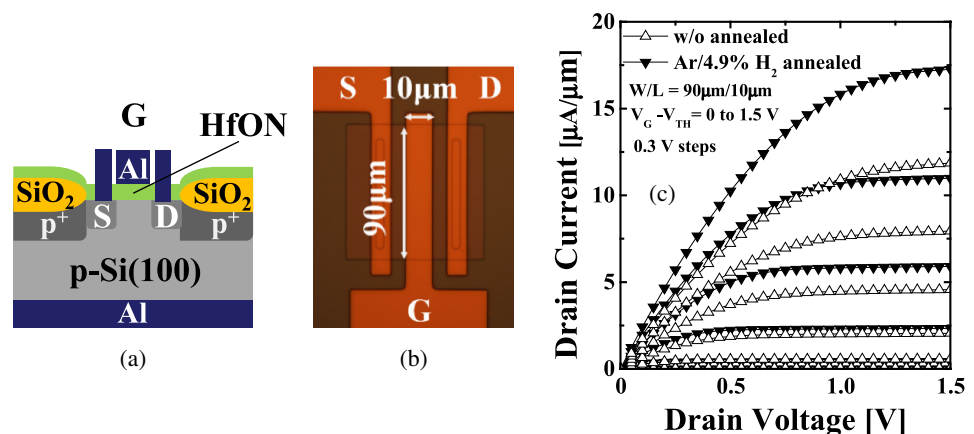


Fig. 7. (a) Schematic cross-section, (b) plane-view and (c) I_D - V_D characteristics of fabricated nMOSFETs.

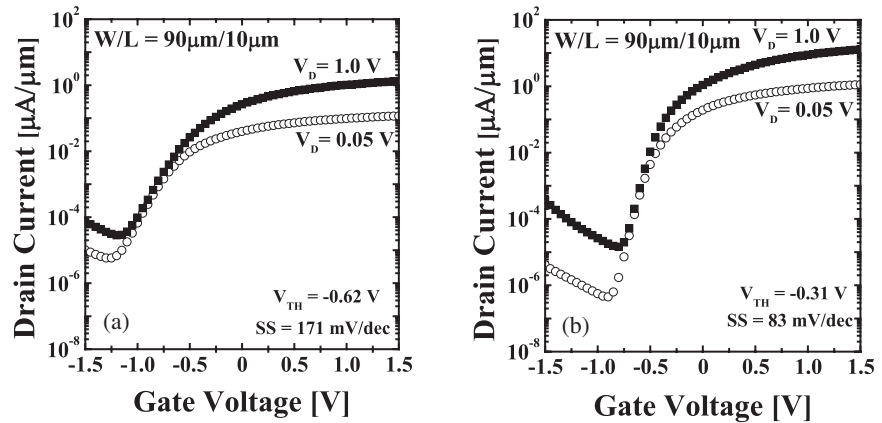


Fig. 8. I_D - V_G characteristics of fabricated nMOSFETs. (a) W/o flattening process, and (b) Ar/4.9% H_2 annealed at 1000°C.

the IL thickness was significantly decreased which led to the small V_{FB} shift with the decrease of fixed charge density at the HfON/Si interface region. It was confirmed that the mobility at the low electric field region, such as 1 MV/cm or below, was significantly increased in case the MOSFET with Si flattening process [not shown]. This is because the Coulomb scattering was also suppressed by the Si flattening process in this gate stack structure [6].

Fig. 8 shows I_D - V_G characteristics of MOSFETs. The threshold voltage (V_{TH}) was changed from -0.62 V (Fig. 8(a)) to -0.31 V (Fig. 8(b)) by the reduction of Si surface roughness. The ideal V_{TH} is 0.12 V for the fabricated MOSFET so that V_{TH} shift was decreased as same as the V_{FB} shift in C-V discussed in Section 3. The subthreshold swing (SS) value of MOSFETs also decreased from 171 mV/dec. (Fig. 8(a)) to 83 mV/dec. (Fig. 8(b)) mainly due to the reduction of D_{it} . Furthermore, off leakage current was decreased by the reduction of Si surface roughness which is attributed to the film quality and D_{it} [6]. D_{it} extracted from SS obtained from I_D - V_G characteristics was $2.8 \times 10^{12} \text{ cm}^2 \text{ eV}^{-1}$ (w/o) and $3.1 \times 10^{10} \text{ cm}^2 \text{ eV}^{-1}$ (Ar/4.9% H_2 annealed at 1000°C), respectively. The obtained D_{it} values are close to the results obtained from C-V characteristics shown in Fig. 5(c).

Fig. 9 shows the noise spectral density in I_D (S_{I_D}) as a function of frequency (f) measured at Tohoku University. $1/f$ noise measurements were carried out using a vector signal analyzer (Agilent 89410A) connected to a low noise preamplifier (Princeton Applied Research 5184) with contacts directly taken on wafer on a cascade probe table (noise level of this system is $10^{-25} \text{ A}^2/\text{Hz}$ at $f = 10 \text{ Hz}$). The MOSFETs were initially biased by a modular dc source (HP 4142B) in order to find the target bias point parameters. The dc source was then replaced by an ultralow noise dc source (Shibasoku PA14A1) for the final noise measurement. As shown in Fig. 9(a), the $1/f$ noise of I_D was significantly decreased by the reduction of Si surface roughness. It is found that the obtained $1/f$ noise level is close to that of the MOSFET with SiO_2 gate insulator fabricated on the atomically flat Si(100) substrate indicated by the dashed line in Fig. 9(a) [41]. This result suggested that the flattening

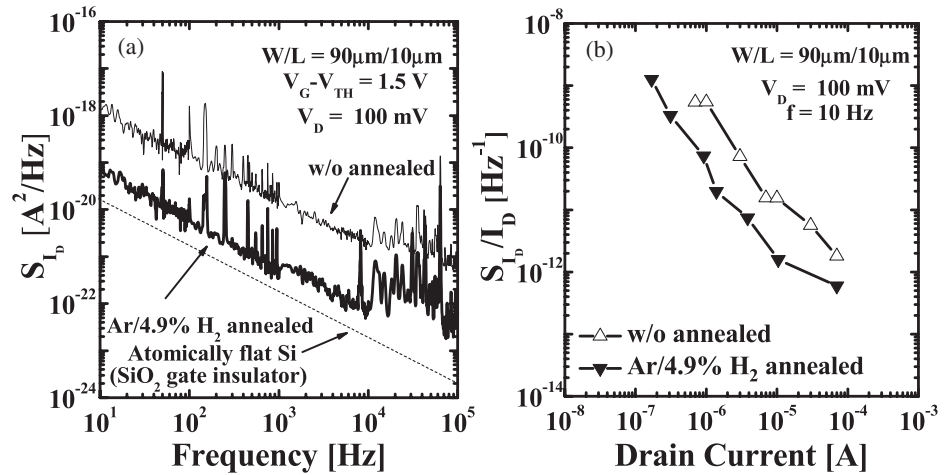


Fig. 9. 1/f noise measurements for fabricated nMOSFETs. (a) Noise spectral density in the drain current ($V_G - V_{TH} = 1.5$ V, and $V_D = 100$ mV), and (b) normalized noise spectral density ($V_D = 100$ mV).

process developed in this study is also effective for the reduction of noise level in the MOSFET with high-k HfON gate insulator.

The normalized noise spectral density (S_{I_D}/I_D) of MOSFET is shown in Fig. 9(b). The MOSFET fabricated on the flat Si surface has lower normalized noise spectral density which is a consequence of the strong influence of the surface roughness scatterings and D_{it} [42, 43]. Further decrease of 1/f noise would be possible by reducing the Si surface roughness to the level of atomically flat, and it will progress the ultralow noise MOSFET applications even with the high-k gate insulator.

5 Conclusions

The impact of Si surface flatness on MOSFET characteristics with ultrathin HfON high-k gate insulator formed by ECR plasma sputtering was described. The surface roughness of Si(100) as well as Si(110) was reduced by Ar/4.9% H_2 annealing utilizing conventional RTA system. Si surface RMS roughness was well controlled by changing the annealing temperature at 700–1000 °C for 1 hr. Although the atomically flat surface was not able to be obtained by the flattening process, Si surface RMS roughness after 1000 °C/1 hr annealing was 0.078 nm for Si(100) and 0.082 nm for Si(110), respectively. This flattening process would be suitable for the surface flattening of 3D gate structures which have various surface orientations of Si.

Electrical characteristics of Al/HfON/Si MOS diodes, such as EOT, J_g , D_{it} and TDDB, showed clear dependence on the Si surface RMS roughness. EOT of below 1 nm, J_g (at $V_{FB} - 1$ V) of 10^{-3} A/cm², and D_{it} of 10^{10} cm⁻² eV⁻¹ were obtained for HfON formed both on Si(100) and Si(110), respectively. Although the annealing temperature was different to control the Si surface roughness, Si surface RMS roughness is considered as a key parameter to evaluate the characteristics to form ultrathin films with new materials on Si substrates.

It was also confirmed that the reduction of Si surface roughness was effective to improve the MOSFET characteristics with HfON gate insulator. Current drivability and mobility were significantly increased by the reduction of Si surface roughness. Furthermore, it was also found that the subthreshold characteristics and 1/f noise characteristics were also remarkably improved.

From the results described in this paper, the author believes that the performance of Si-MOSFETs, as a key device of electronic systems, will be further improved by introducing new materials with various orientations of atomically flat Si surfaces for such as gate insulators, gate electrodes, and S/D contacts.

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