ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.9, No.20, 1611–1616

Divide-by-N and divide-by-$N/N+1$ prescalers based on a shift register and a multi-input NOR gate

Seon-Woo Hwang and Yongsam Moon[a)]

School of Electrical and Computer Eng., University of Seoul, Seoul, Korea

a) *ysmoon001@uos.ac.kr*

Abstract: This paper describes the architecture of a divide-by-N prescaler and a divide-by-$N/N+1$ dual-modulus prescaler based on a shift register and a multi-input NOR gate. The divide-by-N prescaler has a circuit style similar to a linear feedback shift register (LFSR), except for the fact that a multi-input NOR gate is used instead of XOR gates. This architecture can be applied to various division ratios of $N \geq 2$ by changing the numbers of flip-flops and NOR-gate inputs according to specific rules, which will be explained in this paper. The state of the prescaler runs through the correct loop without requiring a reset signal or an initialization circuit.

Keywords: divider, prescaler, dual-modulus divider, linear feedback shift register, PLL

Classification: Integrated circuits

References

[1] Y. Kado, et al., "A 1-GHz/0.9-mW CMOS/SIMOX Divide-by-128/129 Dual-Modulus Prescaler Using a Divide-by-2/3 Synchronous Counter," *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 513–517, April 1993.

[2] B. Chang, J. Park, and W. Kim, "A 1.2 GHz Dual-Modulus Prescaler Using New Dynamic D-Type Flip-Flips," *IEEE J. Solid-State Circuits*, vol. 31, no. 5, pp. 749–752, May 1996.

[3] J. Navarro, et al., "A 1.6-GHz Dual Modulus Prescaler Using the Extended True-Single-Phase-Clock CMOS Circuit Technique (E-TSPC)," *IEEE J. Solid-State Circuits*, vol. 34, no. 1, pp. 97–102, Jan. 1999.

[4] M. V. Krishna, et al., "Design and Analysis of Ultra Low Power True Single Phase Clock CMOS 2/3 Prescaler," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 1, pp. 72–82, Jan. 2010.

[5] W.-H. Chen and B. Jung, "High-Speed Low-Power True Single-Phase Clock Dual-Modulus Prescalers," *IEEE Trans. Circuits Syst. II*, vol. 58, no. 3, pp. 144–148, March 2011.

[6] J. G. Proakis and M. Salehi, *Digital Communications*, Fifth Ed., McGraw-Hill, Boston, 2008.

© IEICE 2012

DOI: 10.1587/elex.9.1611
Received October 06, 2012
Accepted October 10, 2012
Published October 26, 2012

1 Introduction

Phase-locked loops (PLL) have been typically employed in communication IC's and data interfaces for clock generation. Most PLLs include dividers in order to obtain higher frequencies by means of multiplying the reference frequency. A dual-modulus or multi-modulus divider is commonly used in a multi-rate PLL and a fractional-N PLL for frequency synthesis including a spread-spectrum clock generator (SSCG) [1, 2, 3, 4, 5]. In this paper, we use a dual-modulus divider to achieve a fractional-N PLL. By toggling between the two integer division ratios, N or $N+1$, a fractional division ratio can be achieved by time-averaging the divider output. The relationship between the VCO-clock frequency ($f_{\mathrm{VCO\_CLK}}$) and the reference frequency ($f_{\mathrm{REF\_CLK}}$) can be described as

$$f_{\mathrm{VCO\_CLK}} = (N \sim N+1) \times f_{\mathrm{REF\_CLK}} \ . \tag{1}$$

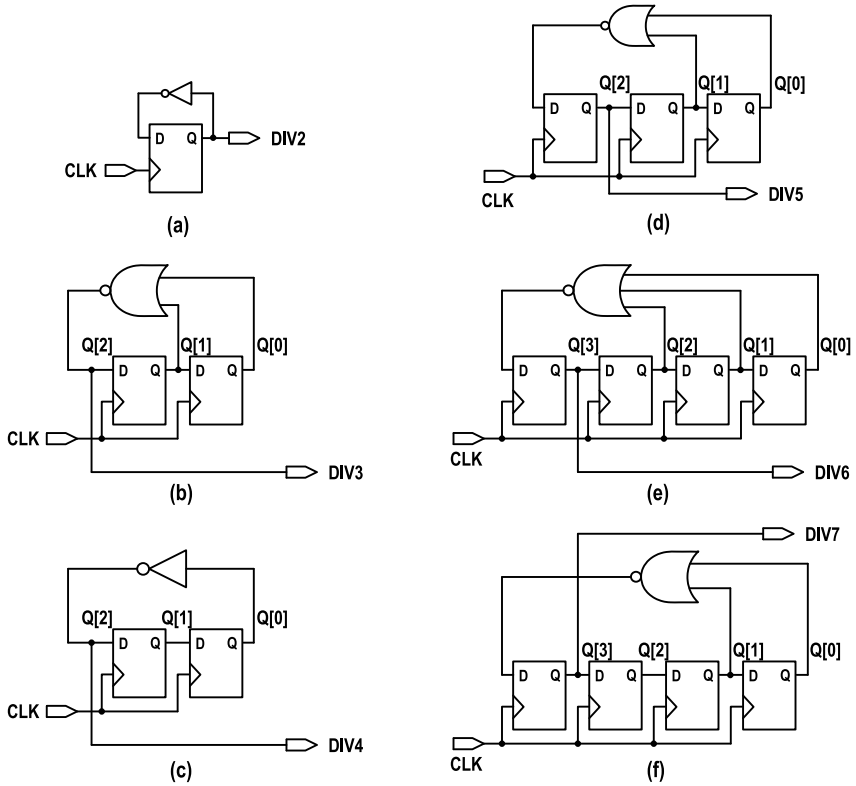
In this paper, the proposed divide-by-N and divide-by-$N/N+1$ dual-modulus prescalers are designed using conventional flip-flops and NOR-gates. The division ratio can be adjusted by varying the numbers of flip-flops and NOR-gate inputs. Of course, if high-speed flip-flops are used as in [2, 3, 4, 5], the operating frequency can be much increased. However, in this paper, the architecture itself is focused on rather than the circuit. This paper is organized as follows. Section II describes the architecture of the proposed divide-by-N and divide-by-$N/N+1$ prescaler circuits. The experimental results are provided in Section III. Finally, Section IV concludes and summarizes this paper.

2 Architecture of divide-by-N and divide-by-$N/N+1$ prescalers

The proposed divide-by-N prescaler circuits are presented in Fig. 1 (a–f), where N ranges from 2 to 7. According to the division ration N, the numbers of the flip-flops and the NOR-gate inputs are determined as K_{N} and R_{N}, respectively. The outputs of the R_{N} consecutive flip-flops from the rightmost flip-flop, $Q[R_{\mathrm{N}}-1:0]$, are connected to the inputs of the NOR gate. Let's explain the proposed divide-by-7 prescaler as an example. It consists of four flip-flops and a two-input NOR gate. In every clock cycle, Q[3:1] are shifted to be Q[2:0] while Q[3] is determined by $\overline{Q[1]+Q[0]}$. The divider has a circuit style similar to a linear feedback shift register (LFSR) [6]. However, while the typical LFSR [6] uses XOR gates and generates a pseudo-random binary sequence (PRBS), the proposed divider uses the NOR gate and generates consecutive '0's and consecutive '1's, which may be thought of as a clock signal with a long period.

In the proposed circuits, the division operation is performed without a reset signal or an initialization circuit. For example, let the divide-by-7 prescaler start with any initial state out of the all states ranging from "0000" to "1111". Although the shift register may go through some transient states, it finally goes into the correct loop, which consists of "0000", "1000", "1100", "1110", "0111", "0011", and "0001". Not only the divide-by-7 prescaler but

© IEICE 2012
DOI: 10.1587/elex.9.1611
Received October 06, 2012
Accepted October 10, 2012
Published October 26, 2012



Division Ratio, N	Output Sequence	# of '0's	# of '1's	K_N	R_N	$K_N - R_N + 1$
2	0_1	1	1	1	1	1
3	00_1	2	1	2	2	1
4	00_11	2	2	2	1	2
5	000_11	3	2	3	2	2
6	0000_11	4	2	4	3	2
7	0000_111	4	3	4	2	3
8	00000_111	5	3	5	3	3

Division Ratio, N	Output Sequence	# of '0's	# of '1's	K_N	R_N	$K_N - R_N + 1$
9	000000_111	6	3	6	4	3
10	000000_1111	6	4	6	3	4
11	0000000_1111	7	4	7	4	4
12	00000000_1111	8	4	8	5	4
13	00000000_11111	8	5	8	4	5
14	000000000_11111	9	5	9	5	5
15	0000000000_11111	10	5	10	6	5

(g)

Fig. 1. Proposed (a) divide-by-2, (b) divide-by-3, (c) divide-by-4, (d) divide-by-5, (e) divide-by-6, (f) divide-by-7 prescaler circuits. (g) The number of flip-flops (K_N) and the number of NOR-gate inputs (R_N) according to division ratio (N).

also any divide-by-N prescaler ($N \geq 2$) has its own correct loop, in which the state of all '0's is always included.

Once the outputs of the flip-flops are all '0's, the leftmost flip-flop (e.g. $Q[3]$ in the divide-by-7 prescaler) will have '1' as the output in the next cycle. Until this '1' is shifted and reaches to the flip-flop whose output is connected to the NOR-gate (e.g. $Q[1]$ in the divide-by-7 prescaler), the leftmost flip-flop will have '1' continuously. If at least one of the NOR-gate inputs is '1', the leftmost flip-flop will have '0' until the outputs of the flip-flops are all '0's. Therefore, a rule can be derived for the number of the flip-flops (K_N) and the number of the NOR-gate inputs (R_N) when the division ratio (N) is larger than one. Here, an inverter is thought of a one-input NOR gate in the case of divide-by-2/-4 circuits. As inferred from the above explanation and tabulated in Fig. 1 (g), the number of '0's in the output sequence is the same

© IEICE 2012
DOI: 10.1587/elex.9.1611
Received October 06, 2012
Accepted October 10, 2012
Published October 26, 2012

as K_N and the number of '1's is the same as $K_N - R_N + 1$. Because the sum of the numbers of '0's and '1's is equal to N,

$$2K_N - R_N + 1 = N. \tag{2}$$

As shown in Fig. 1 (g), whenever N increases by three, K_N increases by two and R_N increases by one. Therefore, the relationship between K_N and N can be derived inductively as shown in Eq. (3). And, from Eq. (2–3), R_N can be expressed as Eq. (4).

$$K_N = \left\lfloor \frac{2}{3}N \right\rfloor \tag{3}$$

$$R_N = 2\left\lfloor \frac{2}{3}N \right\rfloor - N + 1 \tag{4}$$

where $\lfloor\ \rfloor$ is the floor symbol.

With the proposed architecture, a division ratio of any natural number greater than one can be supported without cascading dividers whether the division ratio is a prime number or a composite number.

A divide-by-$N/N+1$ prescaler can be designed by combining a divide-by-N prescaler and divide-by-$N+1$ prescaler as shown in Fig. 2. One input of the AND gate is MC, which controls the division ratio. When MC is '0', the division ratio is N. When MC is '1', the division ratio is $N+1$. In the proposed divide-by-$N/N+1$ prescaler, a rule can also be derived for the number of the flip-flops ($K_{N/N+1}$), the number of the NOR-gate inputs ($R_{N/N+1}$), and the position of the AND gate. First, $K_{N/N+1}$ is determined as the greater one of K_N and K_{N+1}, which are the numbers of the flip-flops in

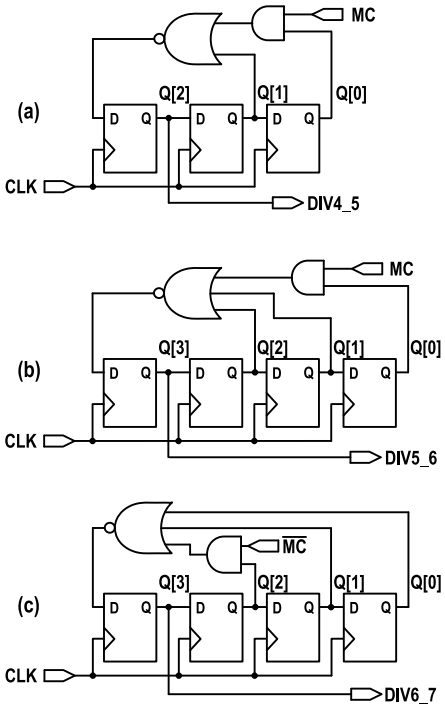


Fig. 2. Proposed (a) divide-by-4/5, (b) divide-by-5/6, and (c) divide-by-6/7 prescaler circuits.

© IEICE 2012
DOI: 10.1587/elex.9.1611
Received October 06, 2012
Accepted October 10, 2012
Published October 26, 2012

the divide-by-N and divide-by-$N+1$ prescaler circuits, respectively. Thus, because $K_{\mathrm{N}} \leq K_{\mathrm{N+1}}$,

$$K_{\mathrm{N/N+1}} = \max(K_{\mathrm{N}}, K_{\mathrm{N+1}}) = K_{\mathrm{N+1}} \tag{5}$$

Second, $R_{\mathrm{N/N+1}}$ is determined as the greater one of R_{N} and $R_{\mathrm{N+1}}$, which are the numbers of the NOR-gate inputs in the divide-by-N and divide-by-$N+1$ prescaler circuits, respectively. Thus,

$$R_{\mathrm{N/N+1}} = \max(R_{\mathrm{N}}, R_{\mathrm{N+1}}) \tag{6}$$

Third, the position of the AND gate is determined by whether or not N is a multiple of three. When N is a multiple of three, the AND gate is located at the output of the R_{N}'th flip-flop, $Q[R_{\mathrm{N}}-1]$ and $\overline{MC}$ is used. Otherwise, when N is not a multiple of three, the AND gate is located at the output of the rightmost flip-flop, $Q[0]$.

3 Experimental results

In order to verify the proposed architecture, a divide-by-10 circuit in Fig. 3 (a) and a divide-by-11 circuit in Fig. 3 (b) are designed and then combined to be a divide-by-10/11 circuit in Fig. 3 (c) according to the aforementioned

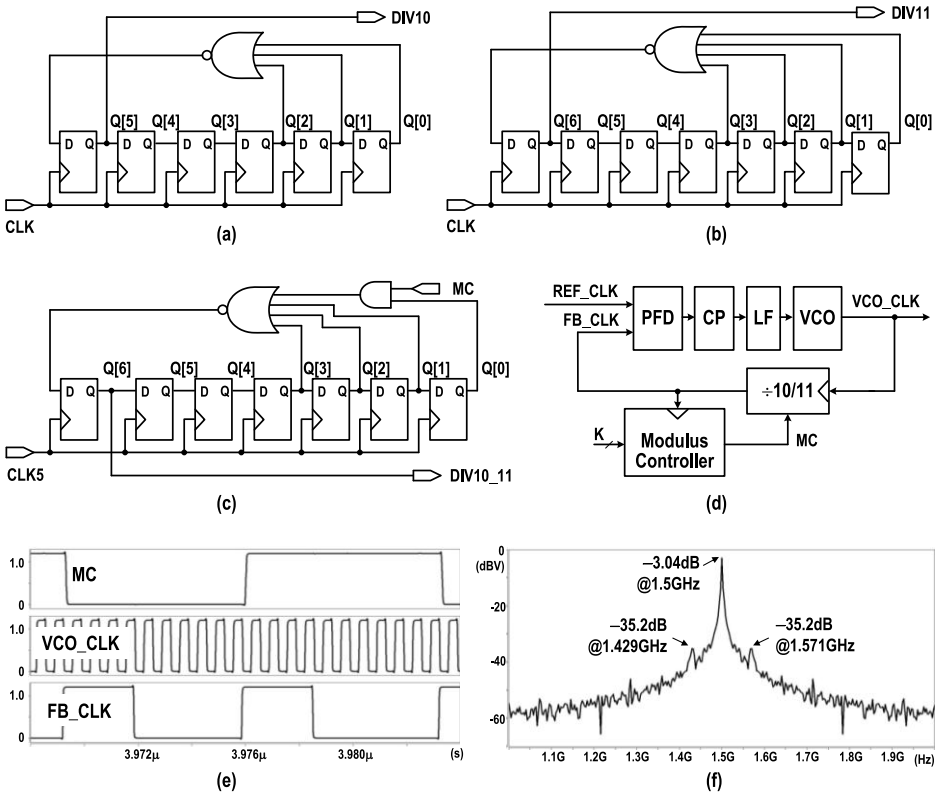


Fig. 3. Proposed (a) divide-by-10, (b) divide-by-11, and (c) divide-by-10/11 prescaler circuits. (d) Test fractional-N PLL circuit. (e) Simulated waveforms in time domain and (f) simulated spectrum of *VCO_CLK*.

© IEICE 2012
DOI: 10.1587/elex.9.1611
Received October 06, 2012
Accepted October 10, 2012
Published October 26, 2012

rules. However, the four-input NOR gate has relatively high fanin, resulting to large gate delay. In order to reduce the gate delay, the four-input NOR function is implemented by a multilevel (or cascaded) logic circuit using INV gates and two-input NOR/NAND gates, which shows the same functionality but smaller delay. Although any signal of Q[6:0] can be selected as *FB_CLK*, Q[6] is selected in this design.

Fig. 3 (d) shows a test fractional-N PLL circuit to demonstrate the functionality of the divide-by-10/11 circuit, which is designed in 0.11-μm CMOS technology. The division ratio is selected by *MC*. The frequency ($f_{\mathrm{REF\_CLK}}$) of the reference clock (*REF_CLK*) is 142.9-MHz (= 1/7 ns). Fig. 3 (e) shows the simulated waveforms of *VCO_CLK* and *FB_CLK*, which are the input and output signals of the divide-by-10/11 circuit, respectively. When *MC* is '0', *FB_CLK* exhibits a periodic pattern of "1111_0000_00" with only two transitions in one period. When *MC* is '1', *FB_CLK* exhibits a periodic pattern of "1111_0000_000." Regardless of *MC*, *FB_CLK* shows a high duration of $4 \times T_{\mathrm{VCO\_CLK}}$. Here, $T_{\mathrm{VCO\_CLK}}$ is the period of the VCO clock, *VCO_CLK*. The duty cycle of *FB_CLK* is not important because only the rising edges are used for phase/frequency detection in the PFD.

MC is intentionally controlled to be alternately toggled between '0' and '1' as shown in Fig. 3 (e). Therefore, the reference frequency is multiplied by 10.5, thereby resulting in the generation of 1.5-GHz ($= 10.5 \times f_{\mathrm{REF\_CLK}}$) *VCO_CLK* as shown in Fig. 3 (f). The spectrum also shows spurious tones at 1.429 GHz ($= 10 \times f_{\mathrm{REF\_CLK}}$) and 1.571 GHz ($= 11 \times f_{\mathrm{REF\_CLK}}$).

As aforementioned, the proposed divide-by-10/11 circuit is designed using conventional flip-flops and logic gates. If high-speed flip-flops and gates are used as in [2, 3, 4, 5], the operating frequency can be much increased.

4 Conclusion

In this paper, we propose the architecture of a divide-by-N prescaler and a divide-by-$N/N+1$ dual-modulus prescaler. By changing the numbers of the flip-flops and the NOR-gate inputs according to specific rules, the divide-by-N prescaler can be easily designed for any division ratio, as long as it is greater than one, without cascading dividers whether the division ratio is a prime number or a composite number. Moreover, the divide-by-$N/N+1$ prescaler is designed by combining the divide-by-N prescaler and divide-by-$N+1$ prescaler circuits with an AND gate. The divide-by-N prescaler and divide-by-$N/N+1$ prescaler operate without a reset signal or an initialization circuit.

Acknowledgments

This work was supported by the 2010 Research Fund of the University of Seoul.

© IEICE 2012
DOI: 10.1587/elex.9.1611
Received October 06, 2012
Accepted October 10, 2012
Published October 26, 2012