IEICE Electronics Express, Vol.7, No.19, 1480–1485

A novel current conveyor with high functionality and optimized ports

Alireza Mahmoodi[a)] **and Adib Abrishamifar**

Electrical and Electronic Engineering faculty, Iranian University of Science and Technology (IUST), Tehran 16846, Iran

a) *Alireza_Mahmoodi@ieee.org*

Abstract: In this paper a novel current conveyor with high functionality is proposed. The current conveyor utilizes a four quadrant current multiplier which can be used as a programmable gain amplifier in addition to current multiplication, which enables the device to function in both linear and non-linear regions. The correlation of the ports was optimized so that all of them would perform as input and output ports that are suitable for programmable applications. The current conveyor was implemented in 0.18 μm CMOS process with a $\pm$0.9v voltage supply. The results were obtained by Hspice and with a high detailed transistor library.

Keywords: current conveyor, optimized correlation, multi-functioning

Classification: Integrated circuits

References

[1] S. Minaei, O. K. Sayin, and H. Kuntman, "A New CMOS Electronically Tunable Current Conveyor and Its Application to Current-Mode Filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 7, pp. 1448–1457, July 2006.

[2] M. Siripruchyanun and W. Jaikla, "Current controlled current conveyor transconductance amplifier (CCCCTA): a building block for analog signal processing," *Electr Eng Springer*, 2008.

[3] A. A. El-Adawy, A. M. Soliman, and H. O. Elwan, "Low voltage digitally controlled current conveyor," *Int. J. Electron. Commun (AEÜ)*, vol. 56, no. 3, pp. 137–144, 2002.

[4] J. Becker, F. Henrici, S. Trendelenburg, M. Ortmanns, and Y. Manoli, "A Field-Programmable Analog Array of 55 Digitally Tunable OTAs in a Hexagonal Lattice," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2759–2768, Dec. 2008.

[5] R. J. Wiegerink, "Application: Fast Four-Quadrant Current Multiplier," *Analysis and synthesis of MOS Translinear Circuits*, Mohammed Ismail, Kluwer Academic Publishers, Massachusetts, pp. 109–124, 1993.

[6] C.-C. Chen, K.-Y. Lin, and N.-K. Lu, "Low Voltage High Performance First and Third Generation Current Conveyor in 0.18 μm CMOS," *IEEE ASICON*, pp. 1498–1501, 2008.

DOI: 10.1587/elex.7.1480
Received August 25, 2010
Accepted September 08, 2010
Published October 10, 2010

IEICE Electronics Express, Vol.7, No.19, 1480–1485

1 Introduction

Current conveyors are useful devices which are greatly used in analog signal processing. Several applications such as filtering, impedance converting, inductor simulation, amplification, sensing and oscillation are practical with current conveyors. Many types of them have been reported since 1968, but they basically function by conducting a current and voltage signal from one port to another. In signal processing many applications like filtering require tuning and adaption, thus a programmable circuit can be worthwhile. Some current conveyors that have the capability to be programmed digitally or electronically are reported [1, 2, 3]. Moreover programmable circuits such as Field Programmable Analog Arrays (FPAAs) and Analog Signal Processors (ASPs) deal with many types of linear and non-linear applications, which require more than tuning. In these systems the functions are fundamentally derived from the combination of several subsystems via programmable internal connections [4]. When subsystems have higher functionality the internal connections between them can be decreased. This results in higher performance due to the decrease of parasitic effects of the connecting lines.

This paper proposes a novel programmable current conveyor with high functionality which performs linear and non-linear tasks in voltage and current mode. The results were compared with similar recent work.

2 The novel current conveyor with high functionality

In this section the concepts of the novel current conveyor and its characteristics are explained. An implementation of the novel current conveyor was proposed in 0.18 μm CMOS technology.

The necessity of programmability has changed many analog circuits to programmable devices. The main idea of implementing this current conveyor was to apply it in analog programmable circuits, where high functionality and low number of input and output ports would decrease the number of internal connections and subsystems. Fig. 1 (a) depicts the realization of the novel current conveyor by its component subsystems and Fig. 1 (b) shows its symbol. The current conveyor consists of two CCIIs and two current squarers. The current squarers obey the MTL square law principle [5] and their output currents are shown in Eq. 1. I_Y is a product of the current squarers and is derived from Eq. 2. The CCIIs conduct I_X and I_G to the inputs of the current squaqrers, I_X to I_Z, V_Y to V_X and V_Z to V_G. The implementation of the current conveyor is shown in Fig. 1 (c). The class AB CCII has low power consumption and high frequency and is actually a current mirror by including I_{b1} and I_{b2} current sources for transferring voltages ($V_X = V_Y$ and $V_G = V_Z$) in translinear loops (M_{V1}, M_{V2}, M_{V3}, M_{V4}) and (M_{V6}, M_{V7}, M_{V8}, M_{V9}). In the absences of I_{b1} and I_{b2}, the CCIIs will become current mirrors and the system will function as a current multiplier only. When considering all the current directions toward the inside of the current conveyor, the matrix in Eq. 3 expresses the terminal relations of the device. It is understood that unlike conventional current conveyors, no completely zero columns exist,

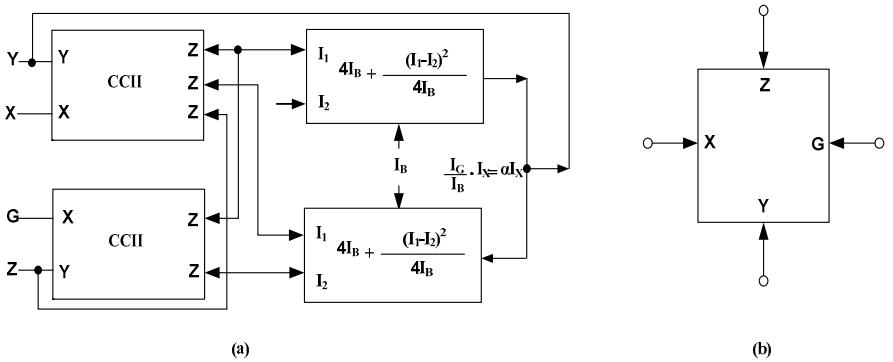
DOI: 10.1587/elex.7.1480
Received August 25, 2010
Accepted September 08, 2010
Published October 10, 2010

which means that all terminals are input and output ports.

$$I_{squarer} = 4I_B + \frac{(I_1 - I_2)^2}{4I_B} \tag{1}$$

$$I_Y = 4I_B + \frac{[-(I_X + I_G)]^2}{4I_B} - 4I_B - \frac{[-(I_X - I_G)]^2}{4I_B} = \frac{I_X.I_G}{I_B} \tag{2}$$

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_G \end{bmatrix} = \begin{bmatrix} 0 & -\frac{I_G}{2I_B} & 0 & -\frac{I_X}{2I_B} \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_G \end{bmatrix} \tag{3}$$



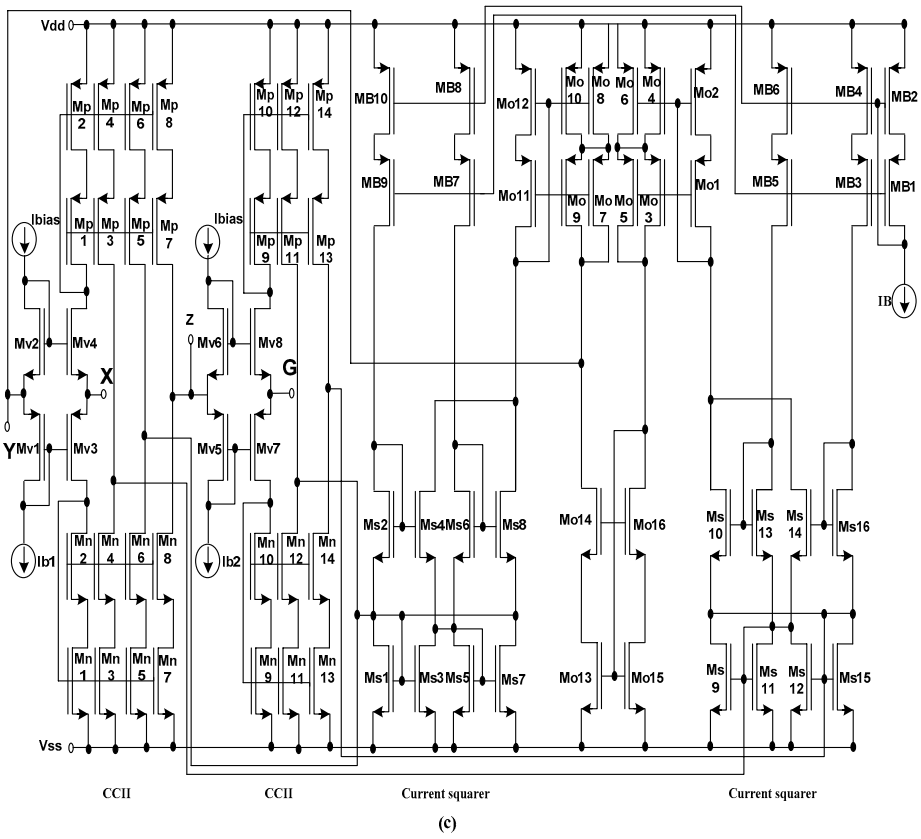


Fig. 1. The proposed current conveyor (a) Realization and block diagram (b) Symbol (c) CMOS circuit implementation

DOI: 10.1587/elex.7.1480
Received August 25, 2010
Accepted September 08, 2010
Published October 10, 2010

3 Application examples

The motivation of designing this current conveyor was to apply analog functions with high density and performance. In the proposed circuit the mixture of linear and non-linear functions and the correlations of the ports can pro-

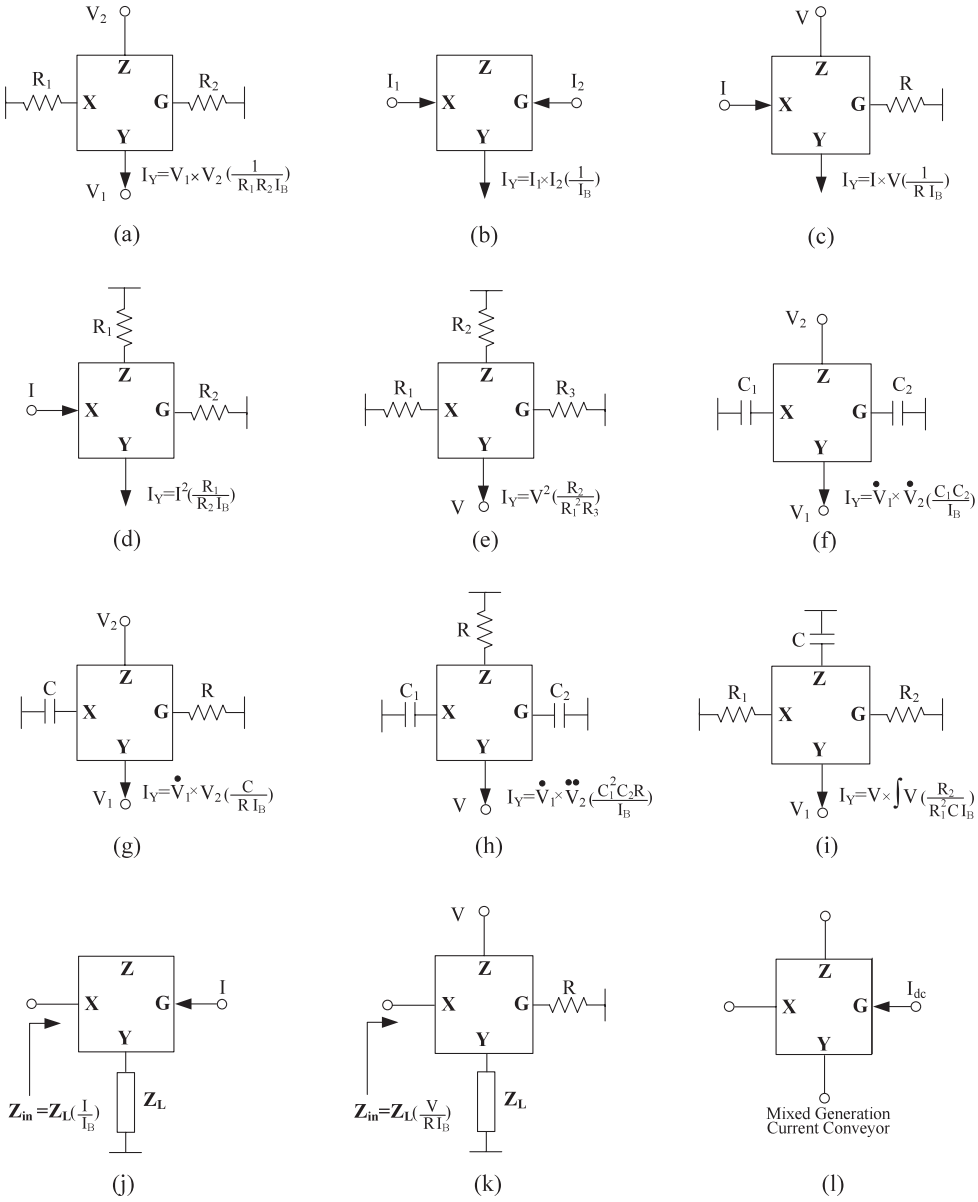


Fig. 2. Application of the proposed novel current conveyor (a) Voltage multiplier (b) Current multiplier (c) Voltage and current multiplier (d) Current squarer (e) Voltage squarer (f) First and first order differential multiplier (g) First and zero order differential multiplier (h) First and second differential order multiplier (i) Integral multiplier (j) Current control impedance converter (k) Voltage control impedance converter (l) Programmable gain current conveyor (Mixed Generation Current Conveyor)

DOI: 10.1587/elex.7.1480
Received August 25, 2010
Accepted September 08, 2010
Published October 10, 2010

duce many linear and non-linear functions which are depicted in Fig. 2. The current conveyor can function as a multiplier, programmable squaqrer, differential multiplier, impedance converter and a programmable gain current conveyor (Mixed Generation Current Conveyor).

4 Simulation results and comparison

The proposed novel current conveyor was implemented in 0.18 μm CMOS technology and the results were obtained by Hspice simulator. The dimension values of transistors M_{v1}-M_{v8}, M_{n1}-M_{n14}, M_{p1}-M_{p14}, M_{s1}-M_{s16}, M_{B1}-M_{B10}, M_{o1}-M_{o12} and M_{o13}-M_{o16} are 10 μm/0.18 μm, 5 μm/0.18 μm, 10 μm/0.18 μm, 2.4 μm/0.2 μm, 10 μm/0.4 μm, 20 μm/0.18 μm and 15 μm/0.18 μm, respec-

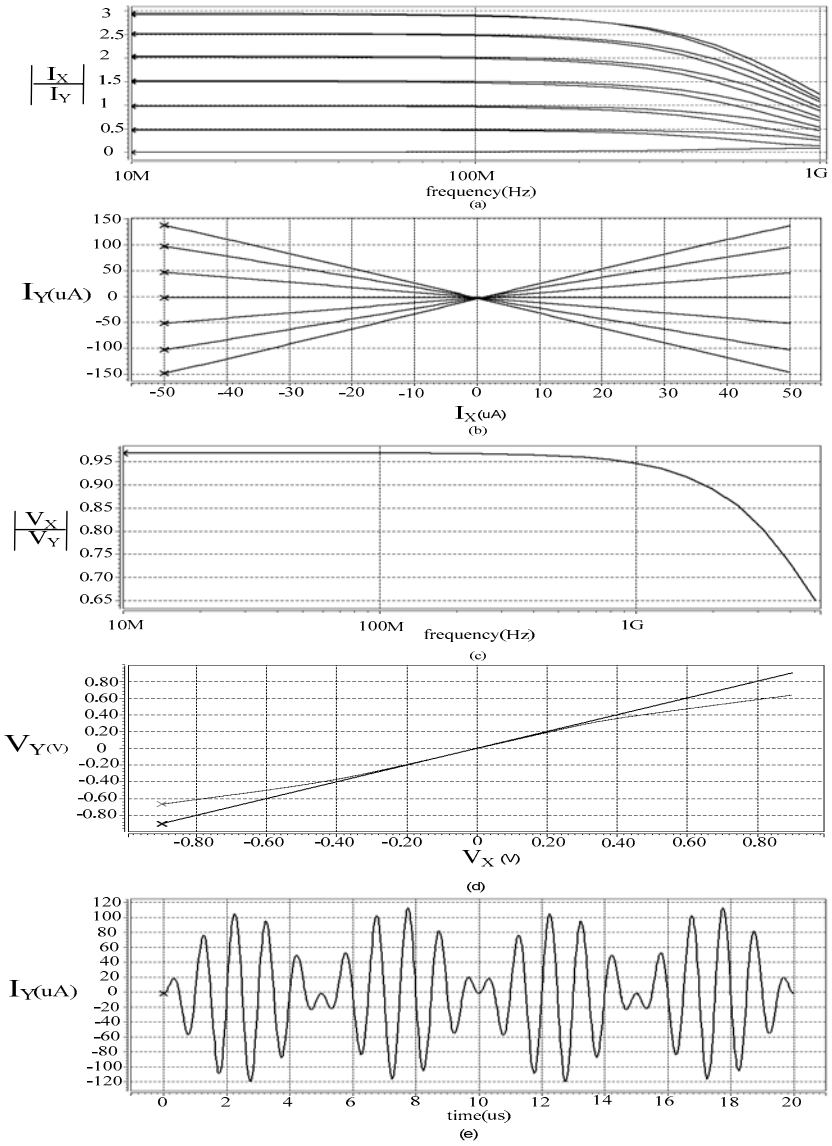


Fig. 3. Simulation results of the proposed current conveyor (a) Current gain (b) The dc current transfer response for different I_G (c) Voltage gain (d) The dc voltage transfer response (e) Four-Quadrant current multiplication

DOI: 10.1587/elex.7.1480
Received August 25, 2010
Accepted September 08, 2010
Published October 10, 2010

tively. The ac current gain between ports Y and X is adjustable from −3 to 3, where the average bandwidth was 574 MHz, shown in Fig. 3 (a). This allows the device to perform functions in video frequencies. Fig. 3 (b) shows the dc current transfer response of ports X and Y for different current gains. The ac voltage gain and dc transfer response between ports X and Y are shown in Fig. 3 (c) and Fig. 3 (d). Fig. 3 (e) shows current multiplication of two sinusoidal input signals. The results were compared with similar works in [1] and [6] in Table I and had higher performance in almost all cases.

Table I. Performance comparison of high functional current conveyor and recently published works

Reference	[1]	[6]	This work
Technology (μm)	0.35	0.18	0.18
Voltage Supply (V)	3	1.8	1.8
THD (%)	1.3	N.A.	1.02
Power Dissipation(mW)	6.6	5.02	1.71
Current BW (MHz)	100	204.5	574
Voltage BW (GHz)	0.2	2.05	4.67
Current Dynamic Range (μA)	±200	±392	±200
Voltage Dynamic Range (V)	-0.5 — 0.6	-0.13 — 0.88	-0.40 — 0.40
Current Gain	0 — 3	1 & -1	-3 — 3

5 Conclusion

A novel current conveyor with high functionality was discussed. All the ports functioned as input and output ports resulting in a transfer function matrix without any completely zero columns. In addition the device had linear and non-linear characteristics which can be very useful in programmable circuits. The device also had high performance and could operate in high frequencies, thus in the future it can be applied in high frequency circuits such as video or RF processors. The design was implemented in 0.18 μm CMOS technology. The results were obtained by Hspice simulator and compared with recently published works.

Acknowledgments

The authors would like to thank Iran Telecommunication Research Center ministry for partially sponsoring this work.

DOI: 10.1587/elex.7.1480
Received August 25, 2010
Accepted September 08, 2010
Published October 10, 2010