

A technique for reducing data converters in MIMO systems

Eui-Rim Jeong¹, Soon-Il Hong¹, In-Pyo Hong²,
and Yong-Up Jang^{2a)}

¹ Hanbat National University,

San 16–1, Duckmyoung-dong, Daejeon 305–719, Korea

² The Agency for Defense Development, 111, Sunam-dong, Daejeon 305–152, Korea

a) yongup.jang@gmail.com

Abstract: We propose a technique to reduce the number of data converters in multiple-input multiple-output (MIMO) systems. While the conventional MIMO systems require the same number of data converters as that of antennas, the proposed method requires only one high speed data converter and one analog switch, regardless of the number of antennas. Hence, the power consumption and implementation area can be reduced. The experiment results confirm the effectiveness of the proposed technique.

Keywords: data converter, MIMO, ADC, DAC, analog switch

Classification: Electron devices, circuits, and systems

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1 Introduction

Multiple input multiple output (MIMO) techniques enable high speed reliable communication in wireless systems, and the modern wireless communication standards such as IEEE 802.11 and LTE adopt these techniques as mandatory options. The MIMO can increase data rates and/or coverage of service area, and improve communication reliability without any additional radio frequencies. To maximize such advantages, the number of antennas tends to increase in the future wireless systems. At the same time, energy efficient communications are receiving attention these days [1]. Energy efficient communication focuses on the throughput divided by the consuming energy, rather than the throughput itself. From the energy

consumption point of view, the MIMO systems consume more energy as the number of antennas increases. To reduce the power consumption and implementation complexity, [2] considers the system whose radio frequency (RF) chains are fewer than the number of antennas, and suggests an analog beamforming method. In [3], an antenna selection technique was proposed for the same scenario in [2]. However, since only a part of antennas are selected and used for communications among the total available antennas, the achievable throughput can be lowered than the systems utilizing the entire antennas.

This paper considers reduction of area and power consumption in MIMO systems by reducing the number of data converters without any loss of the achievable throughput. If the number of antennas is N and there are N RF chains, N data converters are needed in conventional systems. However, the proposed method requires only one high speed data converter and one analog switch. Specifically, the multiple Tx (Rx) signals are time-division multiplexed and converted into analog (digital) signal by a high speed digital-to-analog converter (analog-to-digital converter). For the transmitter case, the digital-to-analog converter (DAC) output is de-multiplexed by an analog switch to separate the N multiple signals. On the other hand, for the receiver case, the sampled TDM Rx signal is de-multiplexed by a simple digital switch. The principle of the proposed idea is very simple, but the power consumption and the area can be significantly reduced. Indeed, according to the data sheets on the commercial devices, multiple low speed data converters consume much more power than a single high speed data converter. To investigate the effectiveness of the proposed technique, we perform experiment with commercial devices. The results confirms that the proposed method can replace multiple data converters with one data converter.

The organization of this paper is as follows. Section II describes the proposed MIMO transmitter and receiver, and their operations. The experiment setup and results are presented in Section III.

2 Proposed technique

Fig. 1 shows the structure of the proposed system. The system has N Tx antennas and M Rx antennas. D represents 1 clock delay in digital domain and T is 1 clock

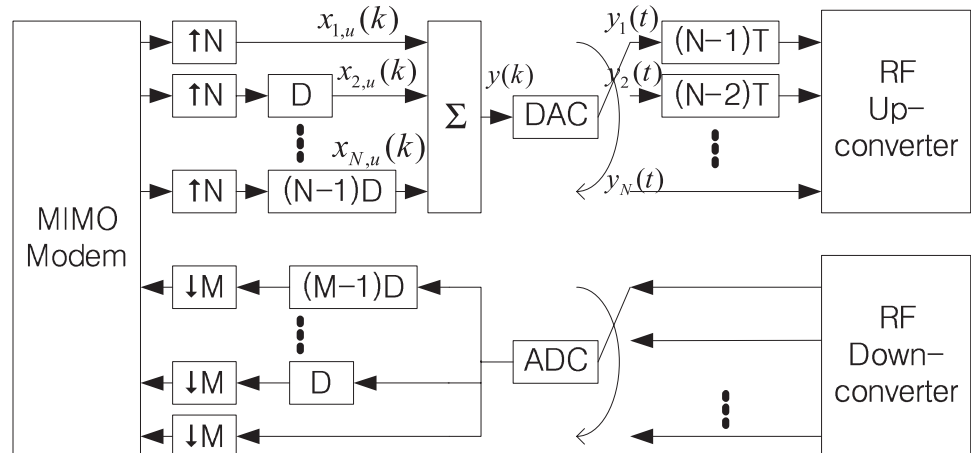


Fig. 1. Structure of proposed MIMO system.

period delay in analog domain, i.e., $T = 1/F_s$ where F_s is the sampling clock of the DAC. we explain the transmitter first, followed by the receiver.

2.1 Transmitter

The Tx modem outputs have N signals to transmit via N antennas. Before converting those signals into analog signals, they are N -times upsampled. Denoting $x_n(k)$ and $x_{n,u}(k)$ as n -th signal to transmit and its upsampled version, respectively,

$$x_{n,u}(k) = \begin{cases} x(k/N), & k = iN (i : \text{integer}) \\ 0, & \text{otherwise.} \end{cases} \quad (1)$$

The upsampled signal has N -times higher clock frequency than the original signal and $N - 1$ zeros are inserted between non-zero samples. Next, the n -th signal, $x_{n,u}(k)$ is delayed by $n - 1$ clocks. Thus, the n -th signal becomes $x_{n,u}(k - n + 1)$. After that, those N signals are summed up. Since all the signals have different integer delays, the non-zero samples do not interfere with each other, i.e., they are multiplexed based on the TDM manner. The multiplexed signal is converted into analog signal via the DAC. Then the analog signal is de-multiplexed by the analog switch. Fig. 2 shows an example when $N = 2$. $y(t)$ represents the DAC output. Due to the nature of zero-order holder (ZOH) of the DAC, the output maintains the value for one clock interval. $y_1(t)$ and $y_2(t)$ are the signals separated by the analog switch for the antenna 1 and the antenna 2, respectively. Since n -th signal has $n - 1$ clock delays with respect to the first signal, a proper delay should be applied to each signal to synchronize all the signals (Fig. 1).

2.1.1 Frequency domain interpretation

The n -th signal $y_n(t)$ of the analog switch output can be written as

$$y_n(t) = \left(\sum_{k=-\infty}^{\infty} x_n(k) \delta\left(\frac{t - kNT}{NT}\right) \right) \otimes h(t) \quad (2)$$

where \otimes represent the convolution operation and $h(t)$ is the impulse response of the ZOH defined as

$$h(t) = \begin{cases} 1, & \text{if } -\frac{T}{2} \leq t \leq \frac{T}{2} \\ 0, & \text{otherwise.} \end{cases} \quad (3)$$

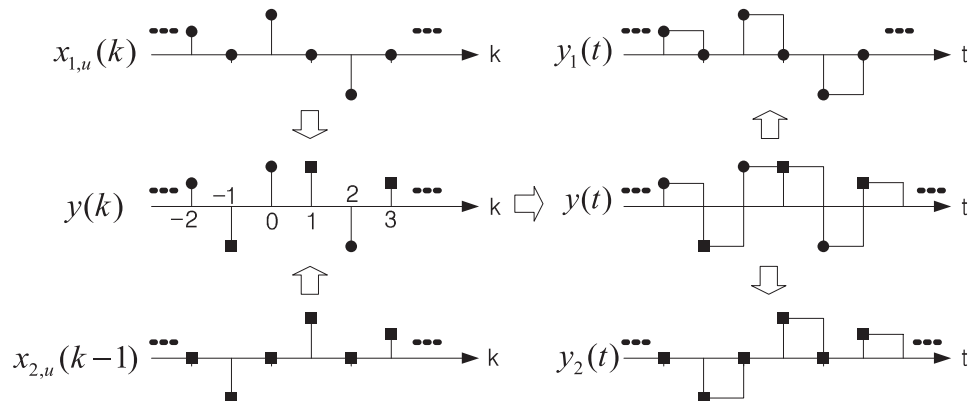


Fig. 2. Example of proposed transmitter for $N = 2$.

On the contrary, for conventional MIMO systems with multiple DACs, the impulse response of the ZOH is N -times longer because the clock speed is N -times lower, i.e.,

$$h_c(t) = \begin{cases} 1, & \text{if } -\frac{NT}{2} \leq t \leq \frac{NT}{2} \\ 0, & \text{otherwise} \end{cases} \quad (4)$$

where $h_c(t)$ denotes the impulse response of the ZOH for DACs in conventional MIMO systems. The Fourier transforms of $h(t)$ and $h_c(t)$ are $H(f) = T \text{sinc}(fT)$ and $H_c(f) = NT \text{sinc}(fNT)$, respectively, where $\text{sinc}(f) = \sin(\pi f)/\pi f$. $H(f)$ is N times smaller and the main lobe is wider than $H_c(f)$. Hence, it is expected that the signal power of the proposed method is N -times smaller than the conventional method, but the spectrum roll-off droop due to the sinc function can be improved.

2.1.2 Power consumption

To investigate the advantages of the proposed technique, the power consumptions of the proposed method and the conventional one are compared. For realistic comparison, we consider commercial data converters and analog switch. Specifically, AD9117 [4] and ADG936 [5] are chosen for comparison. Assume that the DAC clock speed for the conventional method is 20 MHz and the number of antenna is 4. Then, the DAC clock speed of the proposed method becomes 80 MHz. According to Fig. 83 in [4], when the DAC operates in 20 mA OUT mode, it consumes 58 mA at 20 MHz and 65 mA at 80 MHz. Since the supply voltage is 3.3 V, the conventional method with 4 DACs consumes totally 765.6 mW, while the proposed method consumes only 214.5 mW. The analog switch consumes less than 0.00275 mW [5] which is negligible compared with that of the DAC. As a result, the proposed method can reduce 72% of the power consumption.¹ This data shows that the proposed method can significantly reduce the power consumption as well as the implementation area.

2.2 Receiver

Application of the proposed method in MIMO receivers is conceptually the same as the MIMO transmitter (Fig. 1). The analog switch selects the M antennas' signals in turn. To timely multiplex the M signals, the switch operates with a clock speed M -times faster than the conventional ADC in the conventional receivers. The resulting signal is converted into a digital signal via the ADC with the same clock as the analog switch. To separate the M signals at digital domain, proper delays and down-samplers are needed. Since the multiple signals are timely interlaced, the decreasing delays from top to bottom branches as in Fig. 1 are required to synchronize the multiple signals. The final signals after down-sampling by $1/M$ are synchronized M antennas' signals which is the same as those of conventional receivers equipped with M independent ADCs.

Referring to the data sheet of a commercial ADC, AD9445 [6], the power consumptions for 20 MHz and 80 MHz clock speeds are 1.6 W and 1.9 W, respectively. Assuming that the number of receiver antennas is 4, the conventional structure with 4 ADCs consumes 6.4 W while the proposed technique consumes

¹We neglect the power consumption associated with the digital circuits.

only 1.9 W neglecting the power consumptions of the analog switch and the digital circuits. The proposed method can save 70% of the power consumption.

3 Experiment results

In order to verify the proposed method, a MIMO transmitter test bed was made by using commercial FPGA (Xilinx), DAC (AD9114 [4]), and analog switch (ADG936 [5]). The overall experiment setup is shown in Fig. 3. The number of antennas is 2 ($N = 2$). The FPGA is used for MIMO signal generation, upsampling, summation of two signals with a delay, and analog switch control. As a MIMO signal, we generate two sinusoidal waveforms instead of modulated signals to easily observe the separation of two signals by a spectrum analyzer at the analog switch output. The MIMO signal generation block operates in 5 MHz clock. For MIMO signals for antenna 1 and antenna 2, 950 kHz and 650 kHz sinusoidal waveforms are generated, respectively. Since the clock speed of the combined signal is 10 MHz, the DAC also operates in 10 MHz clock.

Fig. 4 shows the 2 analog switch outputs without careful switching time synchronization. Two tones are observed at the analog switch outputs, but the significant portion of the other signal also appears. In other words, the two antennas' signals are not clearly separated. This is due to switching time synchronization error. In the DAC output, the antenna 1 signal and the antenna 2 signal are timely multiplexed. Hence, the analog switch should be exactly changed at the boundary between the two signals. Fig. 4 is obtained without careful timing control. To accurately control the switching time, we empirically adjust the switching clock phase in the unit of $1/300 \text{ MHz} = 3.33 \text{ ns}$. Fig. 5 shows the analog

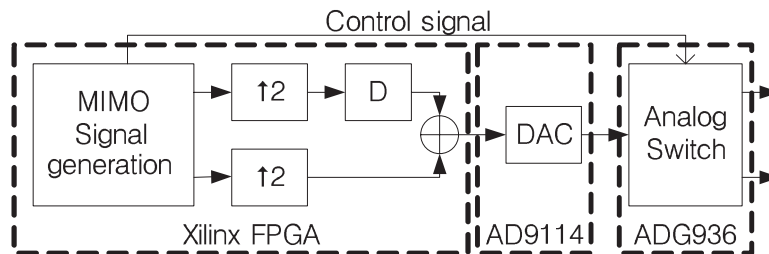


Fig. 3. Block diagram of experiment setup.

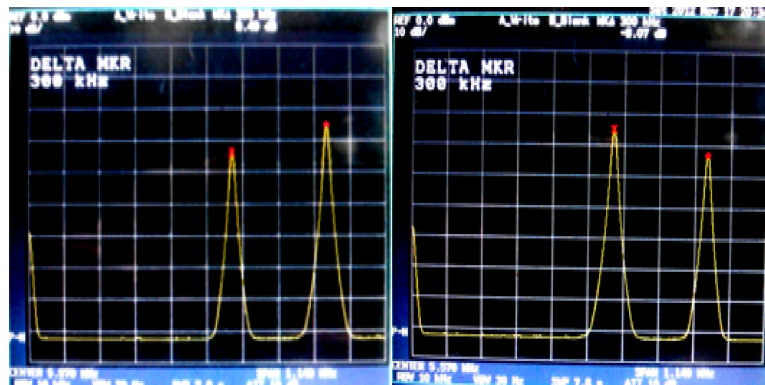


Fig. 4. Spectrum before timing control of analog switch (left: antenna 1, right: antenna 2).

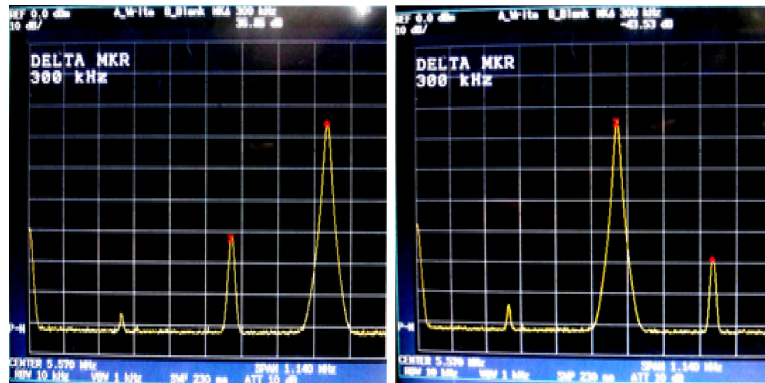


Fig. 5. Spectrum after timing control of analog switch (left: antenna 1, right: antenna 2).

switch outputs after adjusting the switching time. The separation of the two signals is improved, and the other signal's interference is reduced down to -35 dB. Those results confirm that the proposed technique is effective and properly working, but also indicate that the fine timing control of the analog switch is important for perfect signal separation.

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