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Improved soft switching dual switch forward converter

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Abstract: An improved soft switching dual-switch forward converter topology is proposed in this paper. Compared with conventional dual-switch forward converter, the proposed converter employs an auxiliary switch and a clamp capacitor to instead of two reset diodes. Therefore, its duty cycle can exceed 0.5 to achieve wide range input voltage, also soft switching can be achieved for all switches. Especially, voltage stress across main switches can be clamped at $1/2\,V_{in}$, voltage stress across auxiliary switch can be clamped at V_{in}. In addition, due to clamp capacitor series with the transformer, duty ratio can be extended with equation $V_o = \frac{V_{in}(1-D)D}{N}$. Thus, as a kind of better cost-effective approach, it is very attractive for high input, wide range and high efficiency application.

Keywords: dual-switch forward converter, soft switching, wide range
Classification: Science and engineering for electronics

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1 Introduction

Single-switch forward converter is widely used due to the advantage of simple structure and low cost [1]. But it has disadvantage of high voltage stress of switch, in order to overcome the disadvantage, dual-switch forward topology is proposed. Comparing with single-switch forward converter, it has some obvious advantages as follow. The transformer magnetization can be reset by input voltage that improve the efficiency and reduces EMI. Stress of switches is clamed at input voltage to reduce voltage stress of main switch. In addition, there is an important reason which has better robust than other converters. Details operation has been analyzed [2, 3]. However, the dual-switch forward converter has several major disadvantages, such as maximum duty cycle is not exceed to 0.5, hard switching is commutated, large filter inductor is required. Because of above reasons, dual-switch forward converter is not so widely used for wide range input voltage power application. In order to solute these problems, a number of papers are proposed [4, 5, 6, 7, 8]. However, among them, voltage stresses of switches approximately equal or more than input voltage, moreover due to RCD clamp circuit is used, which reduce efficiency.

This paper presents an improved soft-switching dual-switch forward converter topology which employs an auxiliary switch and a clamp capacitor to instead of two diodes. Comparing with conventional dual-switch forward converter, its duty cycles can be more than 0.5 to achieve wider range input voltage, soft switching can be achieved for all switches. In proposed topology, voltage stress across main switches can be clamped at $1/2\,V_{in}$, voltage stress across auxiliary switch can be clamped at V_{in}. There, D is duty cycle of main switches. Furthermore, output voltage can be calculated by $V_o = V_{in}(1-D)D/N$.

2 Circuit description

The configurations of conventional and proposed dual-switch forward converter are shown in Fig. 1 (a) and (b), respectively. The proposed converter is composed with switches S_1, S_2, parasitic capacitors Cs_1, Cs_2, auxiliary switch S_a, its parasitic capacitors Cs_a, clamp capacitor C_c, transformer T,

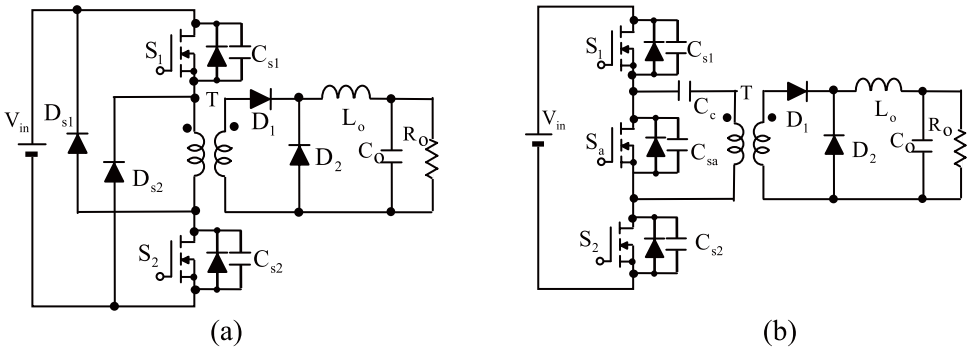

Fig. 1. Diagram of conventional and proposed dual-switch forward converter

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leakage and magnetizing inductances L_l and L_m, rectifier diode D_1, freewheel diode D_2, filter inductor L_o, filter capacitor C_o, and load resistor R_o. Here, C_c is connected in series with the primary winding of the transformer T, S_a is between S_1 and S_2 which parallels with transformer T and clamp capacitor C_c. In order to simplify the operation analysis, all the components are assumed ideal and the filter L_o is large enough to assume it as a constant current source I_o, the clamp capacitor C_c is assumed large enough to neglect the ripple across it and L_m are larger than L_l.

3 Operation principle

During one switching cycle of the proposed converter, it can be divided into six operation modes, equivalent circuits of each operation mode is shown in Fig. 2.

The modes of operations are described as follows:

Mode (1) [t_0-t_1]: During the mode, main switch S_1 and S_2 are simultaneously turned off at t_o, rectifier diode D_1 still keeps on. Magnetizing inductance current I_m and reflected output current nI_o start to resonate with capacitors Cs_1, Cs_2, Cs_a and Cc. To simplify the analysis, assuming the voltage across the coupled capacitor Cc is voltage source V_c. During the period, Cs_1, Cs_2 and Cs_a are charged and discharged through resonant manner. Main switch voltages Vs_1 and Vs_2 rapidly rise. At same time, auxiliary switch voltage Vs_a falls, which will reduce to zero at t_1. Since Vs_1 and Vs_2 share the input voltage together, Vs_1 equals with Vs_2 to $1/2\,V_{in}$. The state equations depicting this mode are

$$V_{in} = V_{s1} + V_{s2} + V_{sa} \tag{1}$$

$$V_{sa} = V_c + L_m \frac{dI_m}{dt} \tag{2}$$

$$C_{s1}\frac{dV_{s1}}{dt} = C_{s2}\frac{dV_{s2}}{dt} \tag{3}$$

$$\frac{dV_{s1}}{dt} + \frac{dV_{s2}}{dt} = -\frac{dV_{sa}}{dt} \tag{4}$$

$$C_{s1}\frac{dV_{s1}}{dt} - C_{sa}\frac{dV_{sa}}{dt} = I_m + nI_o \tag{5}$$

Mode (2) [t_1-t_2]: At $t = t_1$, switch voltage Vs_a falls to zero, the anti-parallel diode Ds_a of switch S_a is turned on, which starts conducting. Rectifier diode D_1 is turn off. Magnetizing current I_m is linearly decreased by V_c during this period. At t_2, switch S_a should be gated within this state to achieve Zero-Voltage-Switching turn-on. The magnetizing currents I_m is given by

$$I_m = I_m(t_1) - \frac{V_c}{L_m}(t - t_1) \tag{6}$$

Mode (3) [t_2-t_3]: At $t = t_2$, switch S_a turns on under ZVS. The magnetizing L_m still resonates with the capacitors C_c. During this period, I_m reverses its direction. The mode ends at t_3. I_m is given by

$$I_m = I_m(t_2) - \frac{V_c}{L_m}(t - t_2) \tag{7}$$

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Mode (4) [t_3-t_4]: At t=t_3, S_a is turned off. Magnetizing inductance L_m resonates again with Cs_1, Cs_2, Cs_a and C_c. During this period, Cs_a is charged, and then Cs_1 and Cs_2 are discharged with resonant manner. When Vs_1 and Vs_2 fall to zero, Vs_a rises to input voltage V_{in}. The state equations depicting this mode are

$$V_{in} = V_{s1} + V_{s2} + V_{sa} \tag{8}$$

$$V_{sa} = V_c + L_m \frac{dI_m}{dt} \tag{9}$$

$$C_{s1} \frac{dV_{s1}}{dt} = C_{s2} \frac{dV_{s2}}{dt} \tag{10}$$

$$\frac{dV_{s1}}{dt} + \frac{dV_{s2}}{dt} = -\frac{dV_{sa}}{dt} \tag{11}$$

$$C_{s1} \frac{dV_{s1}}{dt} - C_{sa} \frac{dV_{sa}}{dt} = I_m \tag{12}$$

Mode (5) [t_4-t_5]: At t=t_4, the switch voltage Vs_1 and Vs_2 decreases to zero, the anti-parallel diodes Ds_1 and Ds_2 are turned on. ZVS can be achieved for main switches S_1 and S_2. The mode ends at t_5.

Mode (6) [t_5-t_6]: At t=t_5, S_1 and S_2 turns on with ZVS, rectifier diode D_1 is turn on. During the period, current of the magnetizing inductance I_m

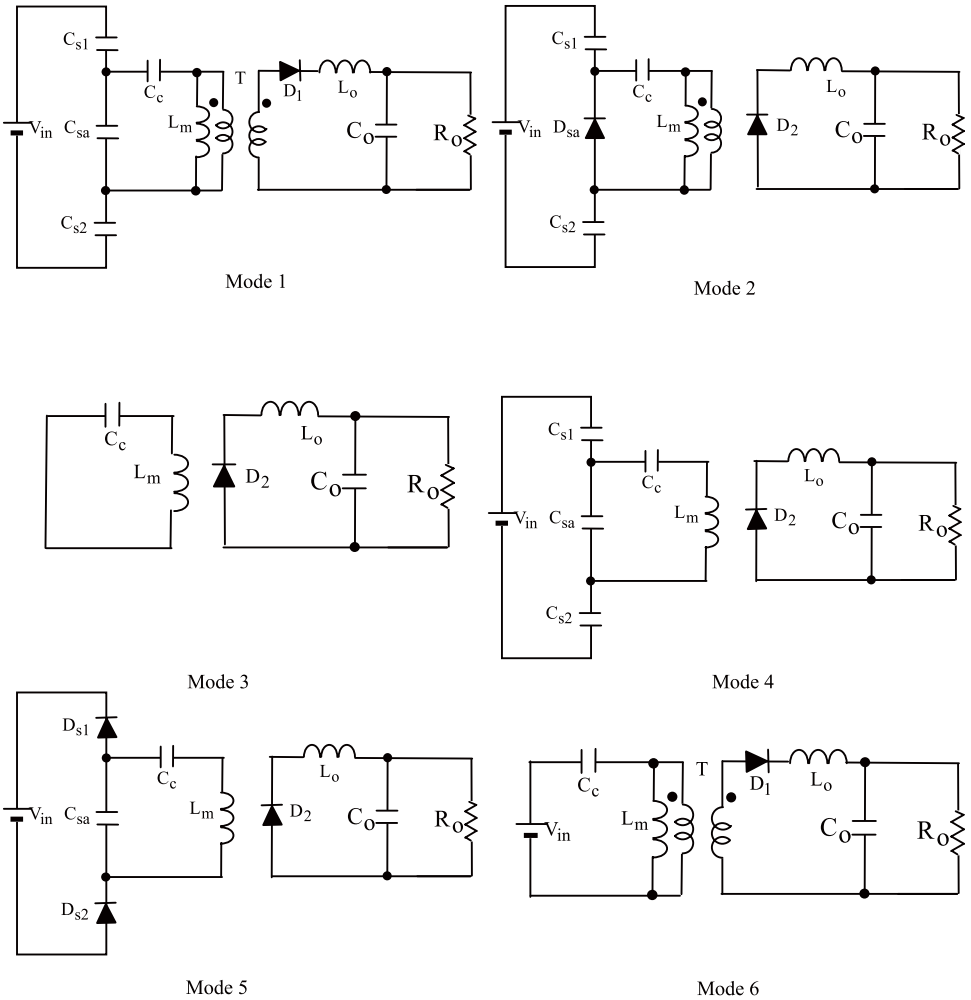

Fig. 2. Equivalent circuits of the proposed converter

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is linearly increasing by ($V_{in} - V_c$), and it is given by

$$I_m = I_m(t_5) + \frac{V_{in} - V_c}{L_m}(t - t_5) \tag{13}$$

4 Steady-state analysis

Steady-state operation of the proposed converter is same as conventional active clamp forward converter. As commutation time is very short which can be neglected. Since transformer must be reset in a switching cycle, Clamp capacitor voltage V_c can be obtained as the following equations.

$$V_c = V_{in} \times D \tag{14}$$

Where, D is the duty ratio of main switch S_1 and S_2, N is transformer turn ratio.

According to the volt-second balance relation, the output voltage can be derived as

$$V_o = \frac{V_{in} \times (1 - D)}{N} \times D \tag{15}$$

5 Simulation results

From the above analysis results, it can be seen that all switches can be turned on under ZVS. Voltage stress across main switches can be clamped at $1/2\,V_{in}$, voltage stress across auxiliary switch can be clamped at V_{in}. and due to C_c series with transformer, the lower output voltage can be got versus the conventional two switches forward converters and wide range can be achieved. To verify the conclusion, the specification of a model used in simulation is as follows.

1. Input voltage V_i=48 V;
2. Switch parasitic capacitor Cs_1=Cs_2=160 pF;
3. Clamp capacitor C_c=1 uF;
4. Leakage inductance L_l=3 uH
5. Magnetizing inductance Lm=187 uH
6. Transformer turn ratio n=5:1;
7. Switching frequency f_s=100 kHz;
8. Filter inductor L_o= 4 uH;
9. Filter capacitor C_o=470 uF;

The simulation waveforms for gate-source voltage and drain-source voltage of main switches and auxiliary switch at duty cycle=0.6 are shown in Fig. 3 (a) and (b), respectively. As can be seen in Fig. 3, stresses of main switches can be clamped at $1/2\,V_{in}$, stresses of auxiliary switch can be clamped at V_{in}. And all of switches are turned on under ZVS.

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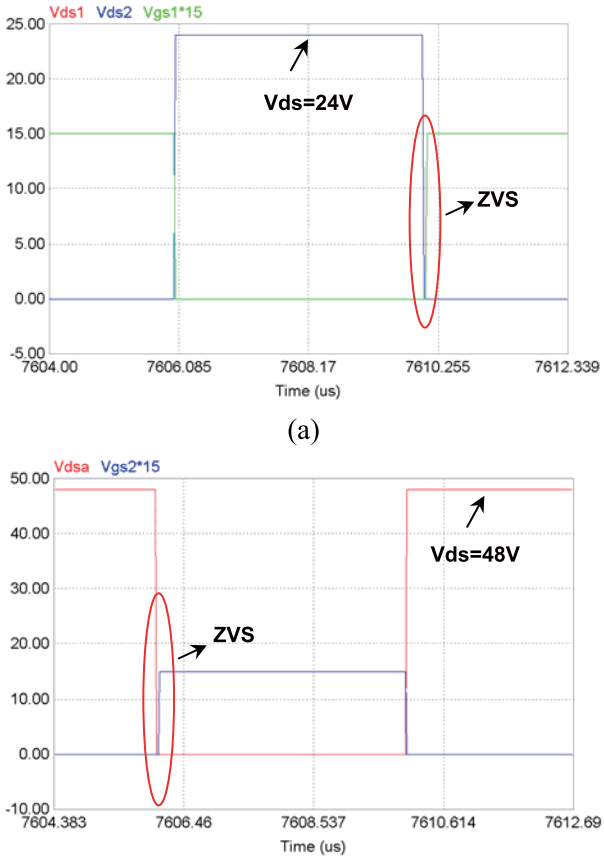

Fig. 3. Waveforms for gate-source voltage and drain-source voltage at D=0.6

6 Conclusion

This paper presents an improved soft-switching dual-switch forward converter topology. Its principle and its steady-state operation were analyzed. Analysis and simulation results have verified the following conclusions.

1. Voltage stresses of main switches were clamped at $1/2\,V_{in}$, and voltage stress of auxiliary switch was clamped at V_{in}.
2. Duty cycle can be more than 50%..
3. Soft switching was achieved for all switches.
4. Lower output voltage can be obtained.

Therefore, as a kind of better cost-effective approach, it is very attractive for high input, wide range and high efficiency application.

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