IEICE Electronics Express, Vol.7, No.7, 473–479

Design of a low-voltage CMOS mixer based on variable load technique

Baolin Wei[1a)], **Yujie Dai**[1], **Jun Wang**[2], **Toshimasa Matsuoka**[2b)], **and Kenji Taniguchi**[2]

[1] *Institute of Microelectronics, Nankai University*

4F, Section 5, TEDA college, Nankai University, no. 23 Hongda Street, TEDA, Tianjin 300457, P.R. China

[2] *Division of Electrical, Electronic and Information Engineering, Osaka University*

2–1 Yamada-oka, Suita, Osaka 565–0871, Japan

a) *guilinwxb@163.com*

b) *matsuoka@eei.eng.osaka-u.ac.jp*

Abstract: A CMOS active mixer based on variable load technique which can operate at 1.0 V supply voltage is proposed and its operation principle is presented. The proposed mixer controls the load impedance according to the LO signal. It has only two stacked transistors at each branch, which is suitable for low-voltage applications. The mixer was designed in 0.18-μm CMOS process and measured in 2.4-GHz ISM band. With a 2.440 GHz RF input signal and a 2.442 GHz LO signal (4 dBm), the conversion gain is 5.3 dB, the input-referred third-order intercept point is 4.6 dBm, the input-referred 1-dB compression point is −7.4 dBm, and the single-sideband noise figure is 21.7 dB. Current consumption is 3.5 mA at 1.0 V supply.

Keywords: CMOS active mixer, variable load technique, low-voltage

Classification: Integrated circuits

References

[1] M. B. Vahidfor and O. Shoaei, "A CMOS low voltage down-converter mixer for sub 1 V applications," *Proc. IEEE Workshop on Microelectronics and Electron. Devices*, Boise, pp. 5–6, April 2006.

[2] V. Vidojkovic and V. D. Tang, "A low- voltage folded-switching mixer in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1259–1264, June 2005.

[3] M. Harada, T. Tsukahara, J. Kodate, A. Yamagishi, and J. Yamada, "2-GHz RF front-end circuits in CMOS/SIMOX operating at an extremely low voltage of 0.5 V," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 2000–2004, Dec. 2000.

[4] H. H. Hsieh and L. H. Lu, "Designed of ultra-low-voltage RF front ends with complementary current-reused architectures," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 7, pp. 1445–1458, July 2007.

[5] C.-H. Chen, P.-Y. Chiang, and F. J. Christina, "A Low voltage mixer with improved noise figure," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 2, pp. 92–94, Feb. 2009.

DOI: 10.1587/elex.7.473
Received February 09, 2010
Accepted March 01, 2010
Published April 10, 2010

[6] R.-M. Weng, J.-C. Wang, and H.-C. Wei, "A 1 V 2.4 GHz down conversion folded mixer," *Proc. IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, pp. 1450–1452, Dec. 2006.
[7] B. Razavi, *Design of analog CMOS integrated circuits*, McGraw-Hill, New York, 2001.
[8] C. S. Kim, J.-W. Park, H. K. Yu, and H. Cho, "Gate layout and bonding pad structure of a RF n-MOSFET for low noise performance," *IEEE Electron Device Lett.*, vol. 21, no. 12, pp. 607–609, Dec. 2000.

1 Introduction

The essential goals in integrated circuit design are highly integrated, low voltage, low power, and so on. These characteristics are especially critical in mobile wireless communication systems due to the limitation of battery capacity. With the reducing scale of CMOS technologies, the key problem of migration to advanced CMOS technologies comes from continual reduction in supply voltages, resulting in poor performance in analog and RF circuits [1, 2]. Insufficient voltage headroom results in some circuit topologies unable to satisfy the required specifications or even unable to operate. Hence, research for low-voltage circuit topologies is important [1, 2, 3, 4, 5, 6].

Mixer is the core component in both transmitter and receiver, and it needs operate with low supply voltage and low power. The Gilbert-type mixer is the most mature mixer architecture widely used as the down-converter in CMOS superheterodyne receiver. Due to large number of stacked transistors at a low voltage supply and the voltage drops across the load resistors, the switching transistors and the transconductance stage of the mixer become critical, so this architecture cannot be used in CMOS advanced technologies which work with low supply voltage below 1 V [1, 2]. To reduce the supply voltages, some folded mixer architectures have been investigated in [2, 3] and [6], but they still have some drawbacks: insufficient linearity under low supply voltage and/or additional inductors increasing area occupation.

In this letter, a low-voltage CMOS down-conversion mixer controlling its variable load according to the LO signal to achieve mixing, is proposed. It was implemented in 0.18-μm CMOS process and measured in 2.4-GHz ISM band.

2 Proposed mixer based on variable load technique

The single balanced version of the proposed mixer enhances suitability for low-voltage applications based on variable load technique instead of RF current commutating, as shown in Fig. 1 (a). V_{B0} and V_B are DC bias voltage. Transistor M2 operating in triode region acts as the variable load. Its conductance $G_L(t)$ is controlled by the LO signal $v_{LO}(t)$, that is [7]:

$$G_L(t) = \beta_p(V_{OUT,B} - V_B - v_{LO}(t) - |V_{THP}|), \quad (1)$$

where β_p is the transconductance parameter, V_{THP} is the threshold voltage

DOI: 10.1587/elex.7.473
Received February 09, 2010
Accepted March 01, 2010
Published April 10, 2010

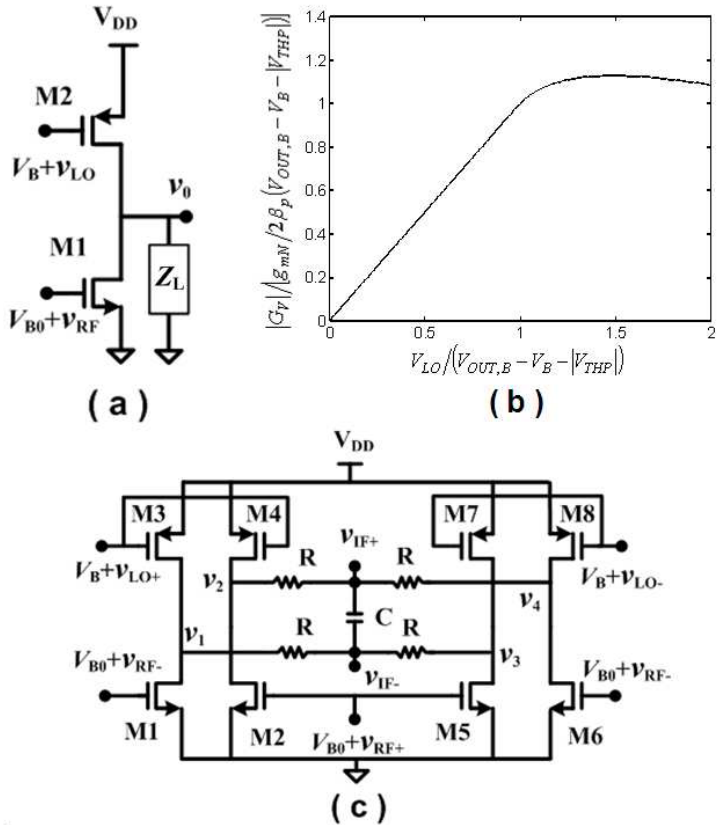

Fig. 1. The proposed mixer based on variable load technique. (a) Basic operation principle of the proposed single balanced mixer and (b) its voltage conversion gain (G_V) versus LO amplitude. (c) Double balanced version of the proposed variable load mixer.

of PMOS transistors, and $V_{OUT,B}$ is DC level at output terminal. In this study, $G_L(t) = 0$ in the case of $V_{OUT,B} - V_B - v_{LO}(t) - |V_{THP}| < 0$ for simplification. When $v_{LO}(t) = V_{LO} \sin \omega_{LO} t$, $G_L(t)$ can be expanded in a series of sinusoids.

$$G_L(t) = g_{L,0} + \sum_{n=1}^{\infty} g_{L,n} \sin(n\omega_{LO} t). \tag{2}$$

When $V_{LO} \leq V_{OUT,B} - V_B - |V_{THP}|$, $g_{L,0} = \beta_p(V_{OUT,B} - V_B - |V_{THP}|)$, $g_{L,1} = -\beta_p V_{LO}$, and $g_{L,n} = 0$ for $n > 1$. On the other hand, the harmonic components $g_{L,n}$ $(n = 3, 5, 7, \ldots)$ generate when $V_{LO} > V_{OUT,B} - V_B - |V_{THP}|$. In this case, $g_{L,0}$ and $g_{L,1}$ are given by

$$g_{L,0} = \beta_p V_{LO} \left[\left(\frac{1}{2} + \frac{\theta}{\pi} \right) \sin\theta + \frac{\cos\theta}{\pi} \right] \tag{3}$$

$$g_{L,1} = -\beta_p V_{LO} \left(\frac{1}{2} + \frac{\theta}{\pi} + \frac{\sin\theta \cos\theta}{\pi} \right), \tag{4}$$

where

$$\theta = \sin^{-1} \frac{V_{OUT,B} - V_B - |V_{THP}|}{V_{LO}}. \tag{5}$$

DOI: 10.1587/elex.7.473
Received February 09, 2010
Accepted March 01, 2010
Published April 10, 2010

Transistor M1 acts as the transconductance (g_m) stage, and operates in saturation region. To derive the down-conversion output voltage of the circuit, focusing on RF input and IF output frequencies, $v_{RF}(t)$ and $v_o(t)$ are expressed as

$$v_{RF}(t) = v_{rf}\exp(j\omega_{RF}t), \tag{6}$$

$$v_o(t) = v_{o,rf}\exp(j\omega_{RF}t) + v_{o,if}\exp(j(\omega_{RF}-\omega_{LO})t). \tag{7}$$

The relationship among v_{rf}, $v_{o,rf}$ and $v_{o,if}$ in Fig. 1 (a) can be written as

$$\begin{aligned} &v_{o,rf}\exp(j\omega_{RF}t) + v_{o,if}\exp(j(\omega_{RF}-\omega_{LO})t) \\ &= -Z_L(\omega_{RF})[g_{mN}v_{rf}\exp(j\omega_{RF}t) + g_{L,0}v_{o,rf}\exp(j\omega_{RF}t)] \\ &-Z_L(\omega_{RF}-\omega_{LO})[g_{L,0}v_{o,if}\exp(j(\omega_{RF}-\omega_{LO})t) \\ &+((jg_{L,1}/2)v_{o,rf}\exp(j(\omega_{RF}-\omega_{LO})t))], \end{aligned} \tag{8}$$

where g_{mN} is the transconductance of the NMOS M1. From this equation, $v_{o,rf}$ and $v_{o,if}$ are given by

$$v_{o,rf} = -\frac{g_{mN}Z_L(\omega_{RF})}{1+g_{L,0}Z_L(\omega_{RF})}v_{rf}, \tag{9}$$

$$v_{o,if} = -\frac{j}{2}\frac{g_{L,1}Z_L(\omega_{RF}-\omega_{LO})}{1+g_{L,0}Z_L(\omega_{RF}-\omega_{LO})}v_{o,rf}. \tag{10}$$

Thus, the voltage conversion gain (G_V) of the mixer is given by

$$G_V = \frac{v_{o,if}}{v_{rf}} = \frac{j}{2}\frac{g_{mN}Z_L(\omega_{RF})}{1+g_{L,0}Z_L(\omega_{RF})}\frac{g_{L,1}Z_L(\omega_{RF}-\omega_{LO})}{1+g_{L,0}Z_L(\omega_{RF}-\omega_{LO})}. \tag{11}$$

When $Z_L(\omega_{RF}), Z_L(\omega_{RF}-\omega_{LO}) \gg 1/g_{L,0}$, $|G_V|$ is $g_{mN}|g_{L,1}|/2g_{L,0}^2$. Figure 1 (b) shows dependence of the voltage conversion gain on LO amplitude V_{LO} in this case. In small LO amplitude region, the conversion gain increases proportionally to LO amplitude, which originates from $g_{L,1}$. With large LO amplitude, the conversion gain saturates and even decreases slightly due to increase in $g_{L,0}$. From these analytical results, to improve the voltage conversion gain, the β_p (i.e. W/L) of the PMOS should be decreased, and V_B and g_{mN} should be increased.

The mixer core proposed in Fig. 1 (a) has some shortcomings. Firstly, it can be seen from Eq. (9) that the RF feedthrough term exists in the output voltage, and it is larger than the mixing term. Secondly, the LO feedthrough will be found in the output if DC current of M1 is taken into account. To solve these shortcomings, the double balance structure is proposed as shown in Fig. 1 (c). It is composed of four parts identical to Fig. 1 (a), four resistors R are used to sum the transconductance stages' output voltage, so it can cancel the RF term in the output voltage of the single balanced version. The four resistors R and capacitor C also act as a low-pass-filter to filter the high-order harmonic of the mixing output.

Based on Eqs. (9) and (10), the drain voltage at M1, M2, M5 and M6, namely v_1, v_2, v_3 and v_4 in Fig. 1 (c) are

$$v_{1(,2,3,4)} = \left(1-\frac{j}{2}\frac{(\pm g_{L,1})}{g_{L,0}}\right)\frac{g_{mN}}{g_{L,0}}(\mp v_{RF}), \tag{12}$$

DOI: 10.1587/elex.7.473
Received February 09, 2010
Accepted March 01, 2010
Published April 10, 2010

where $Z_L(\omega_{RF}), Z_L(\omega_{RF}-\omega_{LO}) \gg 1/g_{L,0}$ for simplification. The first and second terms of the left hand side in Eq. (12) means RF and IF components, respectively. Thus

$$v_{IF+} - v_{IF-} = \frac{v_2 + v_4}{2} - \frac{v_1 + v_3}{2} = -\frac{j}{2}\frac{g_{mN} g_{L,1}}{g_{L,0}^2}(v_{RF+} - v_{RF-}). \quad (13)$$

It can be seen from Eq. (13) that the RF term in the output voltage is canceled.

The proposed mixer in this letter is based on variable load technique. The load transistors (M3-M4 and M7-M8) operate in triode region during the LO signal period, resulting in their resistances ($1/G_L(t)$) controlled by the LO signal. Thus the output has a voltage term to achieve mixing. It can easily operate at sub 1 V low supply voltage because it has only two stacked transistors at each branch.

3 Proposed mixer design and measurement results

The double balanced version of the proposed mixer which is depicted in Fig. 1 (c) had been fabricated in 0.18-μm CMOS process. Its micrograph is shown in Fig. 2 (a). The occupation area is $0.53 \times 0.405\,\text{mm}^2$, including the pads and ESDs. The active chip area is $0.15 \times 0.14\,\text{mm}^2$. To avoid mismatches, all the transistors and metal connections in the circuit was placed as symmetrically as possible [8]. Transistors with non-minimum channel lengths

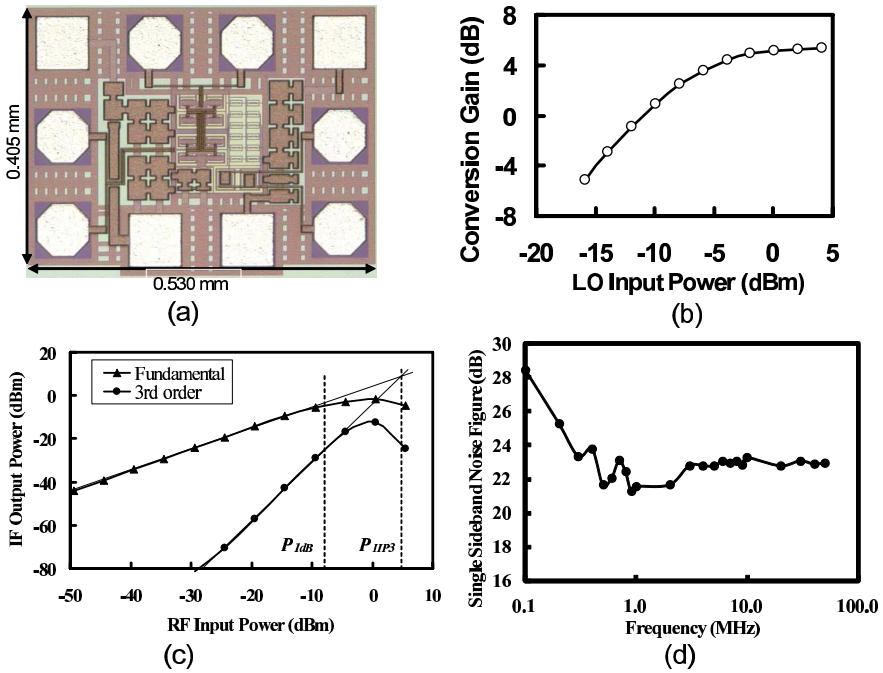

Fig. 2. Micrograph and measurement results of the fabricated mixer, (a) Micrograph, (b) Measured conversion gain versus LO input power, (c) Two-tone harmonic measurement results with an input frequency spacing of 200 kHz, (d) Single side-band noise figure versus frequency.

DOI: 10.1587/elex.7.473
Received February 09, 2010
Accepted March 01, 2010
Published April 10, 2010

were used to optimize the linearity, $1/f$ noise, and device matching. The gate lengths of NMOS in g_m stage are 0.5 μm and the widths are 100 μm, and the W/L ratios of PMOS are 160 μm/0.2 μm. In the RC network, R and C are 3.4 kΩ and 0.5 pF, respectively. All high frequency signals (i.e. RF and LO signals) were routed on the top or upper metal layer to reduce parasitic capacitances.

The fabricated mixer was measured in 2.4-GHz ISM band with a supply voltage of 1.0 V using on-wafer RF probes. The DC bias voltages of V_{B0} and V_B are 0.65 V and 0.25 V, respectively. It draws 875μA DC current at each branch from the supply. The RF signal frequency was 2.440 GHz, and the LO port was driven by a 2.442 GHz LO signal. The typical LO power was set at 4 dBm, corresponding to $V_{LO} \approx 0.5$ V at the gate of PMOS. The RF signal powers have been corrected to compensate for the insertion loss of the passive balun, input matching circuit, cable and probe. The measurement results are also shown in Fig. 2. Figure 2 (b) reveals operation of the proposed mixer shown in Fig. 1 (b). Figure 2 (c) illustrates the measured intermodulation distortion versus the RF input power at the input RF frequencies of 2.4401 GHz and 2.4399 GHz, indicating the input-referred third-order intercept point in power (P_{IIP3}) is 4.6 dBm and the input-referred 1-dB compression point (P_{1dB}) is -7.4 dBm.

The single-sideband noise figure (NF_{SSB}) versus frequency is illustrated in Fig. 2 (d). The measurement result shows a NF_{SSB} of 21.7 dB at the IF frequency. As the resistances in the RC filter contribute considerable noise to the output, the mixer's noise figure is degraded. However, this SSB noise figure can be acceptable since the noise term contributed from the mixer will be compressed by the low-noise-amplifier gain as for the total noise figure of the front-end receiver.

The main performance of the proposed mixer is summarized in Table I, and compared with several published low-voltage mixers. It can be seen that

Table I. Summary of results and performance comparison.

Parameter	This work	[2]	[3]	[5]	[6]*
Supply Voltage (V)	1.0	1.0	1.0	1.0	1.0
CG (dB)	5.3	11.9	6.7	5.8	10.1
P_{1dB} (dBm)	-7.4	–	-15.5	-16.0	-25.4
P_{IIP3} (dBm)	4.6	-3.0	-6.0	-6.0	-17.0
NF_{SSB} (dB)	21.7	13.9	16.1	16.0	–
RF–IF Isolation (dB)	61.5	–	–	39	–
LO–IF Isolation (dB)	63.3	–	–	57	–
Total DC Current (mA)	3.5	3.2	19.0	3.8	12.5
Occupation Area (mm^2)	0.53× 0.405	0.16× 0.20**	–	1.042× 1.102	1.38× 1.38

* Simulation results
** Only active occupation area

DOI: 10.1587/elex.7.473
Received February 09, 2010
Accepted March 01, 2010
Published April 10, 2010

the linearity performance of the proposed mixer is more competitive. High linearity performance is very important in the front-end receiver because the linearity of mixer has great impact to the dynamic range of the receiver. This is a serious issue in low-voltage mixer design. Though the conversion gain (CG) of the mixers in [5] and [6] are larger than that of this work, there are 4 or 5 inductors in these mixers which would augment their occupation area. This point also becomes important for low-cost chip fabrication even in more advanced CMOS process.

4 Conclusion

A novel low-voltage CMOS active mixer was proposed and implemented in 0.18-μm CMOS process. The PMOS transistors operating in triode region are used to act as the active load controlled by the LO signal. This mixer generates the output having down-conversion term. Measurement results show that its linearity performance, the single sideband noise figure, and conversion gain performance are acceptable even under 1.0 V supply voltage. We expect the proposed mixer can operate at lower voltage in more advanced CMOS process technology due to circuit topology of two stacked transistors, and its small area occupation is suitable for low-cost fabrication.

Acknowledgment

The authors would like to thank the Osaka University Global COE Program "Center for Electronic Devices Innovation" from the Ministry of Education, Culture, Sports, Science and Technology of Japan, for sponsoring this work.

DOI: 10.1587/elex.7.473
Received February 09, 2010
Accepted March 01, 2010
Published April 10, 2010