

# CCS: A low-power capacitively charge-sharing transmitter for NoC links

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**Abstract:** In this letter, a capacitively charge-sharing transmitter (CCS) is proposed as a novel design to replace the traditional differential capacitive pre-emphasis transmitter (CPE), for the purpose of reducing the dynamic power consumption by half. The CCS functions as a transmitter for mesh NoC links to achieve high-speed and low-power transmission. CCS generates a pair of differential low-swing signals at a time through charge-sharing. Its capacitively driven mode enables high-speed transmission and provides pre-emphasis to extend the bandwidth. Simulation shows that CCS can achieve 9 Gb/s data rate over 2 mm twisted differential interconnects with only 56.4 fJ/b power consumption. With a clockless hysteresis receiver, the transceiver for NoC links enables a data rate of 7 Gb/s with at least 70% eye-opening while consumes only 90.8 fJ/b.

**Keywords:** charge-sharing, low-swing, capacitively driven, low-power, interconnect, network-on-chip (NoC)

**Classification:** Integrated circuits

## References

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## 1 Introduction

With the increasing number of cores on chips, network-on-chip (NoC) technology becomes increasingly popular today by providing a new

interconnection solution with flexible expansibility to replace complex system-on-chip (SoC). However, the power consumption could be still high in NoCs which has long interconnects with heavy loads [1, 2]. Low-swing technology can effectively reduce the power consumption and improve the signal transmission. Based on this technology, various low-swing transmitters were proposed. In the designs, low swings can be realized by introducing a multi- $V_{DD}$  circuit [1, 3]. Another capacitive pre-emphasis transmitter (CPE) has been widely used because it greatly extends the bandwidth to increase achievable data rate [4, 5, 6]. In a recent paper [7], a transmitter based on charge-sharing (CS) emerged as a new approach to generate low swings. While it is difficult for CS to drive long interconnects, due to the large loads offer a large time constant which decreased the switching speed and limited the data rate.

A novel capacitively charge-sharing transmitter (CCS) is proposed to further reduce the power consumption while maintaining a high data rate in mesh NoC links. The high-speed transmission is achieved through capacitively driven mode. Meanwhile, the bandwidth is further extended due to the pre-emphasis provided by series capacitances. The dynamic power consumption of the proposed CCS is only the half of that of differential CPE.

## 2 Capacitively charge-sharing transmitter (CCS)

Fig. 1 (a) depicts the architecture of the proposed NoC links. It is composed of transmitters (TXs), long interconnects, and receivers (RXs). The proposed CCS functions as the transmitter to generate differential low-swing signals while the twisted differential interconnects is used to restrain the noise and crosstalk. AC-coupled resistive feedback inverters (RFIs) [6] offer  $V_{DD}/2$  bias at the receiving end, and a hysteresis receiver restores the biased signals to full-swing.

### 2.1 Working principle and low-power feature

The circuit diagram of the proposed CCS is shown in Fig. 1 (b). The charges distribution on the nodes A and B in a clock period are as follows.

(i) when  $V_{in}=0$ , both P1 and N1 are on, thus the potentials on the nodes A and B are  $V_{DD}$  and 0, respectively. As a result, the charges stored on the nodes A and B are

$$Q_{A(i)} = (C_1//C_W)V_{DD}, \quad Q_{B(i)} = 0. \quad (1)$$

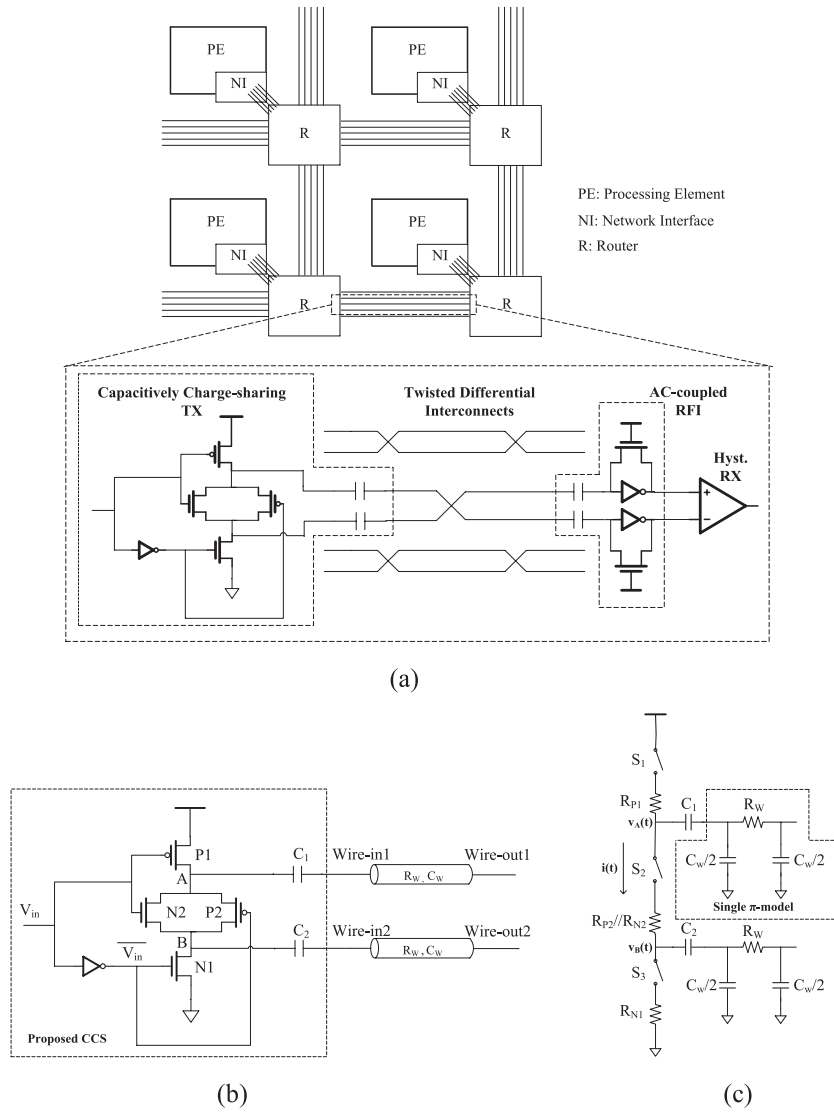
(ii) when  $V_{in}=V_{DD}$ , P1 and N1 are off, while P2 and N2 are on, which enables charges sharing between the two nodes A and B. Therefore, the charges on the two nodes are decreased and increased to

$$Q_{A(ii)} = \frac{(C_1//C_W)^2}{C_1//C_W + C_2//C_W} V_{DD}, \quad Q_{B(ii)} = \frac{(C_1//C_W)(C_2//C_W)}{C_1//C_W + C_2//C_W} V_{DD}, \quad (2)$$

respectively. Therefore, the potential on the nodes A and B becomes

$$V_A = V_B = \frac{C_1//C_W}{C_1//C_W + C_2//C_W} V_{DD}. \quad (3)$$

(iii) when  $V_{in}=0$ , repeat process (i).



**Fig. 1.** (a) The links in a mesh NoC. (b) The proposed CCS. (c) The equivalent model of CCS with single  $\pi$ -model interconnects.

In the process above, swings on the nodes A and B can be calculated by

$$V_{swing(A)} = \left(1 - \frac{C_1 // C_W}{C_1 // C_W + C_2 // C_W}\right) V_{DD} \quad (4)$$

$$V_{swing(B)} = \frac{C_1 // C_W}{C_1 // C_W + C_2 // C_W} V_{DD}. \quad (5)$$

The driven capacitances  $C_1$  and  $C_2$  are in series with the load capacitance  $C_W$ , hence, the swings on the wires can be calculated by

$$V_{swing(wire1)} = V_{swing(A)} \left( \frac{C_1}{C_1 // C_W} \right) = \left( \frac{C_1 C_2}{2C_1 C_2 + C_1 C_W + C_2 C_W} \right) V_{DD} \quad (6)$$

$$V_{swing(wire2)} = V_{swing(B)} \left( \frac{C_2}{C_2 // C_W} \right) = \left( \frac{C_1 C_2}{2C_1 C_2 + C_1 C_W + C_2 C_W} \right) V_{DD}. \quad (7)$$

Eqs. (6) and (7) show that, even if  $C_1$  is not equal to  $C_2$ , the swings on Wire1 and Wire2 are still the same, which means that CCS can eliminate

the mismatch between  $C_1$  and  $C_2$ .

In this letter, it is assumed that  $C_1=C_2=C_T$ , and the final swings on the wires can be expressed as

$$V_{swing} = \frac{C_T}{2(C_T + C_W)} V_{DD}. \quad (8)$$

The dynamic power consumption of  $1 \rightarrow 0$  transition can be calculated by

$$\begin{aligned} E_{1 \rightarrow 0} &= \int_0^\infty i_{VDD}(t) V_{DD} dt = (C_T / C_W) V_{DD} \int_{V_{DD}/2}^{V_{DD}} dv_A \\ &= \frac{(C_T / C_W) V_{DD}^2}{2} \Leftrightarrow C_W V_{DD} V_{swing}. \end{aligned} \quad (9)$$

While the  $0 \rightarrow 1$  transition draws almost no energy from the power supply, which makes  $E_{0 \rightarrow 1}$  almost zero. The dynamic power consumption of traditional differential low-swing circuits reaches to  $2 \cdot C_W V_{DD} V_{swing}$  in a clock period. In other words, the dynamic power consumption of CCS can be reduced to half of that of the traditional differential ones on the premise of the same swing according to Eq. (9).

## 2.2 Delay reduction and bandwidth extension

Fig. 1 (c) shows the equivalent model of the CCS described in Fig. 1 (b). The single  $\pi$  model is employed to estimate the delay of interconnects. The potentials on the nodes A and B are expressed as  $v_A(t)$  and  $v_B(t)$ , respectively, and  $i(t)$  refers to the current flowing through P2 and N2. The time constant of charge-sharing in process (ii) can be calculated as follows:

When S2 is off, the initial state of this circuit can be expressed as

$$v_A(0^-) = V_{DD}, v_B(0^-) = 0, i(0^-) = 0. \quad (10)$$

When S2 is on, charge-sharing occurs which leads to

$$i(0^+) = \frac{V_{DD}}{R_{P2} // R_{N2}}, i(\infty) = 0 \quad (11)$$

$$v_A(0^+) = V_{DD}, v_B(0^+) = 0, v_A(\infty) = v_B(\infty) = \frac{C_1 V_{DD}}{C_1 + C_2} \quad (12)$$

$$v_A(t) - v_B(t) = (R_{P2} // R_{N2}) \cdot i(t). \quad (13)$$

The current  $i(t)$  can be written as

$$i(t) = -C_1 \frac{dv_A(t)}{dt} = C_2 \frac{dv_B(t)}{dt}. \quad (14)$$

Based on Eqs. (11), (13), (14),  $i(t)$  is derived as

$$i(t) = \frac{V_{DD}}{R_{P2} // R_{N2}} e^{-t / (R_{P2} // R_{N2}) \left( \frac{C_1 C_2}{C_1 + C_2} \right)}. \quad (15)$$

Finally,  $v_A(t)$  and  $v_B(t)$  are obtained according to Eqs. (12), (14), (15), as follows:

$$v_A(t) = \frac{C_1 V_{DD}}{C_1 + C_2} \left[ 1 + \frac{C_2}{C_1} e^{-t/(R_{P2} // R_{N2}) \left( \frac{C_1 C_2}{C_1 + C_2} \right)} \right] \quad (16)$$

$$v_B(t) = \frac{C_1 V_{DD}}{C_1 + C_2} \left[ 1 - e^{-t/(R_{P2} // R_{N2}) \left( \frac{C_1 C_2}{C_1 + C_2} \right)} \right]. \quad (17)$$

According to Eqs. (16) and (17), the time constant of charge-sharing can be written as  $(R_{P2} // R_{N2}) \left( \frac{C_1 C_2}{C_1 + C_2} \right)$ , hence, the total time constant [4, 6] in process (i) and (ii) becomes

$$\tau_{(i)} \approx R_{P1(N1)} C_{1(2)} + \frac{1}{4} R_W C_W \quad (18)$$

$$\tau_{(ii)} \approx R_{P2(N2)} \left( \frac{C_1 C_2}{C_1 + C_2} \right) + \frac{1}{4} R_W C_W. \quad (19)$$

Derived time constants of different transmitters in raising and falling cases are shown in Table I. It is observed that the coefficient of item  $R_W C_W$  is the main factor that affects the time constant due to the large load resistances and capacitances. This coefficient is 1/2 in Full-swing, Multi- $V_{DD}$  and CS, while 1/4 in CPE and CCS. It is thus concluded that the delay is significantly reduced with the capacitively driven mode.

**Table I .** Time constants of different transmitters.

Time constant		$\tau_{\text{raising}}$	$\tau_{\text{falling}}$
CCS	Wire-out1	$R_{P1} C_T + \frac{1}{4} R_W C_W$	$\frac{1}{2} (R_{P2} // R_{N2}) C_T + \frac{1}{4} R_W C_W$
	Wire-out2	$\frac{1}{2} (R_{P2} // R_{N2}) C_T + \frac{1}{4} R_W C_W$	$R_{N1} C_T + \frac{1}{4} R_W C_W$
CS	Wire-out1	$R_{P1} C_W + \frac{1}{2} R_W C_W$	$\frac{1}{2} (R_{P2} // R_{N2}) C_W + \frac{1}{2} R_W C_W$
	Wire-out2	$\frac{1}{2} (R_{P2} // R_{N2}) C_W + \frac{1}{2} R_W C_W$	$R_{N1} C_W + \frac{1}{2} R_W C_W$
CPE	Wire-out1/2	$R_P C_T + \frac{1}{4} R_W C_W$	$R_N C_T + \frac{1}{4} R_W C_W$
Multi- $V_{DD}$	Wire-out1/2	$R_P C_W + \frac{1}{2} R_W C_W$	
Full-swing	Wire-out1/2	$R_P C_W + \frac{1}{2} R_W C_W$	$R_N C_W + \frac{1}{2} R_W C_W$

Signal transaction causes an overshoot on coupled capacitances at Wire-in which provides pre-emphasis, and the introduced driven capacitance  $C_T$  moves the pole of transfer function from  $2/R_W C_W$  to  $4/R_W C_W$ . Hence, the bandwidth is extended substantially.

### 2.3 Comparison of transmitters

The simulated results of different transmitters are shown in Table II. The characteristics of Full-swing, Multi- $V_{DD}$ , and CPE can be obtained from [1]. In this letter, the parameters of CCS and CS based on 1.2 V 130 nm CMOS process are acquired from Cadence spectre. Interconnects are placed in metal 4 with both a width and a spacing of  $0.4 \mu\text{m}$ . Under this condition, the total distributed resistance and capacitance of a 2 mm wire is  $270 \Omega$  and 450 fF, respectively. As can be seen from Table II, the power consumption of CCS and CPE is 56.4 fJ/b and 105 fJ/b, respectively. Therefore,

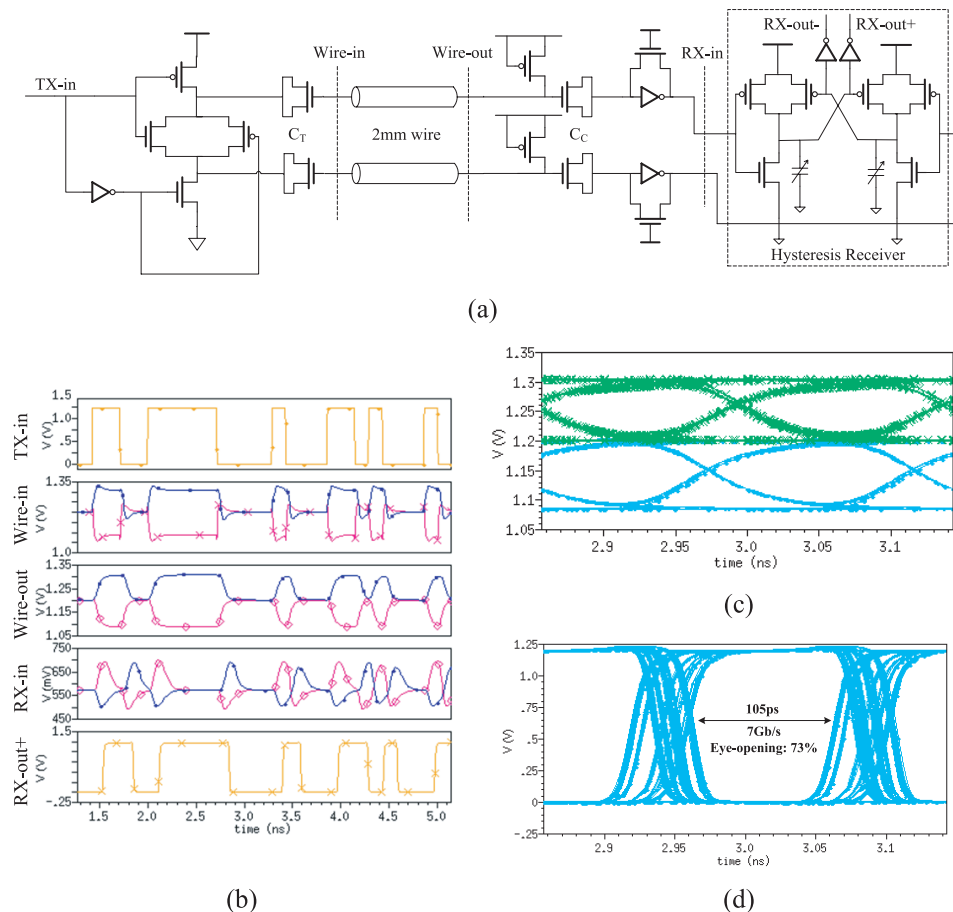
**Table II.** Characteristics of different transmitters.

Transmitter type	Full-swing	Multi- $V_{DD}$	CPE	CS	CCS
Technology	1.2V 90nm 6M CMOS			1.2V 130nm 6M CMOS	
Signaling type	Single ended	Twisted differential			
Power supply	1.2V	$V_{DDH}=1.2V$ $V_{DDL}=1.08V$	1.2V	1.2V	1.2V
Voltage swing	1.2V	120mV	120mV	0.6V	120mV
Energy/bit	420fJ/b	135fJ/b	105fJ/b	167fJ/b	56.4fJ/b
Data rate (≥50% eye-opening)	5Gb/s	5Gb/s	9Gb/s	5Gb/s	9Gb/s
Delay (50%) Typical/Slow	105ps/150ps	90ps/130ps	60ps/80ps	107ps/115ps	63ps/77ps

achieving the same data rate of 9 Gb/s, CCS can reduce the power consumption of the transmitter almost by half compared to CPE. Table II also shows that, the delay of CCS is only 63 ps at the typical process corner, and increases to 77 ps at the slow process corner, which is quite similar to that of CPE.

### 3 Simulation of overall transceiver

An overall transceiver shown in Fig. 2 (a) is obtained by connecting CCS with a clockless hysteresis receiver. Low-swing signals are restored to full-swing due to the contention between NMOS transistors and cross-coupled PMOS transistors in the receiver, and the DC voltage of the wires is biased



**Fig. 2.** (a) Schematic of overall transceiver. (b) Simulated transient waveforms at 7 Gb/s. (c) Eye-diagram at Wire-out. (d) Eye-diagram at RX-out+.

to  $V_{DD}/2$  with AC-coupled RFIs.  $C_T$  and  $C_C$  are realized by NMOS capacitances, and the areas they consume are  $3.0 \times 3.0$  and  $1.6 \times 1.6 \mu\text{m}^2$  to have capacitances of 110 and 30 fF, respectively. The PMOS pull-ups as resistances at Wire-out offer a high gate-source voltage to make the NMOS capacitances exhibit largest. Simulated transient waveforms at 7 Gb/s are shown in Fig. 2 (b), signals are pre-emphasized at Wire-in and converted to RZ pulses at RX-in. The simulated eye-diagram is of high quality at Wire-out and still keeps 73% opening at RX-out+, as shown in Figs. 2 (c) and (d). This whole transceiver consumes only 635.6 mW (i.e., 90.8 fJ/b).

#### 4 Conclusion

In this letter, a high-speed and low-power CCS is proposed as a low-swing transmitter for mesh NoC links. The CCS enables high data rate through capacitively driven mode and decreased its dynamic power consumption by 50% through charge-sharing compared to CPE. Thus, CPE can be replaced by CCS to further reduce the power consumption. Low-swing signals are restored to full-swing with a clockless hysteresis receiver. Simulations of the transceiver for 2 mm interconnects are realized in Cadence spectre. Simulated results demonstrate that CCS achieves 9 Gb/s data rate with at least 50% eye-opening and consumes only 56.4 fJ/b. The whole transceiver enables a data rate of 7 Gb/s with 73% eye-opening, and the total power consumption is only 90.8 fJ/b.

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