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A low DC offset direct conversion receiver for W-CDMA with low current consumption

Hiroshi Yoshida[1a)], **Takehiko Toyoda**[2], **Tadashi Arai**[2], **and Hiroshi Tsurumi**[2]

[1] *Corporate Research & Development Center, Toshiba Corp., Kawasaki, 210–8582 Japan*

[2] *Analog RF System LSI Engineering Dept., Semiconductor Company, Toshiba Corp., Yokohama, 247–8585 Japan*

a) *hiroshi7.yoshida@toshiba.co.jp*

Abstract: We present evaluation results for DC offset in the direct conversion receiver for W-CDMA with low current consumption. Measured results indicate that steady-state DC offset is suppressed to less than 30 mV and transitional variation in DC offset with gain change is limited to around 100 mV. The computer simulation revealed that negligible degradation in bit error rate (BER) performance due to the DC offset transition occurs with the proposed receiver.

Keywords: direct conversion, DC offset, BER performance

Classification: Integrated circuits

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1 Introduction

Direct conversion systems are a candidate for realizing small-size and low-cost mobile terminals since they require no IF components such as bulky IF filters. However, in a direct conversion system, DC offset resulting from the second-order distortion in a QDEM (Quadrature DEModulator) or self-mixing due to LO (Local Oscillator) leakage significantly degrades the receiver performance [1]. Hence, it is important to reduce DC offset in a direct conversion system. In a steady-state, since the DC offset is constant, it can be eliminated by means of DC offset canceling techniques such as a DC offset canceler. However, since received signal strength varies widely, i.e. more than 80 dB in handheld terminals for a mobile communication system such as W-CDMA, the gain of the entire receiver chain changes according to the received signal for automatic gain control (AGC). Consequently, when gain change occurs, the DC offset varies transitionally with the high-pass characteristic time constant for a DC offset canceler. Therefore, a reduction in DC offset transition for the gain change is also required for mobile communication terminals. We have previously reported a fully differential direct conversion receiver, which reduced DC offset including time variation [2]. In [2], we reported that DC offset variation is sufficiently suppressed and causes negligible degradation in receiver performance. However, a large current of 64.0 mA was consumed by the entire receiver chain. Hence, we have developed an improved direct conversion receiver with current consumption of 30.8 mA [3]. In [3], we described power consumption of the receiver and the major evaluation results such as NF, 2nd and 3rd order distortion but not DC offset. The main subject of this paper is evaluation of DC offset in the receiver and verification that the receiver performance is not degraded due to the DC offset. First, the measured results for DC offset including transitional variation are presented, and then computer simulation results for bit error rate (BER) performance in the presence of the measured DC offset are shown.

2 Configuration of the proposed receiver

In the proposed receiver, the following approaches are introduced in order to reduce power consumption.

- A double-balanced mixer is adopted for a QDEM as an alternative architecture to the active harmonic mixer, which was introduced in the previous work [2]. The LO buffer employs capacitor degeneration in order to suppress the DC offset injection to the mixer, which causes local leakage, without an active DC offset canceler. Thus, rise in power consumption is prevented.

- The synthesizer, including an on-chip VCO (Voltage-Controlled Oscillator), which oscillates at twice the received frequency, i.e. 4 GHz band, is integrated into the receiver IC, in which orthogonal LO signals are generated by a phase shifter comprised of a divider. Adoption of twice the received frequency for the VCO suppresses the self-mixing in the

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QDEM, because there is no inherent self-mixing component for the VCO.

- A single-ended configuration is employed for a low-noise amplifier (LNA) IC. Although a differential LNA can suppress the local signal leakage which causes DC offset, it consumes much greater power than a single-ended LNA. In the proposed receiver, an LNA IC is excluded from the receiver IC to increase isolation for LO leakage so as to enable adoption of low-power single-ended architecture.

The block-diagram for the receiver is shown in Fig. 1. The receiver consists of the LNA-IC, the receiver IC, and an external RF-SAW (Surface Acoustic Wave) filter. The receiver IC integrates a QDEM, baseband LPFs (Low-Pass Filters), VGAs (Variable Gain Amplifiers) with active DC offset cancelers, and a frequency synthesizer.

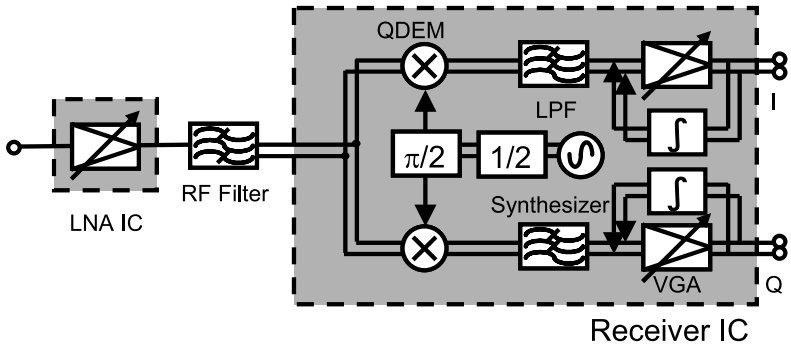

Fig. 1. Configuration of the receiver.

3 Evaluation results for DC offset including transitional variation

In this chapter, evaluation results for local leakage, steady-state DC offset, and DC offset transition at gain change are described.

3.1 LO leakage

Since the LO leakage causes self-mixing in a QDEM due to reflection from the receiver front-end, reduction in LO leakage is required in a direct conversion system. In the proposed system, LO leakage of less than −50 dBm is required to avoid saturation in baseband circuits due to DC offset. Measured LO leakage at the input port of the QDEM is shown in Fig. 2 (a). The differential LO leakage power at a center frequency of 2140 MHz was sufficiently suppressed to −55 dBm.

3.2 Steady-state DC offset

The measured results for steady-state DC offset with respect to a normalized receiver gain are shown in Fig. 2 (b). Although steady-state DC offset performance was degraded as the receiver gain was increased as shown in the

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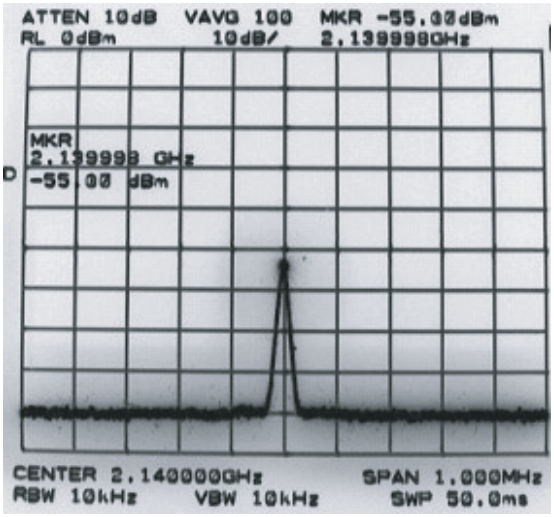
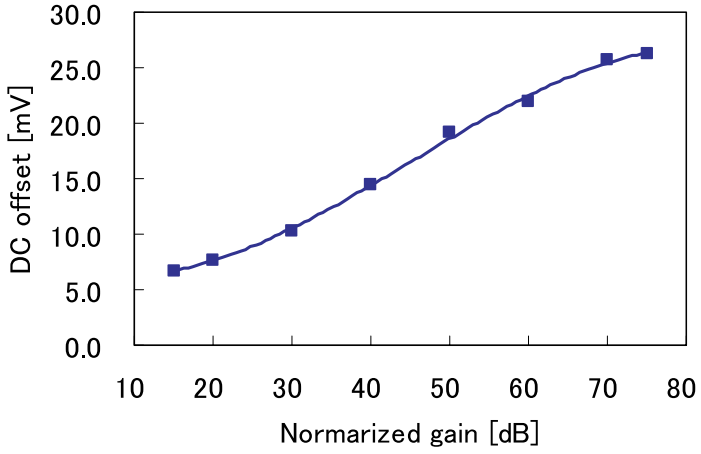
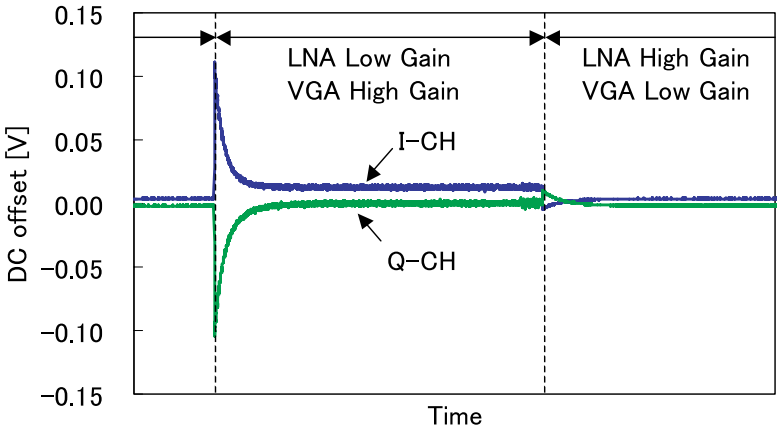


(a)



(b)



(c)

Fig. 2. Evaluation results for DC offset. (a) LO leak from the receiver IC., (b) DC offset in steady-state., (c) DC offset variation with gain change in LNA and VGA simultaneously.

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figure, less than 30 mV DC offset was observed even at the maximum gain. Thus, steady-state DC offset was sufficiently suppressed to less than −30 dB compared to the maximum output voltage of the receiver, i.e. 1.0 V_{p-p}. The reason DC offset is increased in the high-gain region is that DC offset suppression decreases as gain increases. This is because the frequency response of the low-pass filter included in the feedback path of a DC offset canceler depends on gain and its feedback gain is reduced in the high-gain region [4].

3.3 DC offset variation with gain change

Fig. 2 (c) shows measured results for the DC offset variation with gain change. This figure shows output voltage of the receiver with periodical gain change of the LNA and VGAs simultaneously. In this measurement, the total receiver gain remained constant at 47 dB, which is the gain change point of the LNA. The VGA gain was 26 dB while the LNA gain was low (−10 dB) and the VGA gain was −1 dB while the LNA gain was high (17 dB), and the sum of gains in the rest of the receiver chain was 31 dB. The largest DC offset transition occurred when the LNA gain decreased, and peak voltages for the DC offset transition of 106 mV for I-channel and 96 mV for Q-channel were observed, respectively, whereas the steady-state DC offset was less than 15 mV for each channel. Although some increase in transitional variation of DC offset was observed compared to that in the previous study, i.e. 70 mV, it was suppressed to quite a low level. In addition, the performance due to the transitional variation of the DC offset is verified in the next section.

4 Simulation results for BER performance

In order to evaluate the performance degradation for the receiver chain caused by the DC offset transition, the BER performance was computer simulated under 3 GPP standard conditions [5]. In this simulation, measured results for the DC offset including time variation were superimposed on the received signal and then demodulated to evaluate BER performance. The VGA output signal amplitude was 104 dBμ, and the AGC gain change interval was assumed to be 10 msec. The simulation result for BER performance with

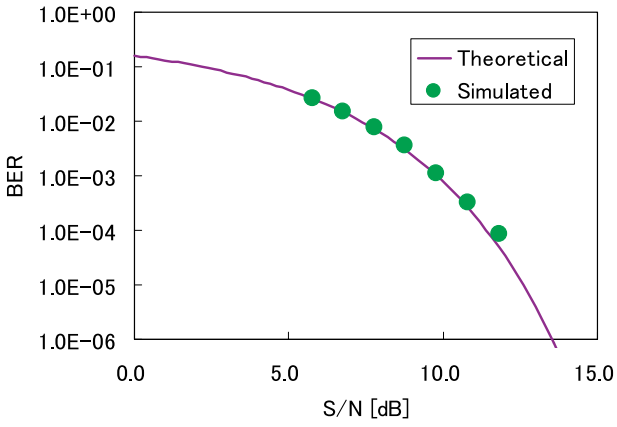

Fig. 3. Simulation results for BER performance.

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respect to S/N is shown in Fig. 3. This simulation result indicates that degradation in the BER performance of less than 0.1 dB was observed for the proposed receiver at a BER of 10^{-3}.

5 Conclusions

A low DC offset direct conversion receiver for W-CDMA with low current consumption was presented. The measured results for the steady-state DC offset were reduced to quite a low level, i.e. less than 30 mV, which is −30 dB compared to the maximum output voltage of the receiver. The transitional variation in the DC offset with gain change, which is the main factor affecting reception for W-CDMA terminals, was suppressed to around 100 mV. The computer simulation result for BER performance indicated that negligible performance degradation due to the DC offset would occur with the proposed receiver.

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