

Characterization of punch-through phenomenon in SiC-SBD by capacitance-voltage measurement at high reverse bias voltage

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Abstract: This paper investigates the punch-through phenomenon in SiC Schottky Barrier Diodes (SBD) from capacitance–voltage (C–V) characteristics at high reverse bias voltage. High voltage bias application has not been possible by conventional measurement instrumentation. The authors, therefore, develop C–V characteristics measurement instrumentation which enables the application of high dc bias voltages on SiC-SBD up to the rated reverse blocking voltage. The measurement is then validated through the comparison of results from different measurement methods. The proposed methods clearly reveal the punch-through phenomenon of measured SiC-SBD, and enable the extraction of pertinent parameters for device modeling.

Keywords: C–V characteristics, high voltage, SiC, punch-through, parameter extraction

Classification: Electron devices

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1 Introduction

Comparing to conventional Si semiconductor, Silicon Carbide (SiC) semiconductor has superior electrical and thermal performance. High voltage power switching devices are the target applications of SiC to utilize the advantages of the material [1, 2, 3]. The electrical capacitance between the terminals of switching device has a tremendous obstruction on the switching performance, since it must rapidly be charged/discharged at the instance of switching operation. The high electric field breakdown of SiC enables the voltage blocking layer of the device to be thinner and higher doped. This results in larger capacitance, which widely varies to the reverse bias voltage change. It implies the importance of careful evaluation and precise modeling for analysis and design of switching circuits. There are commercial instruments to measure the capacitance of a device by applying a dc bias voltage. However, their voltage ranges are insufficient for the capacitance–voltage (C–V) characteristics measurement of high voltage SiC devices. Therefore, the capacitance of the devices biased at high voltage conditions is not available for device modeling [4, 5, 6]. Consequently, this paper develops the capacitance measurement instrumentation, suitable for the measurement of C–V characteristics of SiC Schottky Barrier Diodes (SBD) at high reverse bias voltages. The authors then evaluate the punch-through phenomenon of SiC-SBDs and extract the parameters of device model from the measured results. This paper is one of the series studies for characterization and modeling of SiC power devices [7, 8].

2 Developed Measurement Instruments

A variety of instruments are available to measure the electrical capacitance of devices; such as C–V meter, LCR meter, and impedance analyzer. Several instruments can apply dc bias voltages on the device with their internal circuitry, whose typical ratings being 30–40 V. Another way to apply dc bias voltage on a device is to incorporate an external dc bias fixture in the measurement set up, and the currently available fixtures can apply a bias

voltage up to 200 V. However, the voltage (up to 200 V) is grossly insufficient for the measurement of C–V characteristics of high voltage devices over their rated voltage; e.g., 600 V for the Infineon SBD06S60 SiC-SBD. The precise C–V characterization across the rated voltage of SiC-SBD is indispensable for proper modeling of the device. The authors therefore develop two new methods for the measurement of SiC-SBD capacitance between the anode and the cathode terminals, through which the dc reverse bias voltage can be applied up to the rated blocking voltage exceeding 600 V.

2.1 Measurement Method 1

Figure 1 (a) shows the circuit diagram of developed measurement instrumentation for C–V characteristics to cope with high voltage dc bias condition. The power supply (Agilent N5772A) applies the dc bias voltage on a DUT up to 600 V. The ac measurement signal (100 kHz sinusoidal wave) is generated from a signal generator (Tektronix AFG310), amplified (using NF Corp. HSA4101) and then coupled to the main circuit with a high frequency transformer, which isolates the ac signal generator from the high voltage dc bias. The applied ac signal has an amplitude of 1 V and is superimposed on the dc bias voltage. The measuring frequency is tuned at 100 kHz to follow the highest measurement frequency of the LCR meter in method 2. A digital storage oscilloscope (DSO: Tektronix TPS2024) is employed for the measurement of signals. The current flowing through DUT is obtained as the voltage drop across 10 k Ω non-inductive resistance, which is measured by CH1 of DSO. Under high dc bias voltage, it is difficult to keep high S/N ratio for the superimposed ac signal. Then, a 0.1 μ F film capacitor is placed in parallel to the power supply for bypassing the 100 kHz ac measurement signal. Hence, the applied ac signal voltage on the DUT becomes as the summation of the transformer output voltage, which is measured by CH2 of DSO, and the voltage across the current sensing resistor. The voltage and current wave forms are recorded in the time domain and converted into the frequency values by

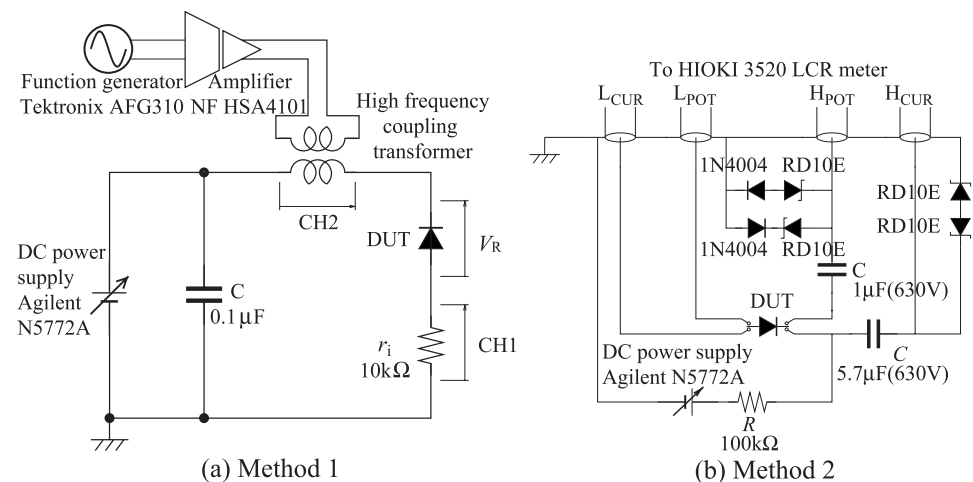


Fig. 1. Configurations of the developed C–V characteristics measurement instrumentation.

digital Fourier transform, hence the 100 kHz components are extracted. The capacitance and the conductance of DUT are then extracted in the form of complex impedance at the measuring frequency. The parasitic components in the measurement circuit are compensated through open, short and load compensations prior to every measurement.

2.2 Measurement Method 2

Method 2 developed in this paper makes use of a LCR meter (HIOKI 3520) as the base measurement apparatus along with a following specially fabricated external dc bias fixture. The basic configuration of the fixture is given in Fig. 1 (b), which refers to the configuration of Agilent 16065 A. The original configuration can apply dc bias voltages up to 200 V. The values of components and their arrangements in fixture are then re-designed to cope with the higher dc bias voltage. The open and short circuit compensation must be conducted prior to the measurements as same as method 1.

3 Results of C–V characteristics measurement

Figure 2 shows the measured C–V characteristics of the SiC-SBD, compared with the values in datasheet. The curve A depicts the result by the internal dc bias circuit of LCR meter with a rated dc bias voltage of 30 V. The curve B also depicts the result by employing Agilent 16065 A external dc bias fixture with a 200 V rated voltage. The curves C and D respectively correspond to the results from Methods 1 and 2 proposed in the previous section with a rated voltage range up to 600 V. The curve E gives the value in datasheet. The reverse dc bias voltage for the SiC-SBD was swept from 1 V to each rated voltage. The amplitude of the superimposed ac measurement signal was set at 1 V and the frequency at 100 kHz.

All results coincide with the datasheet in the range of bias voltage $2 \leq V_R \leq 30$ V, and the available 3 results of curves B–D do with the datasheet in the bias voltage range of $30 < V_R \leq 200$ V. These results clearly show the availability of the proposed methods in the range of bias voltages $2 \leq V_R \leq 200$ V. Then the corresponding 2 results, curves C and D are expected to

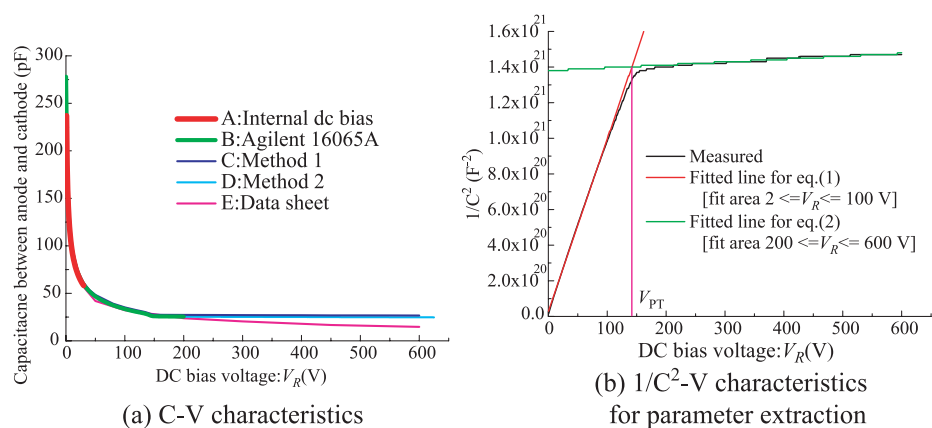


Fig. 2. Measured C–V characteristics of the SiC-SBD.

have the validity in the bias voltage range of $200 \leq V_R \leq 600$ V. There is a difference in the measured results at the dc bias voltage of $V_R = 1$ V. The difference is attributed to the magnitude of the applied ac signal, which is relatively large to the imposed reverse dc bias voltage added to the barrier potential of the SiC-SBD. Therefore the applied ac signal cannot be neglected at the low dc bias voltage. However, this does not in any way affect the results for the high reverse bias voltage range focused in this paper. In addition, there is a difference between the measured results of curves C–D and the datasheet values of curve E in the high reverse dc bias voltage region. The capacitance in datasheet smoothly changes to bias voltage, but the measured results of curves B–D have non-smooth change around $V_R = 150$ V. The difference can be estimated as the punch-through phenomenon occurring at high reverse bias voltage condition. The difference is difficult to evaluate with curve B of conventional method, but the proposed methods enables clearly to show the difference.

Figure 2(b) shows the $1/C^2$ – V characteristics evaluated from the measured C– V characteristics in order to extract the device parameters. The measured SiC-SBD device has a punch-through structure, which consists of a lightly doped epitaxial layer and a heavily doped substrate. It satisfies requirements for high voltage blocking and low forward voltage drop. The punch-through phenomenon affects the C– V characteristics of the device. The relation between the junction capacitance C and reverse bias voltage V_R can be described as Eq. (1), when the doping is uniform in the epitaxial layer and the voltage is insufficient for punch-through [9].

$$\frac{1}{C^2} = \frac{2}{S^2 \epsilon \epsilon_0 N_D} (V_R - V_b). \quad (1)$$

where S denotes the active area of device (1.191 mm^2 for the measured device), ϵ the dielectric constant of SiC semiconductor material ($9.7 \times 8.85 \times 10^{-14}$), e the electronic charge (1.602×10^{-19}), N_D the doping of epitaxial layer, and V_b the built-in potential.

The relation given in Eq. (2) can be easily derived as an expansion of Eq. (1). It supersedes Eq. (1), when the depletion layer punches through the epitaxial layer. Punch-through occurs when the depletion region in the SiC-SBD reaches to the edge of epi layer. In the condition, the C– V relationship can be expressed as:

$$\frac{1}{C^2} = \frac{2}{S^2 \epsilon \epsilon_0 N_{\text{SUB}}} (V_R - V_b) + \left(1 - \frac{N_D}{N_{\text{SUB}}}\right) \frac{W_D^2}{S^2 \epsilon^2}. \quad (2)$$

where N_{SUB} depicts the doping of substrate region, and W_D the thickness of epitaxial layer.

The results given in Fig. 2(b) obviously shows the punch-through phenomenon in the SiC-SBD, which occurs around $V_R = 150$ V. Although the gradient of the characteristic curve becomes low after the occurrence of punch-through, it is still possible to estimate the gradient with some extended measurements. Based on the results, the parameters in Eqs. (1) and

Table I. Extracted parameters of the SiC-SBD (SDT06S60).

Epitaxial layer thickness: W_D	$3.83 \mu\text{m}$
Doping of the epitaxial layer: N_D	$1.06 \times 10^{16} \text{ cm}^{-3}$
Doping of the substrate region: N_{SUB}	$6.36 \times 10^{17} \text{ cm}^{-3}$
Capacitance at punch-through: C_{PT}	26.7 pF
Punch-through voltage: V_{PT}	142 V
Built-in potential : V_b (fit area $2 \text{ V} \leq V_R \leq 10 \text{ V}$)	1.13 V

(2) can be extracted as shown in Table I. They are numerically estimated by applying the least mean square method to measured values.

4 Conclusion

The authors developed C–V characteristics measurement instrumentations to characterize the SiC-SBD across entire reverse blocking voltage range. The developed instrumentations have an ability to measure capacitance with imposing reverse dc bias voltage up to 600 V. The validity of the measurements was confirmed from the coinciding results from plural measurement methods. The measured C–V characteristics of the SiC-SBD showed the abrupt change of the capacitance at a voltage bias around 150 V. It indicates that the extended depleted region punches through the epitaxial layer according to the increased reverse bias voltage. The developed instrumentation could measure the expansion of the depletion region into the substrate of the device after the occurrence of the punch-through. This enabled the extraction of doped impurity density in both the epitaxial layer and the substrate region, and the thickness of the epitaxial layer from the punch-through voltage. The extracted parameters are crucial in modeling the SiC-SBD. Moreover, the proposed methods can easily be extended to higher dc bias voltage, which enables the measurement of the C–V characteristics of devices rated for higher reverse voltage blocking, such as PiN diodes.

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