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5 V input level shifter circuit for IGZO thin-film transistors

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Abstract: A 5 V input level shifter circuit based on depletion-mode In-Ga-Zn-O thin-film transistors (TFT) worked up to 100 kHz. By employing metal-insulator-semiconductor (MIS) active capacitor, we enhanced the bootstrapping effect and reduced the rise time of the output signal. SPICE simulation results showed that the proposed level shifter worked for wide threshold voltage range from −2 V to +1 V and the fabricated circuit exhibited the propagation delay t_{plh} and t_{phl} of 0.6 µsec and 0.3 µsec respectively.

Keywords: 5 V input, level shifter, depletion-mode, oxide TFT, active capacitor

Classification: Electron devices, circuits, and systems

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1 Introduction

Recently thin-film transistors (TFT) employing metal-oxide semiconductors such as In-Ga-Zn-O (IGZO) are expanding their application because they exhibit low process cost compared with the low-temperature polycrystalline silicon (LTPS) TFT and superior stability and higher on-current than the amorphous silicon (a-Si) TFT. They are suitable for high-resolution active-matrix liquid-crystal display (AMLCD) and large-area active-matrix organic light-emitting diode (AMOLED) display [1, 2].

However the oxide TFT operates only as n-channel field-effect transistor and it is difficult to control the threshold voltage (V_T) as intended. They often exhibits depletion-mode characteristics due to narrow process window and by external influences such as illumination and bias stress [3, 4, 5]. As a result, a considerable amount of current may flow at zero gate-to-source bias (V_{GS}). Due to the possible negative threshold voltage (V_T) of the oxide TFTs, it is not desirable to utilize conventional circuit scheme when we integrate the driving circuitry on a display panel. Accordingly several new circuit structures have been devised based on the depletion characteristics of the metal-oxide TFTs [6, 7, 8, 9]. In this letter, we report a new level shifter circuit that is compatible with the 5 V TTL(transistor-transistor logic)-level input and depletion-mode oxide TFTs.

Fig. 1 shows the circuit structure and the timing diagram of the level shifter. It generates a 20 V digital signal from two 5 V input signals, i.e. V_{IN} and V_{INB}. So it can be used in generating the control signals, e.g. start and clocks of a gate driver in the active-matrix display from the 5 V TTL-level signals of a driver IC. This circuit is composed only of n-channel oxide TFTs, so it is difficult to pull-up the output voltage up to V_{DD} (20 V). Therefore

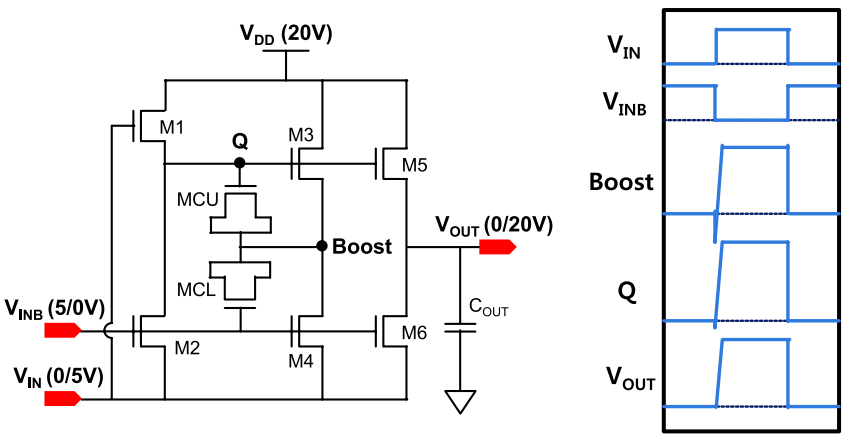

Fig. 1. Circuit structure and timing diagram of the level shifter.

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bootstrapping effect is used to turn on the pull-up TFT M3 and M5 even when the output voltage reaches V_{DD} by pushing up the Q node above V_{DD}.

The Q node voltage may fall while V_{IN} keeps 5 V due to large zero-bias current of M2 if M2 is turned off with zero V_{GS}. However our circuit applies negative V_{GS}, i.e. −5 V to M2 when V_{IN} is 5 V and V_{INB} is 0 V, which suppresses the leakage current through M2 and keeps the Q node voltage above V_{DD}. The metal-insulator-semiconductor (MIS) active capacitors MCU and MCL enhance the pull-up speed by varying the capacitance depending on the situation during the transient period.

2 Operation of level shifter

Fig. 2 shows the transient response of each node voltage in the level shifter circuit when V_T of the TFTs is 0 V. At T1, V_{IN} rises from 0 V to 5 V while V_{INB} falls from 5 V to 0 V. At this moment MCL has large capacitance because it has been turned on by the previous bias condition, i.e. $V_{GS} = 5$ V. Therefore the Boost node is pulled down by strong capacitive coupling with V_{INB}. However the capacitive coupling between the Q node and the Boost node is minimized because MCU has been almost turned off by $V_{GS} = 0$ V. This phenomenon is graphically shown in Fig. 3(a) and is verified in the SPICE simulation results of Fig. 2. As a result, V_{GS} of M3 is higher than 0 V and M3 is slightly turned on at T1.

At the beginning of T2 period, the Q node voltage rises faster than the B node because M1 is more strongly turned on by $V_{IN} = 5$ V than M3 as shown in Fig. 3(b) and Fig. 2. This effect further increases the VGS of M3. Soon the Q node voltage approaches 5 V and the current through M1 decreases to

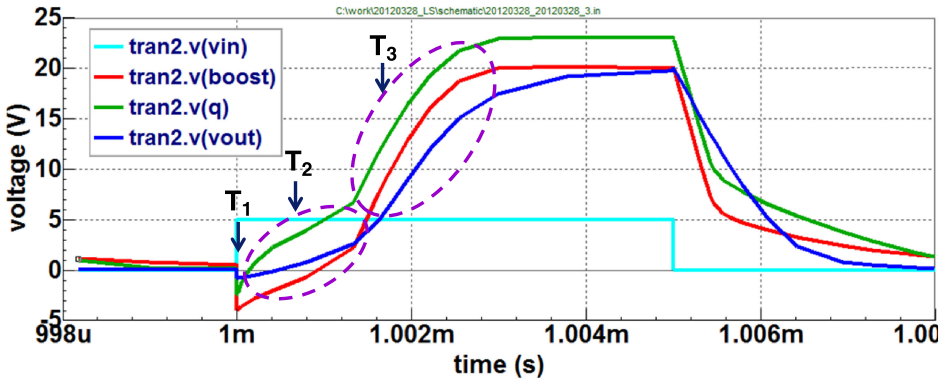

Fig. 2. Transient response of each node voltage in the level shifter

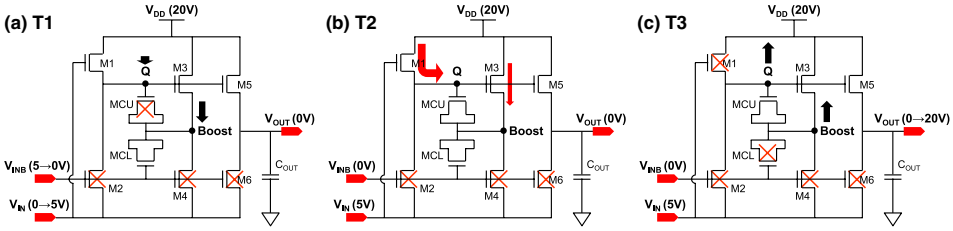

Fig. 3. Operation of each TFT during pull-up process.

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below the current through M1. At this moment M3 is considerably turned on ($V_{GS} \sim 5\,V$) and the current through M3 raises the voltage of the Boost node. Accordingly MCU is also turned on and has large capacitance. Therefore the Q node is pushed up effectively by capacitive coupling with the Boost node and the voltage rising speed of the Q and the Boost nodes become similar as shown in Fig. 2. However the voltage rising speed by the bootstrapping effect is not so high because the large capacitance of MCL restrict the voltage rising of the Boost node.

At the end of T2 period, the Boost node voltage exceeds V_{INB}, 0 V and so MCL is turned off. Therefore the capacitance of MCL decreases substantially and the voltage rising speed of the Boost node increases noticeably as shown in Fig. 2. During T3 period, the Q node and the Boost node voltages rise fast by the bootstrapping effect with large MCU and small MCL. It should be noted that the bootstrapping speed is enhanced by the capacitance variation of the two active capacitors, MCU and MCL.

Once the Q node is boosted up, it is maintained stably even though the TFTs exhibit depletion-mode characteristics because the two switch TFTs, M1 and M2 are turned off with negative V_{GS}. When V_{IN} falls to 0 V and V_{INB} rises to 5 V, the pull-down TFTs, M2, M4, and M6 are turned on and the Q node and the Boost nodes are pulled down to 0 V.

3 Results

We used SmartSpice in simulating the operation of the level shifter. Fig. 4 shows the simulation results the level shifter for various TFT V_T values. For each V_T value, it is assumed that all the TFTs in the circuit have same V_T. Input pulse duration is 5 µsec. This corresponds to 100 kHz operation when 50% duty is assumed. The circuit works even though V_T is −2 V. As V_T falls below −2 V, the output low level, though not shown here, rises gradually. Propagation delay and rise/fall time increase as V_T increases.

We fabricated the designed level shifter using the IGZO TFTs as shown in Fig. 5. Fig. 6 shows the measured input and output waveforms of the level shifter working at 100 kHz input signal frequency. In the fabricated circuit, V_T of the TFTs was not so uniform. For Fig. 6(a), the sample TFTs around the

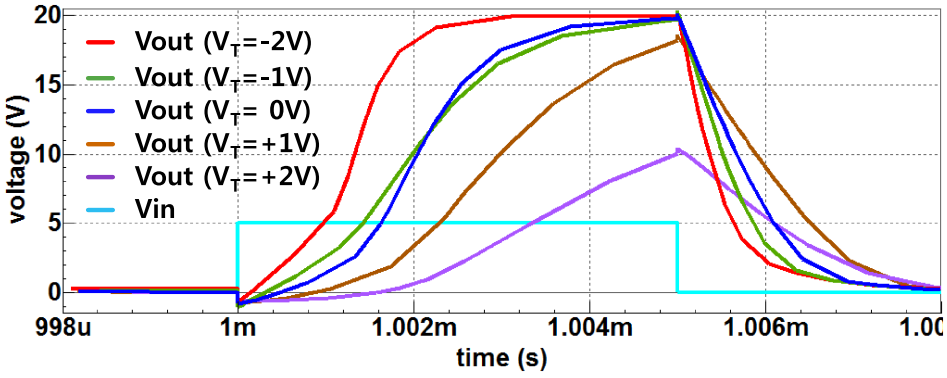

Fig. 4. SPICE simulation results of the level shifter for various TFT V_Ts. Input pulse duration is 5 µsec.

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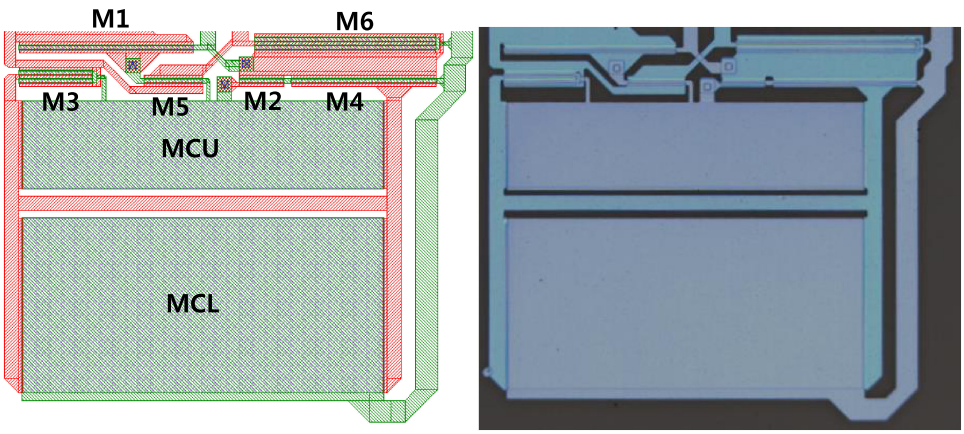

Fig. 5. Layout and photograph images of the level shifter.

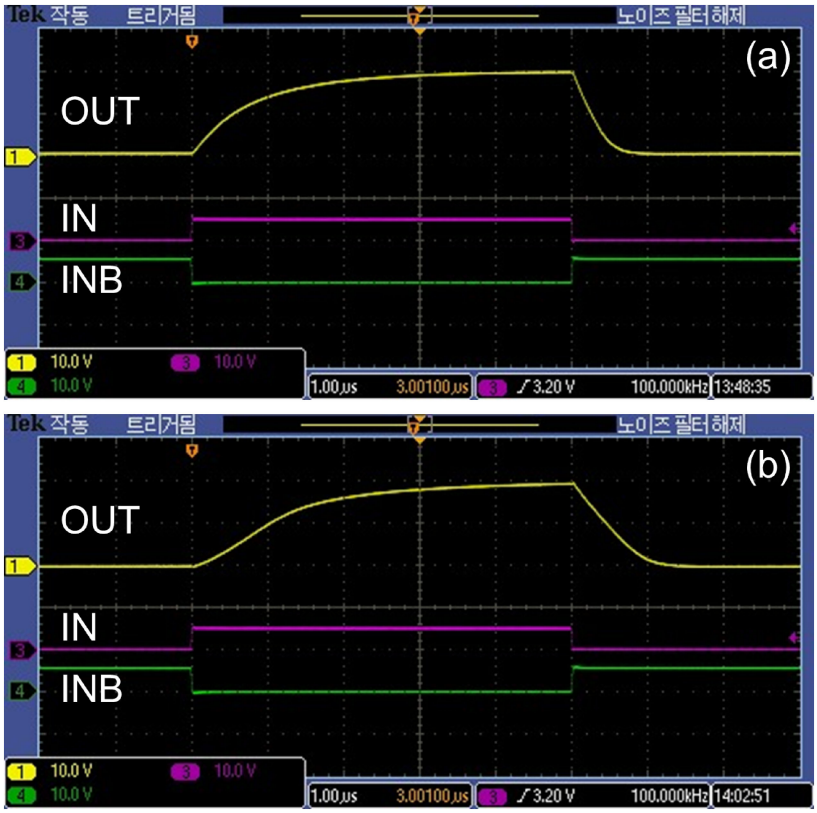

Fig. 6. Measured results of the fabricated level shifter with IGZO TFT process. (a) $V_T \sim -2$ V. (b) $V_T \sim -1$ V. Input pulse duration is 5 µsec.

circuit exhibited V_T of −2 V or so, while for Fig. 6(b), V_T was around −1 V. Therefore the propagation delay t_{plh} and t_{phl} are as small as 0.6 µsec and 0.3 µsec respectively in Fig. 6(a), while they are as large as 1.1 µsec and 0.5 µsec in Fig. 6(b).

4 Conclusion

We have developed a 5 V input level shifter circuit suitable for the n-channel metal-oxide TFT characteristics. This circuit generates a 20 V output signal

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even though V_T of the TFTs varies from −2 V to +1 V. The fabricated IGZO level shifter worked successfully at 100 kHz input signal frequency with the propagation delay less than 1 µsec. The high pull-up speed despite the disadvantage of n-channel transistor circuit, is owing to the enhanced boot-strapping effect of the active MIS capacitors.

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