

A thin film thermoelectric cooler for Chip-on-Board assembly

Shiho Kim^{a)}, Hyunju Lee, Namjae Kim, and Jungho Yoo

Dept. of Electrical Engineering, Chungbuk National University,
Gaeshin-dong, Cheongju city, Chungbuk, 361–763, Korea

a) shiho@chungbuk.ac.kr

Abstract: We have proposed and demonstrated an embedded thin film thermoelectric cooler attached between die chip and metal plate for Chip-on-Board (COB) direct assembly. The proposed structure of COB cooler was modeled by electrical equivalent circuit for SPICE simulation including operational heat generation of chip and PWM control of input power supply. The optimum input power of the TEC to achieve maximum temperature difference between chip and heat sink was simulated by using the proposed equivalent circuit. The measured and simulated results offer the possibility of thin film active cooling for COB direct assembly.

Keywords: thermoelectric cooler, Chip-on-Board cooling, PWM Driver of TEC

Classification: Electron devices, circuits, and systems

References

- [1] Overview of Chip-on Board [Online] www.SiliconFarEast.com
- [2] I. Chowdhury, R. Prasher, K. Lofgreen, G. Chrysler, S. Narasimhan, R. Mahajan, D. Koester, R. Alley, and R. Venkatamanian, “On-chip cooling by superlattice based thin film thermoelectrics,” *Nature Nanotechnology*, vol. 4, pp. 235–238, 2008.
- [3] H. Lee, S. Park, S. Cho, H. Kim, and S. Kim, “A Thin Film Thermoelectric Cooler for Chip-on-Board direct Assembly,” *IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS) 2009*, #47, 3 Dec. 2009.
- [4] Datasheet of Optocooler UPF-40, Nextremethermal solution Inc, 2008.
- [5] S. Lineykin and S. Yaakov, “Analysis of thermoelectric Coolers by a SPICE-compatible equivalent-circuit model,” *IEEE Power Electron. Lett.*, vol. 3, no. 2, pp. 63–66, 2005.
- [6] D. Mitrani, A. Tome, J. Salazar, A. Turo, M. Garcia, and J. Charvez, “Methodology for Extracting thermoelectric module parameters,” *IEEE Trans. Instrum. Meas.*, vol. 54, no. 4, pp. 1548–1552, 2005.
- [7] G. Snyder, J. Fleurial, T. Caillat, R. Yang, and G. Chen, “Supercooling of Peltier cooler using a current pulse,” *J. Appl. Phys.*, vol. 92, no. 3, pp. 1564–1569, 2002.

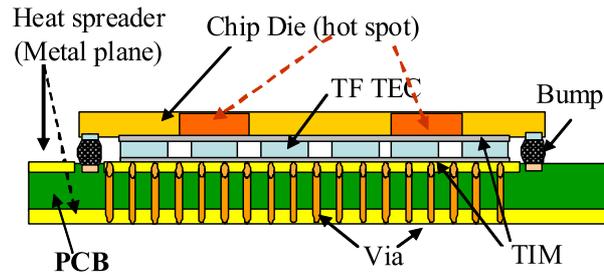
1 Introduction

Chip-on-Board (COB) is a direct chip assembly technology wherein the chip die is directly mounted on and electrically interconnected to its final circuit board, instead of undergoing traditional packaging process as an individual IC [1]. The COB assembly technology can simplify the over-all process of designing and manufacturing the final product, as well as improves its performance as a result of shorter interconnection paths thanks to the elimination of conventional device packaging. The COB process consists of major steps of die attach, and encapsulation of the die. Encapsulation is generally done by dispensing a liquid organic based encapsulating material over the die-on-board. One of the concerns of the COB application is significantly lower thermal conductivity of organic material of PCB, and limited heat spreading path because die chip is attached on board and encapsulated by the protective layer. There is a significant demand for site-specific and on-demand cooling in Chip-on-Board systems. However, integrating heat sink in COB is very difficult, especially for the case of encapsulated COB due to encapsulating material over the active surface of the chip. The thermoelectric (TE) device is a solid-state active heat pump which transfers heat from one side of the device to the other side against the temperature gradient. The thermoelectric cooler (TEC) uses the Peltier effects to create a heat flux between the junction of two different types of semiconductor materials [2, 3].

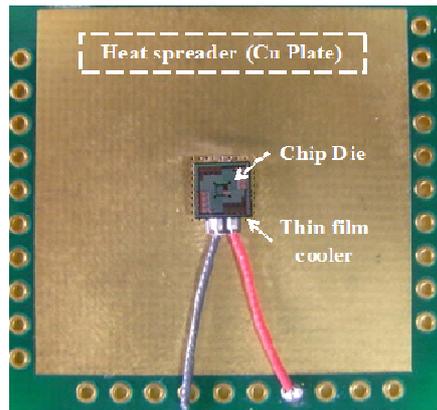
This paper will elaborate on the issues and solutions associated with thermal management of Chip-on-Board assembly to provide a suitable solution to thermally limited applications of COB technology. Here, we show the design and integration of thin film thermoelectric coolers into Chip-on-Board electronic system. This is the first demonstration of viable thin film thermoelectric cooler for COB assembly.

2 Proposed structure of COB Cooler

Fig. 1 illustrates the proposed structure of the thin film thermoelectric cooler for COB assembly. Thin film thermoelectric cooler is attached between Chip die and the metal plate of PCB. The basic idea of proposed architecture is using the metal plate on the PCB as a heat spreader with thermoelectric active heat pump. Metal plates for GND and/or VDD plane can be used for air cooled heat spreader to reject heat to ambient. Thermal rejecting path between chip and metal plate is formed through the thermoelectric cooler attached to the underside of the integrated heat spreader. The thermal interface material (TIM) was placed between the cooler and interface of the silicon chip and metal plates to establish good thermal contact. We can place via between top and bottom metal layers of PCB to enhance thermal spreading capability. The thermal via is used to transfer heat from top metal to bottom plate. The proposed thin film thermoelectric cooler can be applied both for wire bonding and flip-chip COB's. Since flip-chip COB has their chips facing downward on the board, it is necessary to fill the gap under the flip-chip to protect its active surface and bumps from thermo-mechanical



(a)



(b)

Fig. 1. (a) Schematic cross-section of proposed TFTEC for flip-chip bonding COB structure. (b) Fabricated COB cooler using commercial thin film thermoelectric module [4] and Copper metal plate as a heat spreader. Area of metal heat spreader is $35\text{ mm} \times 35\text{ mm}$, and die size is $5\text{ mm} \times 5\text{ mm}$.

damage [1]. Embedded thin film thermoelectric cooler (TFTEC) under the flip-chip provides a heat pump for rapid die cooling, and it also provides the under-fill layer protecting the chips from mechanical stress. Recently, thin film thermoelectric coolers are commercially available, the thickness of nanostructured thin film thermoelectric materials of Bi_2Te_3 is less than $30\text{ }\mu\text{m}$ [4].

The COB fabrication process with the thin film thermoelectric cooler is similar to conventional process, except for additional step for mounting TFTEC on the heat spreader. Fig. 1 (b) shows fabricated test vehicle of the thin film thermo electric cooler for the COB assembly. The heat spreader in Fig. 1 (b) is a Copper metal plate for GND plane of the COB assembly. The cooler is powered through the leads on either side. The thin film cooler is attached on the top metal layer, but heat generated by COB will also be spreading on the bottom metal layer through thermal conducting via. To measure the temperature of the chip and heat sink, encapsulation processing step was skipped in the fabricated test samples. The active area of the commercial thin film TEC is $1.6\text{ mm} \times 3.2\text{ mm}$ [4], whereas area of the chip die is 25 mm^2 .

3 Modeling, simulation, experimental results and discussions

Cooling performance of the fabricated TFTEC was measured by Infra red thermal imager. Fig. 2 (a) shows Infra red image of test vehicle, and Fig. 2 (b) is temperature gradient profile across the straight line marked on the metal plate and the chip. The ambient temperature during experiment was 28.5°C. Infrared images of the test chip are illustrating cooling effects of the thermoelectric cooler.

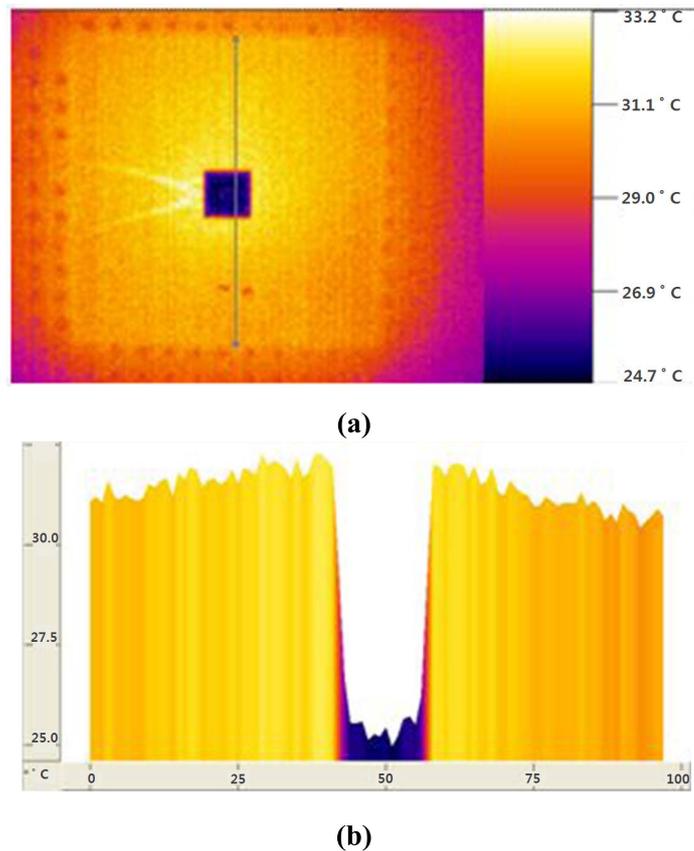


Fig. 2. (a) IR image from fabricated COB in a case of supplying $I = 0.13\text{ A}$ at $V = 0.1\text{ V}$ (b) Temperature profile along the strait line.

Electro-thermal behavior of the proposed thin film thermoelectric COB cooler can be modeled by SPICE equivalent circuit of thermoelectric devices, as shown in Fig. 3(a). An accurate but simple SPICE model is very beneficial for precise temperature control of TEC. The SPICE model consists of the electrical part reflecting Seebeck effects where thermally generated voltage (V_α) is proportional to Seebeck coefficient (α_m) and temperature difference between hot and cold side of TEC, and the thermal part circuit considering electrical analogy of thermal behavior [5]. Model parameters of the equivalent circuit were extracted using the experimental method to determine thermoelectric module parameters [6]. In the thermal model, node voltage represents absolute temperature in Kelvin and current source means heat in watt [5]. In the equivalent circuit, R_m is internal electrical resistance,

and current source $P = I^2 R_m + \alpha_m (T_h - T_C) I$ and $P_x = -0.5 I^2 R_m + \alpha_m T_C I$ represent electric power and cooling power of TEC, respectively. R_{sink} , R_{ch} , R_{sil} are thermal resistances (unit of Kelvin/watt) of heat sink, of chip die, and of TIM, respectively.

The electrical capacitors are used to model the following thermal capacitances (unit of Joule/Watt); C_{sink} for heat sink, C_{ch} for chip die, C_C for cold side of TEM, and C_h for hot side of TEM, respectively. Voltage source V_{tem} is used for electrical analog of ambient temperature (i.e. for the simulation, $V_{\text{tem}} = 28.5 + 273 = 301.5 \text{ V}$).

Fig. 3 (b) shows measured and simulated temperatures of chip die and heat spreader as a function of supplying current. There is a good agreement between measured and simulated temperatures. The minimum chip temperature is 21.1°C and hot temperature of the sink is 30.5°C when 216 mW of power applied to the TE cooler. After applying 0.54 A to the TEC (216 mW of input power), the chip temperature began to rise. Measured and simulated maximum active cooling performance is about 7.5°C for the fabricated structure.

The pulse width modulation (PWM) technique can be used to control the optimum supply to the TEC [7]. Fig. 3 (c) shows modified SPICE equivalent circuit model of the proposed TEC including a heating element and PWM control. The current source in the thermal part of the model, I_{chtemp} , is electrical modeling for heat generation by the chip during operation. PWM control switch is added to the electrical part model, where power to the TEC is adjusted by varying the duty ratio of the square wave. Fig. 3 (d) shows a simulated temperature profile as a function of duty ratio, under a condition that chip temperature without cooling is set to 100°C by using I_{chtemp} , when supply voltage is 0.6 V and 1.2 V, respectively. The simulated maximum active cooling temperature is about 7.5°C , which is close to the measured value in the fabricated structure without heat generation. The optimum duty ratio for minimum temperature of the chip is about 0.4 for 1.2 V and about 0.7 for 0.6 V, respectively. Simulated and measured data were revealed that the maximum cooling capacity is almost independent on chip temperature.

The cooling performance of the fabricated thin film thermoelectric cooler for the COB assembly might be not sufficient for the whole chip cooling. We investigated the physical reason for limitation of cooling capacity. When power is supplied to the TEC, the heat of cold side is pumping to the hot side, and the temperature of heat spreader is increasing very rapidly. The cooling power due to Peltier effects of TEC is proportional to supplying current ($\sim \alpha_m T_C I$), but the generated heat in the TEC caused by joule heating effects is proportional to square of supplying current ($\sim I^2 R_m$). If the heat pumped from the chip is not rejected to air insufficiently through the heat sink, the heat in the hot side is back drift to the cold side of the cooler.

The main reason for insufficient heat pumping capability of TFTEC is smaller area and poor Seebeck coefficient (α_m) of commercial of TFTEC, besides, limited heat conductance of the thin Copper metal plate of PCB. The

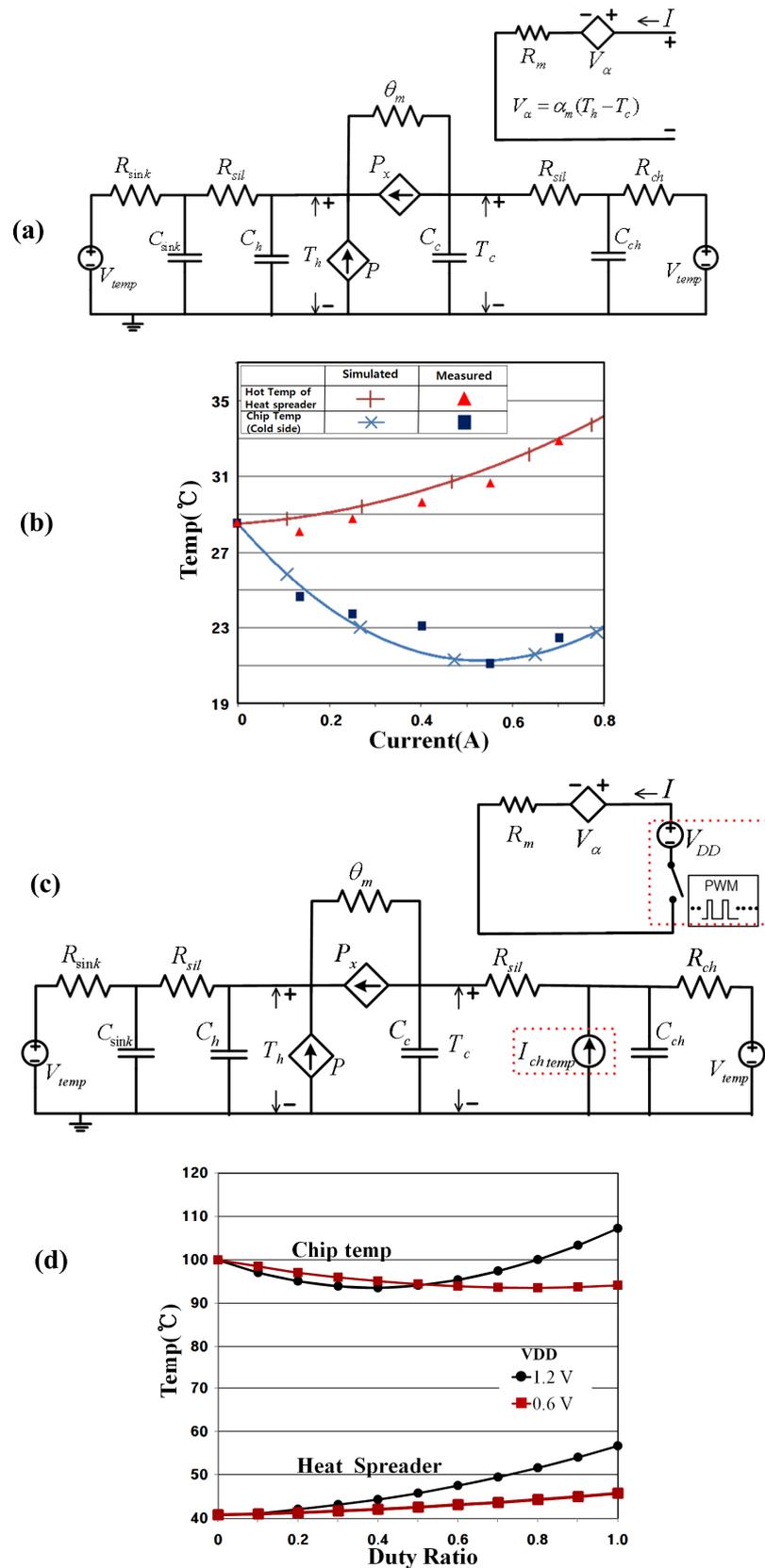


Fig. 3. (a) SPICE equivalent circuit model of proposed TF TEC, (b) Measured and simulated temperature of chip die and heat spreader versus input current of TEC, (c) SPICE equivalent circuit model of proposed thin film Thermoelectric COB cooler including a heating element and a PWM control switch, (d) Simulated temperature of chip and heat spreader as a function of duty ratio when supply voltage is 0.6 V and 1.2 V, respectively.

area of the TFTEC of the fabricated test vehicle was only about 5.12 mm^2 , which is only about one fifth of the die chip area (25 mm^2).

For enhancing the cooling capability, we need to co-design heat pumping capability with system level cooling structure. The TFTEC has to be large enough for sufficient cooling capability in whole chip cooling application. The heat spreader using Copper metal plate should be thermally connected to the Body or the Chassis of the system to reduce thermal resistance of the heat rejecting path.

Measured performances of the proposed thin film cooler is not satisfactory in this moment, however, this demonstration offers the possibility of thin film active cooling for the COB direct assembly. This technology can be extended to hot spot cooling for COB assembly that can be selectively switched on and off by monitoring local hot temperature of a chip

4 Conclusions

A thin film thermoelectric cooler for COB direct assembly was proposed and the electro-thermal behavior of proposed COB cooler structure was model by electrical equivalent circuit for SPICE simulation. The embedded cooler attached between the die chip and metal plate can offer the possibility of thin film active cooling for the COB direct assembly. We proposed a driving method of TEC by using pulse width modulation technique. The optimum power to achieve minimum chip temperature of the TEC is simulated by using proposed SPICE. The measured and simulated results offer the possibility of thin film active cooling for the COB direct assembly.

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