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Work function modulation of PtSi by alloying with Yb

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Abstract: Work function modulation of PtSi by alloying with Yb to achieve ultra-low contact resistance for advanced CMOS was investigated. Pt_xYb_ySi was formed by depositing Pt(6-18 nm)/Yb(2-14 nm)/n-Si(100) stacked structure followed by 400-800°C/1-30 min silicidation in N_2 ambient. It was found that barrier height for electron (Φ_{Bn}) was decreased as the silicidation temperature and time increased, and Φ_{Bn} was reduced to 0.52 eV by depositing Pt(6 nm)/Yb(14 nm) followed by 800°C/30 min silicidation. It was found that Yb diffusion toword the silicide/Si interface was enhanced, compared to the sample formed by 500-600°C silicidation, which leads to further decrease of Φ_{Bn}. The estimated effective work function of PtSi decreased from 4.92 eV to 4.57 eV.

Keywords: PtSi, YbSi, barrier height, work function, sputtering

Classification: Electronic materials, semiconductor materials

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1 Introduction

In nanoscale complementary metal-oxide-semiconductor field effect transistors (CMOSFETs), contact resisitance acounts for the large portion of the series resistance, and results in degradation of transistor perfomance [1]. To obtain a high-driving current in MOSFET, it is effective to reduce the series resistance including contact resistivity of silicides at source/drain regions. In order to reduce the contact resistivity, low Schottky barrier height (SBH) contact material for each n- and p-type Si, such as 0.3 eV or lower is required [2]. Therefore, the SBH modulation of the contact material has been widely studied [3, 4, 5]. Mono-silicide, such as NiSi is expected to be a candidate for the contact material with shallow junction, however, its poor thermal stability and difficulty to form thin NiSi layer is reported [6, 7]. PtSi is a promissing contact material for PMOS source and drain, because of its excellent thermal stability, low Si consumption and low SBH for hole. However, the barrier height for electron (Φ_{Bn}) is 0.87 eV, which is relatively high compared to that of NiSi [3, 5]. PtSi alloying with low work function metal is a promissing process to reduce Φ_{Bn}, and we have reported that a 0.3 eV reduction of Φ_{Bn}, was achieved by PtSi alloying with Hf [8].

Ytterbium (Yb) is known to have a low work function of 2.7 eV, and it is reported that Yb silicide also have a low Φ_{Bn} of 0.27 eV [9]. Some researchers reported that Yb incorporation to NiSi reduced the Φ_{Bn} of NiSi effectively [10, 11]. In this paper, reducing the Φ_{Bn} of PtSi by alloying with Yb was investigated [8], and the silicidation mechanism was proposed for the first time.

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2 Experimental procedure

N-Si(100) substrate (10 Ωcm) were chemically cleaned and dipped in DHF followed by rinsing in ultra pure water. Then, SiO_2 (100 nm) was grown by wet thermal oxidation at 1000°C, followed by contact holes ($100 \times 100\,\mu m^2$) patterning. Pt(6-18 nm)/Yb(2-14 nm)/n-Si(100) stacked structures were in-situ deposited at room temperature (RT) by RF magnetron sputtering method. The total thickness of stacked layers was 20 nm. The Ar gas pressure in the chamber during deposition was 0.65 Pa (Ar flow rate: 4.0 sccm). In this study, Pt/Yb/n-Si(100) stacked structure was examined so that Pt acts as a capping layer to prevent Yb oxidation during ex-situ annealing. Silicidation was performed using the silicon wafer covering rappid thermal annealing (SWC-RTA) [12] at 400-800°C for 1-30 min in N_2 ambient. The unreacted metal on the SiO_2 was removed by diluted aqua regia ($HCl : HNO_3 : H_2O = 3 : 2 : 1$) at 40°C. Finally, Al was deposited on the back side of sample as electrical contact by evaporation process.

The sheet resistance of silicide layer was evaluated by a four point probe method. The silicide layer was also characterized by x-ray diffraction (XRD), x-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM). Φ_{Bn} was calculated from the J-V characteristics of fabricated Pt_xYb_ySi/n-Si(100)/Al Schottky diodes.

3 Result and discussion

Fig. 1 shows silicidation temperature and Yb thickness dependence of Φ_{Bn} and sheet resistance of the sample formed at 400-700°C silicidation after depositing Pt(6-18 nm)/Yb(2-14 nm)/n-Si stacked structure. As shown in Fig. 1 (a), reduction of Φ_{Bn} was observed as Yb thickness increased. In case of 6-10 nm-thick Yb, Φ_{Bn} once increased as the silicidation temperature increased to 600°C, and starts decreasing, when the silicidation temperature is higher than 600°C.

Low sheet resistance was obtained for the silicide with 6 nm-thick Yb or thinner, and the sheet resistance was approximately 20 Ω/sq, which is close to that of PtSi. However, when Yb thickness was increased to 10 nm, sheet resistance obviously increased, and low silicidation temperature seems insufficient for complete silicidation, which results in high sheet resistance.

Fig. 2 (a) shows silicidation temperature dependence of Φ_{Bn}. Φ_{Bn} reduction is observed by high temperature silicidation, which corresponds to the reverse current of the J-V characteristics of the Schottky diode, as shown in Fig. 2 (b). Furthermore, Φ_{Bn} decreased as silicidation time increases when the silicidation was carried out at 800°C as shown in Figs. 2 (c) and (d). For the case of 14 nm-thick Yb, Φ_{Bn} is reduced to 0.52 eV by 800°C/30 min silicidation. The rms roughness decreased to approximately 0.8 nm when silicidation was carried out at 800°C/30 min (Not shown). Interestingly, surface morphology was greatly improved by incorporating Yb, compared with that of PtSi [8].

To investigate the mechanism of Φ_{Bn} reduction, XPS depth profile of

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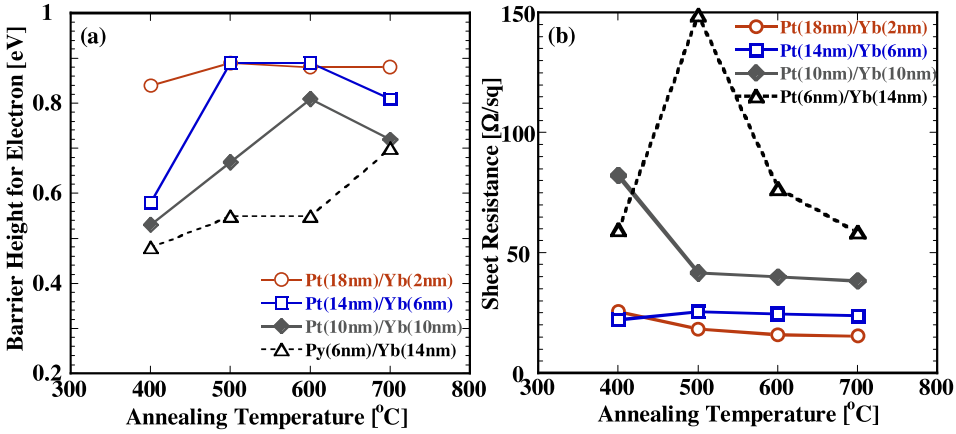

Fig. 1. Silicidation temperature and Yb thickness dependence of (a) Φ_{Bn} and (b) sheet resistance.

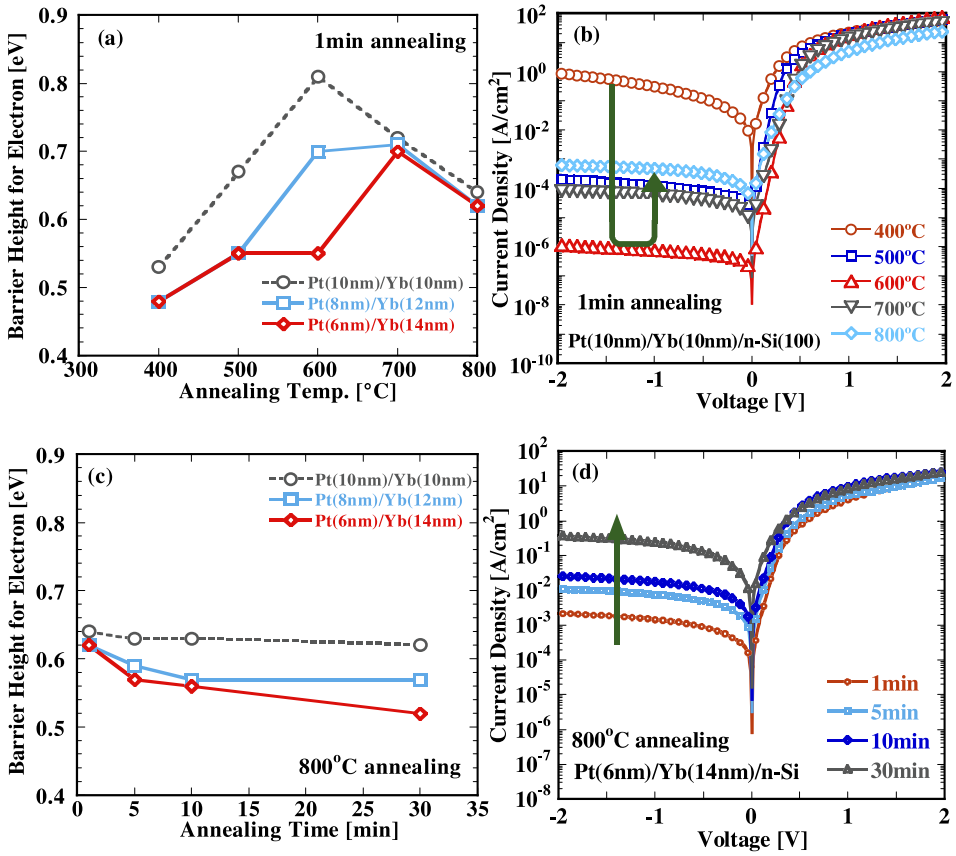

Fig. 2. Silicidation temperature dependence of (a) Φ_{Bn} and (b) J-V characteristics, and silicidation time dependence of (c) Φ_{Bn} and (d) J-V characteristics.

the silicide layers was studied, as shown in Figs. 3 (a) and (b). In case of 600°C/1 min silicidation, Yb segregation at the silicide surface was observed, and almost no Yb remained at the silicide/Si interface. On the other hand, depth profile of the silicide formed at 800°C/1 min shows existence of Yb at the silicide/Si interface, as shown in Fig. 3 (b). This result indicates that Φ_{Bn} reduction is due to the existence of Yb at the silicide/Si interface. Moreover,

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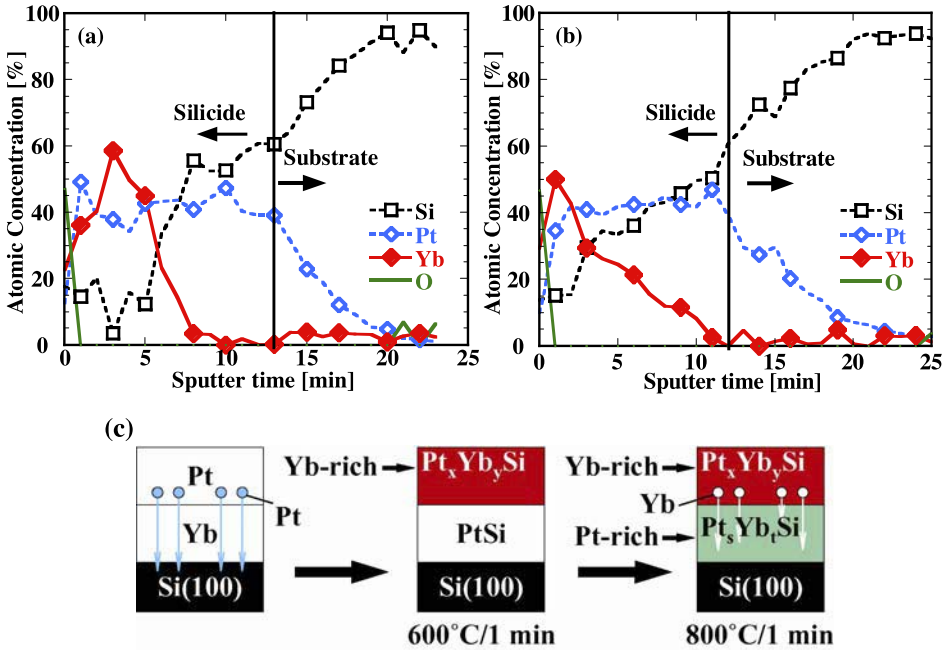

Fig. 3. XPS depth profiles of the silicide formed by (a) 600°C/1 min, (b) 800°C/1 min silidcidation. (c) Schematic model for silicidation for PtSi alloying with Yb.

this redistribution of Yb toword the silicide/Si interface was caused by large thermal energy during silicidation, which led to the reduction of Φ_{Bn}.

A schematic model for silicidation of Pt/Yb/n-Si(100) structure is shown in Fig. 3 (c). Diffusion species are Pt and Si in this ternary system. At the initial stage of the silicidation, Pt diffuses toword Si substrate, and PtSi layer are formed at the silicide/Si interface, which result in high Φ_{Bn}. When the thermal energy during the silicidaiton is high enough, Yb accumulated at the surface starts to diffuse toword the silicide/Si interface, which results in the reduction of Φ_{Bn}.

4 Conclusion

Formation of PtSi alloyed with Yb by annealing of Pt/Yb/n-Si(100) stacked structure was studied. Reduction of Φ_{Bn} was clearly observed, and the contribution of Yb distribution toword the silicide/Si interface was indicated. $\Phi_{Bn} = 0.52$ eV was obtained by 800°C/30 min silicidation after Pt(6 nm)/Yb(14 nm)/n-Si(100) deposition. From the result of Φ_{Bn} modulation, the effective work function of PtSi estimated to be decreased from 4.92 eV to 4.57 eV. Furthermore, it was found that surface morphology was greatly improved by incorporating Yb.

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