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A decoupled architecture for multi-format decoder

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Abstract: We propose a VLSI design of Multi-Format Decoder (MFD) to support multiple video codec standards such as MPEG-2, MPEG-4, H.264 and VC-1. A decoupled MFD architecture is introduced in order to easily add or remove the codecs. The decoupled architecture preserves the stability of the previously designed and verified codecs. It also reduces the gate count by sharing the large-size common resources. The design size is 2.4 M gates and the operating clock frequency is 225 MHz in the 65 nm process.

Keywords: codec, multi-format decoder, decoupled architecture

Classification: Integrated circuits

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1 Introduction

Recently, the demand for supporting various video codec standards is rapidly increasing in the consumer electronics market such as D-TV and mobile phones. H.264, VC-1 and MPEG-4 including DivX as well as MPEG-2 are used in many applications. Many hardware and software solutions have been developed to support these codecs. In the hardware solution, if individual codecs are designed separately, the whole design becomes too large. Various attempts have been introduced to reach better area-efficiency by merging these codecs [1, 2, 3]. They are called multi-format codecs or decoders (MFD).

If the required codecs are changed with the market change, the MFD needs to be modified. However, the design complexity increases as we try to merge the logic at the lower level. Then the design time and the chance of errors increase as well as the difficulty of the verification. All these lead to an unreliable design of MFD and increased cost. In this paper, we propose a decoupled MFD architecture to overcome these problems. It preserves the previously designed and verified parts while reducing the chip-size drastically. The proposed MFD supports up to Full-HD (1920x1088@60 fps) video decoding.

This paper is organized as follows. Section 2 introduces the previous work on the MFD design. Section 3 explains the proposed MFD architecture in detail. Section 4 shows the analysis of the design results. Finally, section 4 concludes the paper.

2 Previous Work

Chien's work [1] shows the VLSI design of Multi-Standard Multi-Channel Video Decoder. The target performance is 1080 p@30 fps, which is 50% of ours. The supported codecs and their profiles are MPEG-2/ MPEG-4 Simple and H.264 Baseline profiles. VC-1 is not supported. The design approach of [1] is to fuse everything together and minimize the area. Hase [2] shows the encoder and decoder of MPEG-4, H.264 and VC-1. It optimizes the area by sharing hardware resources between the codecs. It focuses on the low-power design. The target performance is D1 (720x480@30 fps), which is 8.3% of ours. The design approach is not a decoupled architecture. Liu [3] shows a low-power design approach for MPEG-2 and H.264. It is different from our design interest since we focus on the performance and size rather than power.

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3 Proposed MFD

The proposed MFD consists of the following major components: a RISC processor, on-chip memories, host I/F, MC (memory controller) and hardwired accelerator modules to perform the macroblock level decoding. The operating sequence is as follows. At first, MFD is initiated by the external host CPU. Once the RISC processor confirms it, then the elementary stream is read and stored in the external memory. Then, the RISC processor reads the syntax data and performs syntax parsing up to the slice level. The result is stored in the register file and the on-chip SRAM. The macroblock level parsing and decoding are done in a pipelined fashion by the hardwired accelerator modules such as entropy decoder, inverse Quantization/Transform (Q/T), prediction and loop filter. The final result is stored in the external memory.

The dominant common resources of MFD are the RISC processor, on-chip memories, host I/F and MC. They account for 60% of the whole MFD size and can be shared between codecs. The hardwired accelerator modules still contain relatively large and easy-to-share components such as large tables, filters and multipliers. We investigate this carefully and design our MFD with a decoupled architecture so as to achieve both flexibility and small size. The decoupled architecture is explained in detail in the following subsections.

3.1 Macroblock Syntax Decoder

In the macroblock level decoding, the macroblock level data is parsed from the stream, modified slightly, and then passed to inverse Q/T, prediction, and loop filter. The Macroblock Syntax Decoder (MSD) performs the macroblock level parsing. It creates the residual data and the motion vector. Figure 1 shows the architecture of MSD. Macroblock Syntax Parser (MSP) performs the syntax parsing and Motion Vector Decoder (MVD) creates the motion

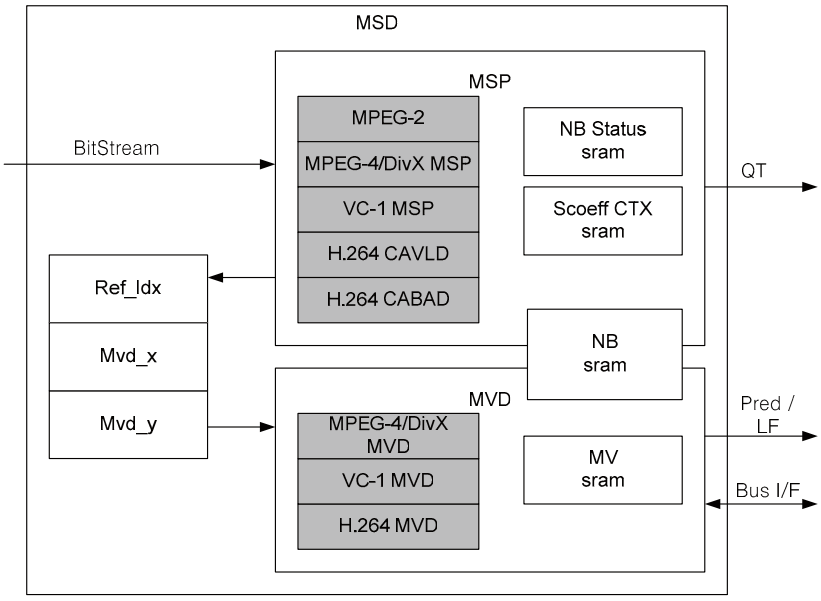

Fig. 1. Macroblock Syntax Decoder (MSD) Architecture

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vector.

The computation of MSD is very different among codecs as follows. For the syntax parsing, CABAD and exponential Golomb coding are used for H.264 while the variable length decoding is used for the rest. To compute the coefficients, run-level decoding is used. The motion vector computation for MPEG-2 is simple. However, it becomes more complicated for MPEG-4, H.264 and VC-1. For interlace computation, MPEG-4 has interlace frame only, but VC-1 has interlace frame and field, which are computed differently. H.264 has MBAFF mode to handle a pair of macroblocks together.

If we try to merge aforementioned logics at low level, the design becomes very complicated and the area reduction should be trivial. The computation of MSD requires many look-up tables, and they are around 50% of the whole MSD size. Therefore, we share the look-up tables by SRAMs and implement the logic part separately except for some large multipliers.

3.2 Inverse Q/T

Inverse Q/T performs DC/AC prediction, inverse zigzag scan, and inverse quantization/transform. The architecture is shown in Fig. 2. QT_Pred_Process block performs DC/AC prediction. The DC/AC predictions of MPEG-4 and VC-1 are very similar and merged as one. The DC prediction of MPEG-2 is very different from others and thus decoupled from others. H.264 performs Hadamard transform for the DC coefficients, and it is decoupled from others.

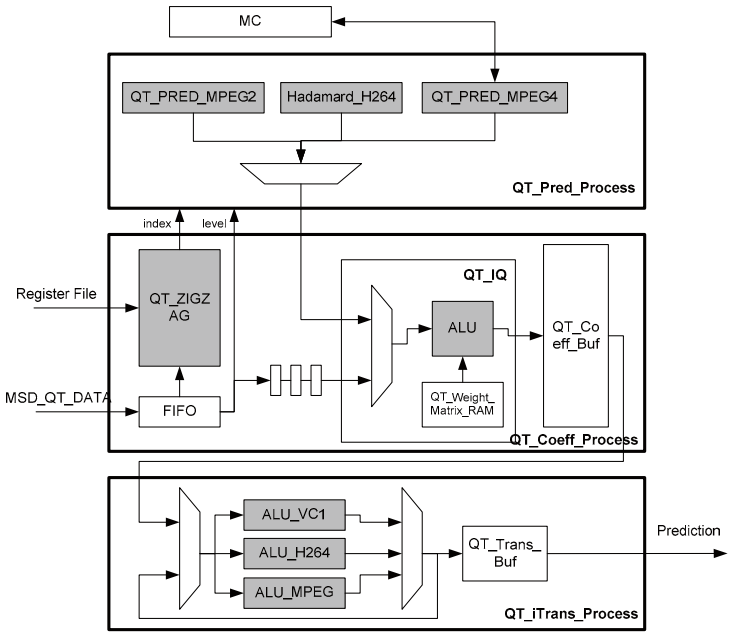

Fig. 2. Inverse Q/T Architecture

QT_Coeff_Process block performs the inverse zigzag scan and the inverse quantization. For the inverse zigzag scan, the scan table of MPEG-2 is the subset of that of MPEG-4 and can be shared with MPEG-4. However, VC-1 uses a very different scan table, and thus it is decoupled from others. The

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inverse quantization part is merged as one because of similarity across the codecs, and the common portion of the computation is very large.

QT_iTrans_Process block performs the inverse transform. MPEG-2 and MPEG-4 are designed as one since they use the same inverse transform matrix. H.264 and VC-1 are designed separately since they have different inverse transform matrices. However, the control logic for computations and the large transpose memory can still be shared.

3.3 Prediction

Prediction performs the reconstruction of the reference macroblock by using the motion vector. Figure 3 shows the architecture of Prediction. H.264 performs intra prediction, and VC-1 performs overlap transform for intra macroblocks. They are designed separately from others. Performing the motion reconstruction for inter macroblocks is common to all the codecs supported in the proposed MFD. The prediction of MPEG-2 is a complete subset of that of MPEG-4.The prediction of MPEG-4 is similar to, but not identical to that of H.264. Interpolation filters of these codecs are not quite large (i.e., H.264 8.9 K gates, VC-1 39.0 K gates and MPEG-2/MPEG-4 18.0 K gates). Therefore, the interpolation filters are designed using a decoupled architecture. The SRAMs can be shared to save the area.

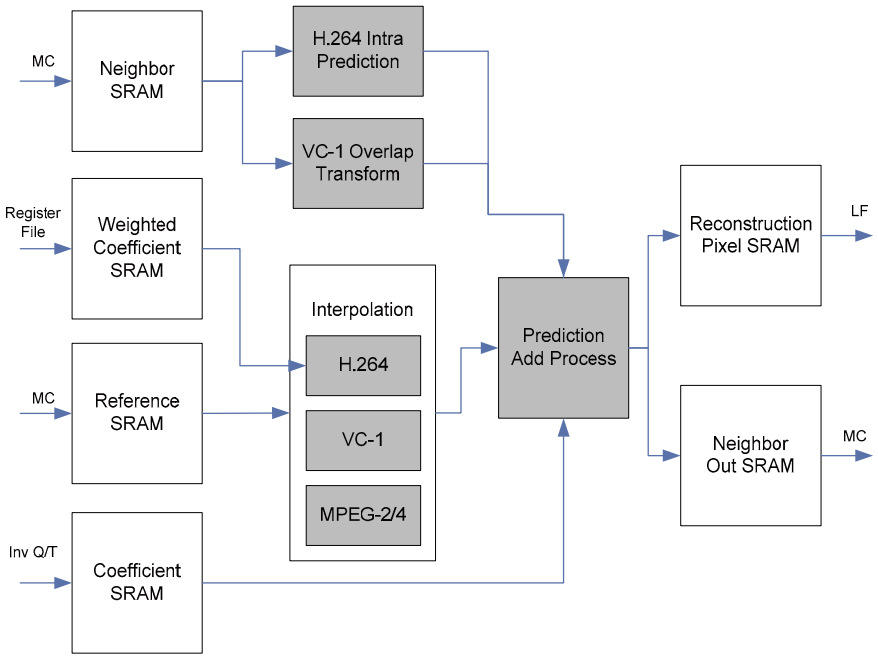

Fig. 3. Prediction Architecture

3.4 Loop Filter

The codecs using deblock filters are H.264, VC-1, and MPEG-4. Among these, H.264 and VC-1 use an in-loop filter and MPEG-4 uses a post-processing filter. The filter of H.264 or VC-1 can be reused as post-processing filter and replace that of MPEG-4. The filters of H.264 and VC-1 are very different

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except for the name. Therefore, a decoupled architecture is used for them. H.264 uses three different types of filters adaptively according to the boundary strength. More information about the design of H.264 loop filter module can be found in [8]. VC-1 uses only one filter. The size of the hardwired logic is 33 K gates for H.264 and 73.6 K gates for VC-1. However, SRAMs to store the filtering data are shared between the codecs to reduce the size.

4 Results

The proposed MFD is integrated into a D-TV SoC. It is critical to reduce the memory latency and secure enough memory bandwidth. The latency factors affecting the system performance are internal bus latency, external bus latency, and memory access time. The memory access time is the most critical factor, and thus a block-based addressing scheme is used to reduce it. Storing pixel values of a macroblock in the same row address of DDR improves the memory access time.

The proposed MFD is designed to work at the clock frequency of 225 MHz in Samsung 65 nm process. The overall size of the proposed MFD is 2.4 M gates. The size of the RISC processor with caches, on-chip memory, and the peripherals is 1.44 M gates, which is 60.1% of the total MFD. MSD is 334 K gates (13.9%). Inverse Q/T is 202 K (8.4%). Prediction is 290 K gates (12.1%). Loop filter is 132 K gates (5.5%).

5 Conclusion

In this paper, we have presented the VLSI design of MFD, which can support Full-HD (1080 p@60 fps) video and multiple video codec standards including MPEG-2, MPEG-4, H.264, and VC-1. The proposed MFD first reduces the design size dramatically by sharing the common large-sized resources, which account for more than 60% of the MFD area such as the RISC processor, on-chip memory, and interface logic. The remaining hardwired logic is designed using a decoupled architecture, so that design and verification time can be dramatically reduced and reliability is also improved.

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