

A 600 kHz to 1.2 GHz all-digital delay-locked loop in 65 nm CMOS technology

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Abstract: This paper presents an ultra-wide-range all-digital delay-locked loop (DLL). The proposed DLL uses a novel delay circuit which uses the transistor's leakage current in advanced CMOS process to generate a very large propagation delay. Thus, the proposed DLL can operate at very low frequency with small chip area and low power consumption. The proposed DLL can operate from 600 kHz to 1.2 GHz in the typical case. The power consumption of the DLL is 2.6 mW at 1.2 GHz and 0.366 mW at 600 kHz with 1.0 V power supply. The measured r.m.s jitter and peak-to-peak jitter at 1.2 GHz are 3.38 ps and 39.29 ps, respectively.

Keywords: digital delay-locked loop, delay line, delay circuit, clocks, synchronization, jitter

Classification: Integrated circuits

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1 Introduction

Delay-locked loops (DLLs) are widely used in high-speed microprocessors, memory interfaces and communication integrated circuits to eliminate the clock skew. To facilitate the DLL for various applications especially in low-power system-on-a-chip (SoC) with dynamic voltage and frequency scaling (DVFS), DLLs are desired to achieve wide-range operation.

Traditionally, DLLs are designed with charge pump based architecture [1]. However, the leakage current of the charge pump induces the ripples in the control voltage to degrade the overall jitter performance in nano-meter CMOS technology. In addition, a low supply voltage (1.0 V) in nano-meter CMOS technology presents a design challenge for an analog control loop to achieve wide-range operation. Hence, all-digital DLLs [2, 3, 4] with robust digital control code can avoid those problems and become more and more popular now.

The highest operating frequency of a DLL is limited by the minimum delay of the delay line while the lowest operating frequency is restricted by the maximum delay of the delay line. To enlarge the operation range of an all-digital DLL, a cycle-controlled delay unit (CCDU) [2] has been proposed to save area cost and power consumption. The CCDU reuses the delay units to enlarge the operating range rather than cascades a huge number of delay units. However, the programmable counter in the CCDU must run at very high speed to provide a reasonable delay line resolution. Otherwise, the area cost for designing the coarse-tuning delay unit and the fine-tuning delay unit will be too much. In addition, it is difficult to increase bits of the high-speed counter to extend the delay range of the delay line for low frequency operation.

In order to overcome those problems in nano-meter CMOS technology, a novel delay circuit (leakage delay cell) which uses the transistor's leakage current to generate a very large propagation delay is presented in this paper. The proposed all-digital DLL with leakage delay cells can enlarge the DLL operation range to a very low frequency with a small chip area and low power consumption. As a result, the proposed DLL is very suitable for wide-range clock de-skew applications.

2 The proposed DLL architecture

Fig. 1 (a) shows the architecture of the proposed DLL. It is composed of a phase detector, a DLL controller and a digital-controlled delay line which cascaded by four delay units namely: leakage delay unit (LDU), cycle-controlled delay unit (CCDU), coarse-tuning delay unit (CDU) and fine-tuning delay unit (FDU). The phase detector detects the phase error between the reference

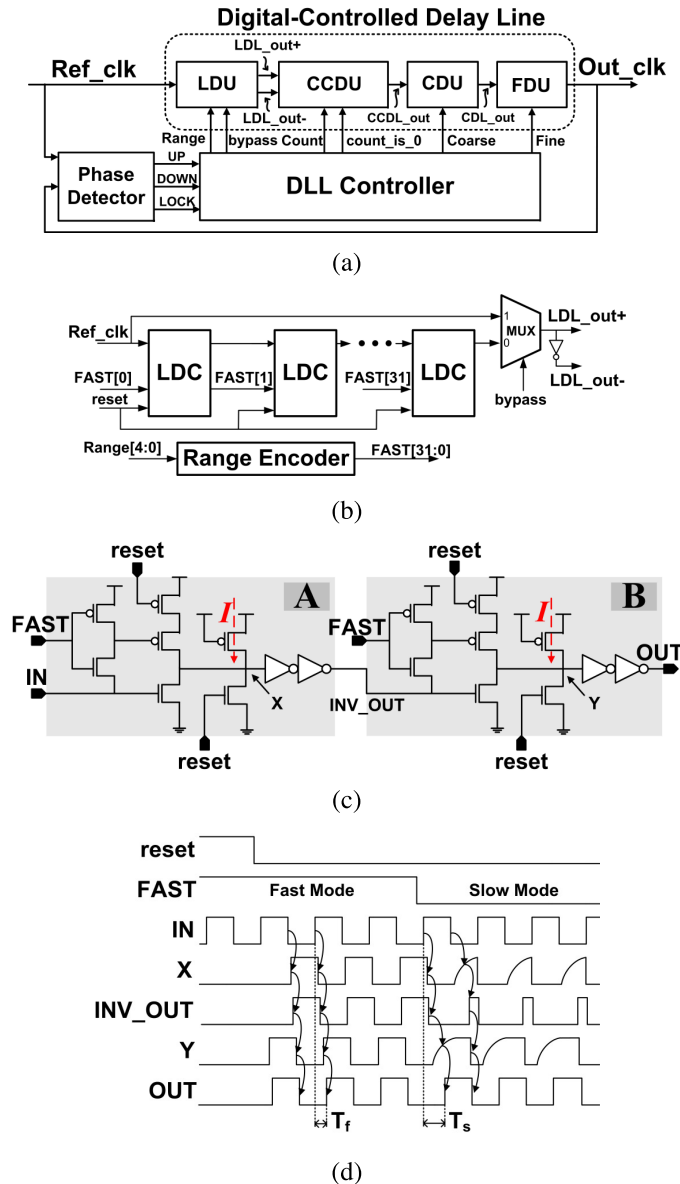


Fig. 1. (a) The proposed ultra wide range all-digital DLL (b) leakage delay unit (LDU) (c) leakage delay cell (LDC) (d) timing diagram of LDC

clock (Ref_clk) and the output clock (Out_clk), and it outputs UP/DOWN signal to the DLL controller which adjusts the control code of the delay line to increase or decrease the delay of the delay line. After system is reset, the DLL takes one cycle to initialize the delay line. After that, a binary search scheme is applied to shorten the lock-in time. At first, the DLL controller adjusts the control code of the LDU (Range[4:0]) to choose the operating range of the delay line. Subsequently, the DLL controller adjusts the control code of the CCDU (Count[6:0]), the CDU (Coarse[4:0]), and the FDU (Fine[4:0]) in order to minimize the residual phase error between the reference clock and the output clock.

In the proposed digital-controlled delay line, there are four cascading delay units. The controllable delay range of one delay unit must be larger than

the delay step of previous delay unit. Thus if the delay step of CCDU is T_d , the total controllable delay range of the CDU should be larger than T_d . If T_d can be reduced, the number of delay cells in the CDU can be also reduced. However, the minimum value of T_d is restricted by the maximum operation speed of the programmable counter in the CCDU [2]. Besides, it is difficult to directly increase the bits of the counter to enlarge the total controllable delay range of the CCDU. This is because the operation speed of the programmable counter becomes slower when bits are increased. Therefore, in the proposed DLL, the LDU is added in front of the CCDU to provide a required delay in low frequency operation with small area and low power consumption. The proposed LDU can provide a very large delay for saving the bits of the counter in the CCDU, and it enlarges the DLL operation range to a very low frequency.

3 Chip implementation

The proposed leakage delay unit (LDU) is composed of one 2-to-1 multiplexer and 32 leakage delay cells (LDCs) in series connection, as shown in Fig. 1 (b). When DLL operates at high frequency, the input reference clock (Ref_clk) is directly bypassed to the output (LDL_out+ and LDL_out-). Each LDC has one control pin to control the propagation delay. When “FAST[m]” is low, it means that the m-th LDC is in slow mode. Oppositely, when “FAST[m]” is high, the m-th LDC is in fast mode. The detail circuit of the proposed leakage delay cell (LDC) is shown in Fig. 1 (c), and the related timing diagram is shown in Fig. 1 (d).

The proposed LDC use transistor’s leakage current in standard performance (SP) 65 nm CMOS technology to generate a very large propagation delay. In the fast mode, the LDC works just like two cascading inverters with small delay time. In the slow mode, in part A of the proposed LDC, the delay from “IN” rising transition to “INV_OUT” falling transition is still very small. However, in part B of the LDC, the delay from “INV_OUT” falling transition to “OUT” rising transition becomes very large. This is because both the pull-up path and the pull-down path at node “Y” are switched off. The leakage current of the always-off PMOS transistor charges the node “Y” and continuously increases the voltage of this node. After a long time, the node “Y” will be charged to logic high. Similarly, when “IN” has falling transition, the delay from “IN” falling transition to “INV_OUT” rising transition is very large. In addition, the delay from “INV_OUT” rising transition to “OUT” falling transition is very small. Thus, the delay time of the LDC becomes very large in slow mode.

In the proposed LDC, the node “X” and node “Y” has four leakage paths in the slow mode. Therefore, the leakage current of the always-off PMOS transistor must be larger than the leakage current of the NMOS transistor to ensure the correct functionality of the proposed LDC. As a result, the always-off PMOS transistor should have a wider channel width, and the LDC should be verified with process variations in balanced process corners (TT/SS/FF)

and skew corners (SNFP/ FNFP). The delay times of the proposed LDC in different process corners are TT: 37.73 ns, SS: 270.67 ns, FF: 5.07 ns, SNFP: 13.04 ns, and FNFP: 166.55 ns.

The delay time of the proposed LDC is sensitive to process variations, thus, the delay controllable range of the next cycle-controlled delay unit (CCDU) must be larger than the delay step of the LDU with process, voltage, and temperature (PVT) variations. The CCDU is composed of two cycle-controlled delay cells (CCDCs) [2], an edge combiner and a 2-to-1 multiplexer. In order to generate an output with 50% duty cycle, two CCDCs and one edge combiner are used. In addition, a pair of complementary inputs, “LDL.OUT+” and “LDL.OUT-” with a 180 degree phase shift is required. When DLL operates at high frequency, the signal “count_is_0” will be pulled high to directly bypass the input signal (LDL.OUT+) to the output (CCDL_out).

The output transition of the leakage delay unit (LDU) enables the ring oscillator inside the CCDC. Once the ring oscillator is enabled, the output of the ring oscillator triggers the 7-bit programmable counter to count up until the specified counter value is matched to the input control code of the CCDU (Count[6:0]). Then, the programmable counter is reset and a positive edge transition is generated by the CCDC. Finally, the output delayed signals of the two CCDCs are edge combined to generate the output signal (CCDL_out) with 50% duty cycle. The delay time of the CCDC can be express as:

$$t = (c - 1) * T_d + \frac{T_d}{2}, \text{ for } c = 1 \sim (2^n - 1) \quad (1)$$

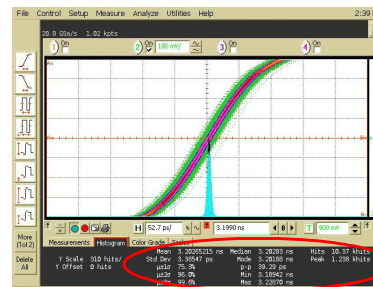
where c is the times that the CCDC is reused, and n is the bit number of the programmable counter.

To improve the overall delay resolution of the proposed delay line, a path selector type coarse-tuning delay unit (CDU) [6] and a digital-controlled varactor (DCV) type fine-tuning delay unit (FDU) [5] are inserted after the CCDU to enhance the resolution with pico-second scale. Moreover, the DLL controller is written with hardware description language (HDL), and the cell-based design flow is used to implement the full chip.

4 Experimental results and performance comparisons

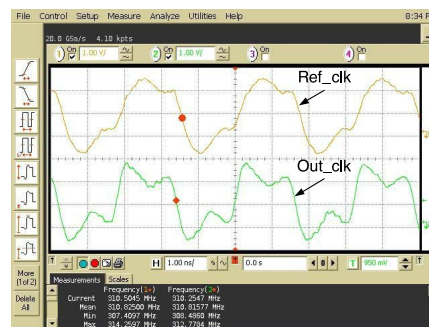
The proposed ultra wide-range DLL is fabricated on a standard performance (SP) 65 nm CMOS technology. One digital-controlled oscillator (DCO) is added in this test chip for testing the proposed DLL with high-speed reference clock. The DLL test chip can choose the reference clock source from an external reference clock or from the internal DCO. Due to the speed limitation of the I/O pads, the output clock frequency must be lowered for testing. Hence when internal DCO is chosen as the reference clock, the output of the DLL is divided by 4.

Fig. 2 (a) shows the measured long-term jitter histogram of the output clock at 1.2 GHz. The experimental result shows that the measured root-mean-square jitter and peak-to-peak jitter at 1.2 GHz is 3.38 ps and 39.29 ps,

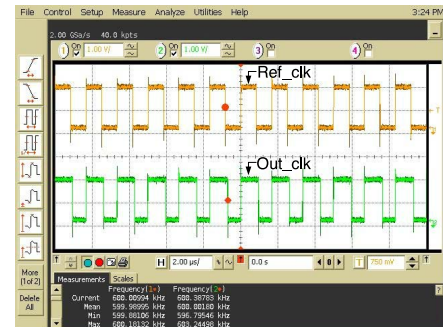


Mean	3.20265215 ns	Median	3.20283 ns	Hits	10.37 khits
Std Dev	3.38547 ps	Mode	3.20188 ns	Peak	1.238 khits
$\mu \pm 1\sigma$	75.3%	p-p	39.29 ps		
$\mu \pm 2\sigma$	96.0%	Min	3.18942 ns		
$\mu \pm 3\sigma$	99.6%	Max	3.22670 ns		

(a)



(b)



(c)

Fig. 2. (a) measured long-term jitter histogram at 1.2 GHz (b) locked state of the DLL at 1.2 GHz (c) locked state of the DLL at 600 kHz

Table I. Performance Comparisons

DLL	Proposed	JSSC'05 [2]	TCASII'10 [3]	JSSC'09 [4]	JSSC'05 [7]
Process	65nm CMOS	0.18 μ m CMOS	0.13 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS
Type	Digital	Digital	Digital	Digital	Analog
Supply (V)	1.0	1.8	1.2	1.8	1.8
Frequency Range (MHz)	0.6-1200	2-700	30-1000	440-1500	250-2000
r.m.s Jitter (ps)	3.38 (1.2GHz)	2.0 (700MHz)	N.A.	0.936 (1.5GHz)	2.81 (2GHz)
p-p Jitter (ps)	39.29 (1.2GHz)	17.6 (700MHz)	30 (1GHz)	7.0 (1.5GHz)	20.4 (2GHz)
Active Area (mm ²)	0.01	0.88	0.02	0.053	0.046
Power (mW)	2.6 (1.2GHz)	23 (700MHz)	3.6 (1GHz)	43 (1.5GHz)	6.4 (2GHz)

respectively. Fig. 2(b)(c) shows the measured output clock when the proposed DLL is locked at 600 kHz and 1.2 GHz. The operation range of the proposed DLL ranges from 600 kHz to 1.2 GHz in the typical case. The power consumption of the proposed DLL is 2.6 mW at 1.2 GHz, and is 0.366 mW at 600 kHz. Table I lists comparison results with existing wide-range DLLs. As compared with conventional approaches, the proposed DLL with leakage delay cells can generate a large delay time for low frequency operation, and the leakage delay cells only occupied a small area. Therefore, the proposed DLL is very suitable for wide-range frequency operation.

5 Conclusion

In this paper, an ultra wide-range all-digital delay-locked loop in 65 nm CMOS technology is presented. The proposed leakage delay cell with cycle-controlled delay unit can easily achieve ultra wide frequency range operation. The proposed DLL can operate from 600 kHz to 1.2 GHz. It also achieves smaller chip area and lower power dissipations than previous wide-range DLLs. As a result, it is very suitable for wide-range clock de-skew applications in SoC era.