

A study of clock and data recovery with composite structure of oversampling and gated oscillator for 10 Gbit/s subscriber network

Hitoyuki Tagami^{a)}, Norio Suzuki, and Seiji Kozaki

Information Technology R & D Center, Mitsubishi Electric Corporation,
5–1–1 Ofuna, Kamakura, Kanagawa 247–0051, Japan

a) Tagami.Hitoyuki@ab.MitsubishiElectric.co.jp

Abstract: A composite clock and data recovery circuit based on oversampling and a gated oscillator is proposed. The reduction in the number of multi-phase clocks to be integrated in current silicon technology is discussed. The tolerance to pulse-width variation in a data packet is predicted numerically for an application to 10 Gbit/s-based subscriber networks.

Keywords: FTTH, optical access system, PON, CDR, gated oscillator

Classification: Fiber-optic communication

References

- [1] *IEEE802.3av Task Force*, [Online] <http://www.ieee802.org/3/av/>
- [2] *FSAN NGA*, [Online] <http://www.fsanweb.org/>.
- [3] S. Yoshima, M. Nogami, S. Shirai, N. Suzuki, M. Noda, H. Ichibangase, and J. Nakagawa, "A 10.3 Gbit/s LAN-PHY based Burst-mode Transmitter with a fast 6 ns turn-on/off time for 10 Gbps-based PON Systems," *OFC2008*, San Diego, CA, USA, OWL4, Feb. 2008.
- [4] N. Suzuki, K. Nakura, M. Ishikawa, S. Yoshima, S. Shirai, S. Kozaki, H. Tagami, M. Nogami, A. Takahashi, and J. Nakagawa, "Demonstration of 10.3-Gbit/s Burst-mode CDR employing 0.13 μm SiGe BiCMOS Quadrature sampling IC and Data-phase decision-algorithm for 10 Gbps-based PON Systems," *ECOC2008*, Brussels, Belgium, P.6.03, Sept. 2008.
- [5] M. Ishikawa, N. Suzuki, H. Tagami, S. Kozaki, and A. Takahashi, "A study of an over-sampling burst-mode CDR with gated VCO for 10 Gbps PON systems," *COIN2008*, Tokyo, Japan, C-14-PM1-2, Oct. 2008.
- [6] H. Tagami, S. Satou, M. Nogami, K. Motoshima, and T. Kitayama, "156 Mbit/s burst-mode transceiver with a new bit synchronization technique for PON application," *ECOC 1996*, Oslo, Norway, ThC 2.4, Sept. 1996.
- [7] H. Tagami, S. Kozaki, K. Nakura, M. Nogami, and K. Motoshima, "A burst-mode bit-synchronization IC with large tolerance for pulse-width

- distortion for Gigabit Ethernet PON,” *IEEE Solid-state Circuits*, vol. 41, no. 11, pp. 2555–2565, Nov. 2006.
- [8] Y. Ota, R. G. Swartz, V. D. Archer III, S. K. Krotky, M. Bunu, and A. E. Dunlop, “High-speed, burst-mode, packet-capable optical receiver and instantaneous clock recovery for optical bus operation,” *J. Lightw. Technol.*, vol. 12, no. 2, pp. 325–331, Feb. 1994.

1 Introduction

The rapid growth of IP traffic has spurred the development of lower-cost and broader-band access services. Building on the world-beating success of 1 Gbit/s-based passive optical networks (PONs), 10 Gbit/s-based PON with a time division multiplexing topology is a promising approach for future subscriber networks. Although standards activities are being vigorously progressed [1, 2], technical breakthroughs are still required to realize such a high-speed PON [3, 4, 5].

The clock and data recovery (CDR) in a PON extracts a clock immediately from the header area of the burst packets and recover the data precisely at the optimum clock timing. The CDR also has to tolerate the pulse-width variation of the incoming data, because convergence errors in transmitting optical power, receiving gain, and threshold controls in the burst-mode optical transceiver induce large distortion in the pulse shape, especially at the beginning of burst packets. The effective CDR architecture to achieve the 10 Gbit/s-based response and the tolerance to pulse-width variation is currently the subject of feasibility studies.

An oversampling architecture [6], which selects the best data recovered at an optimum phase from the data-family sampled by multi-phase clocks (MPCs), is one candidate to realize a fast-response CDR. This type of CDR has the advantage of good tolerance to pulse-width variation [7]. Meanwhile, the generation of the MPCs requires high-speed silicon technology, and this requirement increases in proportion to the number of MPCs. Another candidate is a gated oscillator architecture, which restarts oscillation by detecting the pulse edges in data stream [8]. This type of CDR can generate a clock synchronized with the pulse phase in a relatively compact circuit. However, it can not tolerate pulse-width of less than 50% duty, because the clock edges are not placed at the center of the pulses but at the pulse edges. This paper proposes a novel 10 Gbit/s-based CDR combining the oversampling architecture with a gated oscillator. It is predicted numerically that approximately the same tolerance can be realized with half the number of MPCs compared with the conventional architecture.

2 Proposed architecture

An oversampling CDR is shown in Fig. 1 (a). The precisely arranged MPCs, of which the frequency and phase are synchronized with the system clock, are generated in advance by a ring-type voltage controlled oscillator (VCO) in a

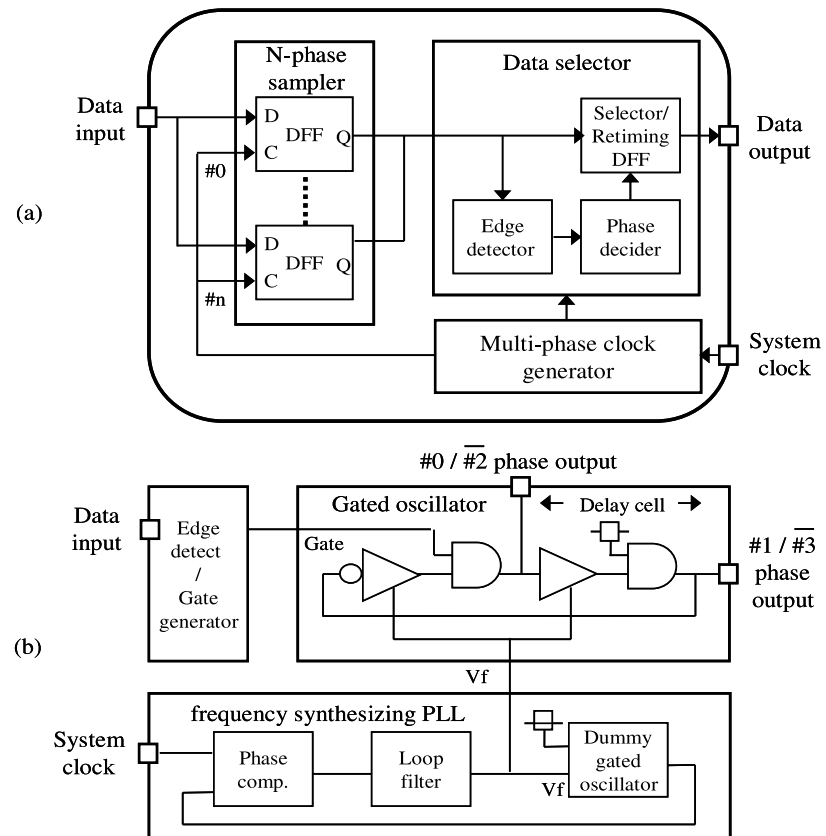


Fig. 1. Block diagram of CDR: (a) oversampling architecture, (b) 4 phase clock generator based on gated oscillator

PLL-based MPC generator. An incoming data packet with arbitrary phase is sampled by the MPCs in an N-phase sampler. A data selector selects the best pulse sampled at an adjacent optimum phase using the following function:

$$\Phi_{sel} = \text{Integer} \left(\frac{\Phi_{rise} + \Phi_{fall}}{2} \right) \quad (1)$$

where Φ_{sel} is the phase of the MPC to be selected, and Φ_{rise} , Φ_{fall} are respectively the phases of the rising and falling pulse edges detected by the MPCs. Here, the VCO in the MPC generator and the DFFs in the N-phase sampler have to operate at a speed of more than the bit-rate, and the operating speed increases in proportion to the number of MPCs. A previous report shows that more than 8 MPCs are required to achieve sufficient tolerance to pulse-width variation [7], but the current silicon technology cannot support a 10 Gbit/s conventional CDR with 8 MPCs, which needs an operating speed equivalent to 80 GHz.

The MPCs are here proposed to be generated by a gated oscillator. An example of a 4 phase clock generator based on a gated oscillator is shown in Fig. 1 (b). Since the gated oscillator is permitted to restart oscillation by the gate signal created by detecting the pulse edges, a phase-synchronized clock can be generated. The ring connection between the same 2 delay cells gives accurately quadrature phases to the MPCs [7]. The oscillation frequency, i.e. the delay time through the delay cells, is set by the control voltage at

terminal Vf, which is generated in the frequency synthesizing PLL with a dummy gated oscillator of the same configuration [8].

3 Phase error

Fig. 2 shows the decision process for optimum phase with the worst pulse distortion, i.e. almost 25% duty, both for the conventional architecture with 8 phase clocks and the proposed architecture with 4 phase clocks. Since the MPC phase is not correlated with the incoming pulse phase in the conventional architecture, two extreme conditions are discussed for the case where the rising edge is located between clock phases #1/8 and #2/8. In both conditions, phase #3/8 is selected as the optimum by equation (1), because the rising edge at #2/8 and the falling edge at #4/8 are detected. Then, the phase error between the selected clock and the central phase of the pulse is about 1/8 unit-interval (UI) at most. In the proposed architecture with 4 phase clocks, phase #1/4 is selected for the optimum, because the rising edge at phase #0/4 and the falling edge at #2/4 are detected independently of the pulse phase by the fixed correlation of the MPC phases. The phase error of about 1/8 UI is the same as that for the conventional architecture with 8 phase clocks, despite the reduction of MPCs by half.

As a supplementation, the jitter on the incoming data is not suppressed by the gated oscillator, of which bandwidth for the jitter transfer is not limited ideally. Since the jitter on the data passes through the oscillator to the clocks, the residual jitter between the data and clock does not exist with the exception of the jitter generated internally in the oscillator. This fact in

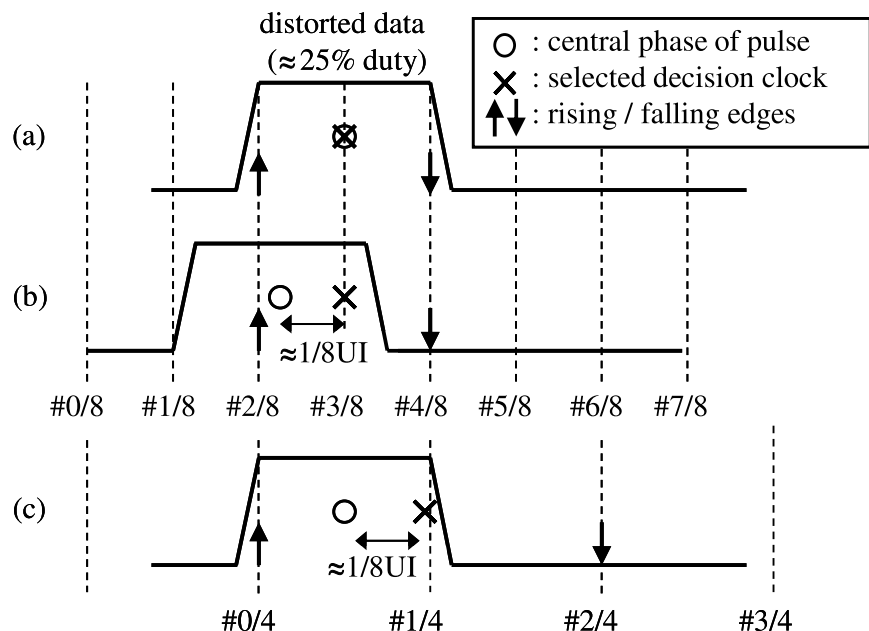


Fig. 2. Phase selection at the worst pulse-width distortion: (a) rising edge right before #2 for conventional architecture with 8 MPCs, (b) rising edge right after #1 for conventional architecture with 8 MPCs, (c) proposed architecture with 4 MPCs

the propose architecture is preferable for a good tolerance to the distorted data.

4 Distortion tolerance

The tolerance to pulse-width variation is discussed quantitatively. If the rising and falling edges are detected at neighboring phases, the central phase to be selected as the optimum does not exist. In other words, as shown in Fig. 2, a data pulse has to involve at least 3 phases for the conventional architecture, whereas 2 phases are required for the proposed architecture due to the fixed phase correlation between the data edge and the MPCs. These conditions can be expressed as the pulse-widths needing to be more than $2/N$ and $1/N$ UI for N -phase MPCs, respectively. Considering the phase degradation caused by the sum of setup and hold times (Tsh) of the sampling DFFs, the clock jitter generated internally in the MPC generator ($Jclk$), the phase error (Pe) between the MPCs at the input of the DFFs, and the sinusoidal data jitter ($Aj \cdot \sin(2\pi \cdot Fj)$) in M -bit interval of bit period ($M \cdot Tb$) for edge detection [7], the distorted pulse-width ($1 - D$) expressed in UI has to satisfy the condition:

$$1 - D \geq \frac{n}{N} + Tsh + Jclk + Pe + Aj \cdot \sin(2\pi \cdot Fj \cdot M \cdot Tb) \quad (2)$$

Fig. 3 shows the calculated tolerable distortion (D) as a function of phase number (N). The proposed architecture with 4 phase clocks can tolerate up to 0.64 UI, which is the same value for the conventional architecture with 8 phase clocks as qualitatively predicted in the phase error section. Although the tolerance specification for 10 Gbit/s PON has not been standardized, 0.2 UI can be assigned for the additional distortion generated in an optical receiver over the 0.44 UI distortion on the optical fiber specified for GE-PON systems.

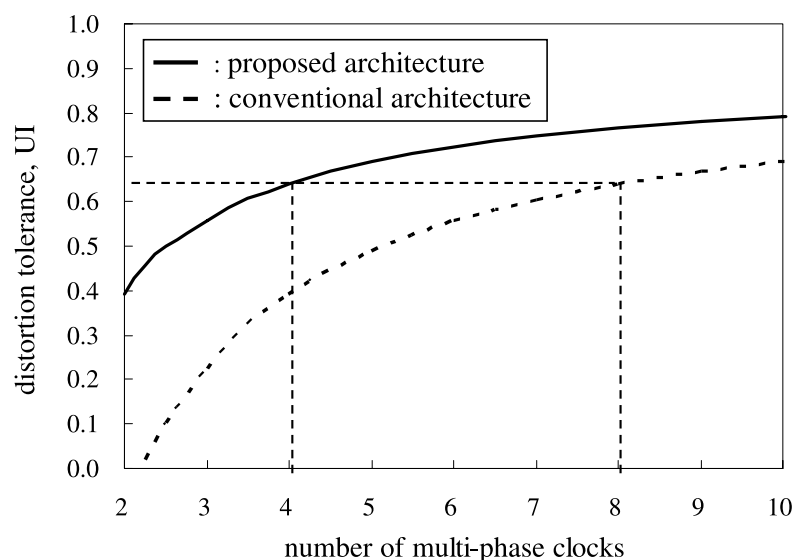


Fig. 3. Calculation results of distortion tolerance

5 Advantages of proposed architecture

Keeping a good tolerance to pulse-width variation in the data packet, the number of the MPCs can be reduced by half, i.e. from 8 phases in the conventional to 4 phases in the proposed architecture. The reduction in the MPCs contributes to the easy design of the integrated circuit under the current silicon technology. The 10 Gbit/s conventional CDR with 8-phase clocks requires an operating speed equivalent to 80 GHz for the MPC generator and the N-phase sampler, whereas the proposal CDR with 4-phase clocks requires that to 40 GHz. This requirement is sufficiently reduced for the circuit integration by 0.12 μ m SiGe bipolar transistors with 200 GHz cutoff-frequency, which is the fastest silicon available commercially.

The reduction in the MPCs also ensures the saving of power consumption and chip area to realize an ecological and economical system. An estimation on the basis of circuit simulation and pattern layout shows that both of the power and chip area can be cut by nearly 40%, considering the additional effect of the reduction in buffer circuits to transmit signals. The power saving facilitates the design of heat radiation for packaging and assembling on a board.

6 Conclusion

Using a gated oscillator in the MPC generator has been proposed on the basis of an oversampling architecture for a 10 Gbit/s CDR. The 4-phase MPC reduced by half allows finally the circuit integration on the fastest silicon, and contributes to the power and cost savings. The tolerance to pulse-width variation is maintained sufficiently for the stable operation of 10 Gbit/s subscriber networks.

Acknowledgments

The authors would like to thank Mr. M. Poole for his fruitful comments.