

Dynamic-static hybrid near-threshold-voltage adder design for ultra-low power applications

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Abstract: Near-threshold-voltage (NTV) circuit is to set the operating voltage near the threshold voltage of CMOS transistors to pursue the maximum energy efficiency. However, the characteristics for each logic family are quite different under NTV while comparing to its operation under normal supply voltage. In this paper, we proposed a new dynamic-static hybrid near threshold voltage adder design. The proposed keeper design can suppress the leakage current and avoid signal contention in the dynamic CMOS circuit, which lets the dynamic CMOS logic family can be adapted to NTV environment with excellent speed characteristics and higher energy efficiency. The proposed low leakage dynamic-static hybrid NTV 32-bits adder design can achieve the maximum energy efficiency with 161.7% enhancement as compared to the mirror adder under NTV with 0.3 V.

Keywords: near-threshold voltage, energy efficiency

Classification: Integrated circuits

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1 Introduction

Nowadays, portable devices are more and more popular. Due to the volume limiting the battery capacity, how to effectively reduce power consumption of the core CPU, ALU, and DSP is a crucial challenge in SoC design. To power consumption, reducing the chip operating voltage is the most efficient way. However, it also causes the drastic degradation of circuit performance. To make the circuit system capable of operating in lower operating voltage and to enhance the power efficiency, since 2012, Intel began to vigorously promote Near-Threshold-Voltage (NTV) [1] design. NTV is a new low-power design concept to pursue maximum energy efficiency. NTV operating voltage is set closing to the threshold voltage of MOS transistors, instead of unlimitedly lowering the operating voltage [2].

In the past arithmetic logic circuit design, different logic families have respective characteristics and application ranges. For example, the static CMOS circuit design is a ratio-less circuit and has a wider noise margin; the dynamic CMOS circuit design has a better computing speed. However, when the circuit is operated at low voltage, problems in dynamic CMOS circuit design, such as charge sharing and floating node disturbance are highlighted. In addition, the keeper in the evaluation phase, the pull-up network and the pull-down network have serious signal contention, resulting in huge power consumption generally more than 10 times greater than the power consumption of static CMOS circuits under NTV. Therefore, static CMOS circuit design is often regarded as a more feasible design in low voltage operation. However, as long as the floating issue can be resolved in the case without causing signal contention and ratio logic issues, the dynamic CMOS circuit in NTV environment still has a chance to show excellent performance.

In this paper, we proposed a new dynamic-static hybrid near threshold voltage adder design. We adopt dynamic CMOS logic to realize sum generation circuit of mirror adder and adopt static CMOS logic to realize the carry generation circuit. Through the dynamic CMOS circuit, the “sum” generation circuit is realized, making the load of the “carry” generating circuit reduce and improve the speed of the “carry” signal propagation. In the dynamic part of the circuit design, we present a new keeper circuit design to suppress the leakage current and avoid signal contention in the dynamic CMOS circuit. Controlling the keeper circuit with the inverted clock signal together with the delayed clock signal, we can further divide the “evaluation phase” in conventional dynamic circuits into “evaluation phase” and “isolation phase” and thus significantly reducing the leakage current consumption caused by the dynamic CMOS circuit in the “evaluation phase” and enhancing energy efficiency of the adder circuit under NTV.

2 The proposed dynamic-static hybrid NTV adder design

In the static CMOS adder design, the traditional 28T full adder [3] can be divided into carry generation circuit and the sum generation circuit. The 28T adder can be simplified to mirror adder with smaller area [3]. Pseudo-nMOS and dynamic-static hybrid full adder [3] may be candidates for designs in high speed considerations. However, the pull-up pMOS of Pseudo-NMOS design results in huge DC power

consumption. Dynamic circuit is also attractive in high speed applications; however, when the dynamic circuit is operated in NTV region, a large amount of power consumption is generated in the evaluation phase due to the leakage path arising from the keeper which maintains the voltage level.

Fig. 1 shows the dynamic-static hybrid NTV adder proposed in this paper. The circuit can be divided into the static part which is utilized to generate the “carry,” the dynamic part which is utilized to generate the “sum,” and the delay line which is utilized to generate the control signal for the keeper circuit in dynamic part. In carry generation circuit, since the driving ability of the dynamic circuit is poor for cascaded designs, we adopt the static CMOS logic to realize the carry generation circuit. We adopt the proposed dynamic CMOS logic to realize the sum generation circuit to reduce the load capacitance of carry generation circuit, therefore the carry generation can operate faster. In addition, through the hybrid design of the dynamic and static circuit, we can allow timing borrowing between the static “carry” generation and the dynamic “sum” generation, enabling to enhance the process variation tolerance under NTV.

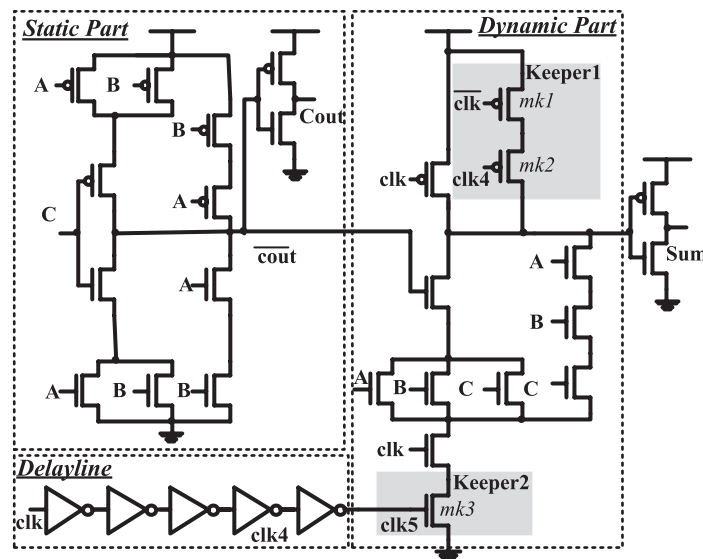


Fig. 1. The proposed dynamic-static hybrid NTV adder

In order to avoid the traditional output conditional feedback keeper design resulting in decreasing speed and increasing power consumption due to signal contention and output load increases, and the ratio circuit structure under NTV, we adopt mk1 with mk2 transistors as the “keeper” in proposed dynamic CMOS logic structure. The gate terminals of mk1 and mk2 are controlled by the reverse clock signal CLKB and the delayed clock signal CLK4, respectively. As “keeper” enters the evaluation phase, mk1 and mk2 are conducting and CLKB signals can turn-on mk1 immediately to provide with leakage compensation path and charge sharing compensation path. During “pre-charge phase,” mk1 is turned-off, without increasing additional leakage path. CLK4 further turns-off mk2 transistor in the keeper to enter the “isolation phase” after evaluation state of the pull-down network (PDN)

stabilizes. As a result, after the dynamic circuit enters the “isolation phase”, not only output level is held through the keeper but also the issues in signal contention, the formation of the ratio circuit, DC current conduction path, and the charge leakage path are avoided; thus significantly reduced power consumption during evaluation phase. The proposed leakage isolation dynamic circuit design and operation schematic diagram is as shown in Fig. 2. In conventional dynamic design, the conditional feedback keeper forms a DC path in whole period of evaluation phase leads to enormous leakage power. As the circuit operates under NTV region, the percentage of leakage power in total power would increase much higher than that operates under normal supply voltage. In the proposed design, transistors mk1 and mk2 are keeper transistors to maintain the output level when the circuit is operated in NTV. The mk3 transistor is PDN leakage barrier to reduce the leakage current in PDN path. This design can also reduce the burden of leakage current compensation of mk1 and mk2 transistors. In the proposed leakage isolated dynamic circuit design, the biggest difference from the traditional dynamic circuit design lies in the condition that we further separate “evaluation phase” of traditional dynamic circuit into “evaluation phase” and the “isolation phase” by increasing leakage barrier under NTV through delay clock signals, as shown in Fig. 2. When clock signals are switched into “High,” the circuit enters the “Eva. Phase”. Meanwhile, the keeper circuit controlled by CLKB and CLK4 can remain open for a period of time to make the dynamic circuit operations correctly in the “Eva. Phase”. Then, the dynamic circuit enters “Iso. Phase” immediately by turning-off transistors mk2 and mk3 to isolate the possible leakage path to reduce power consumption. As shown in Fig. 2, leakage current is much smaller as compared with traditional dynamic circuit design in “Eva. Phase” by introducing “Iso. Phase,” therefore total power of proposed design can be decreased significantly under NTV environment.

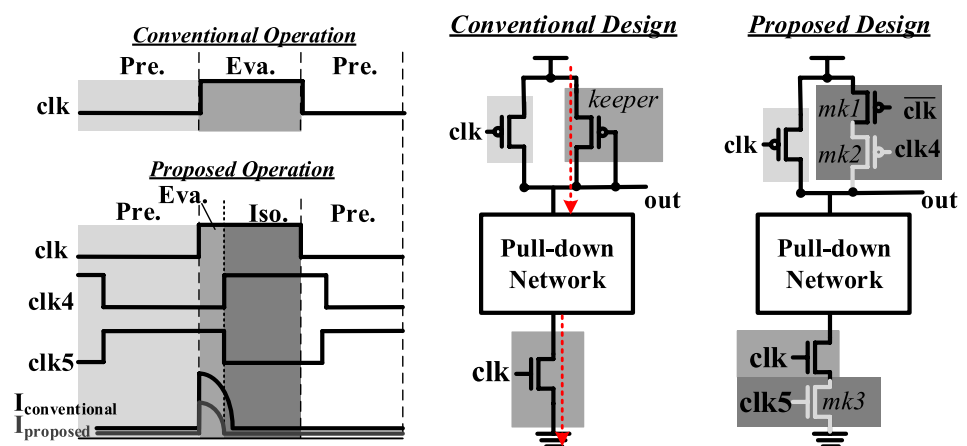


Fig. 2. The design and operating diagram of conventional and the proposed dynamic design

3 Simulation and performance comparison results

In order to demonstrate the energy efficiency of proposed NTV adder design, we conduct performance analysis and comparison of various 32-bit adder designs constructed by conventional 28T full adder, mirror adder, Pseudo-NMOS adder, conventional dynamic-static hybrid adder, and the proposed dynamic-static hybrid NTV adder under TSMC 90 nm CMOS technology process. We analyze the delay of the critical path of each circuit under different operating voltages and average power consumption at such speed, which is shown in Fig. 3(a). Fig. 3(b) shows the simulation waveform of current comparison between the proposed design and conventional dynamic design. We can find that also active or leakage current of proposed design is smaller than conventional design. As shown in Fig. 3(a), the critical path delay of proposed design just increased a little bit as compared with the conventional dynamic-static hybrid design. However, even the extra transistor in discharging path of proposed design may decrease the discharging current; the output capacitance of proposed design is also decreased by removing the conditional feedback keeper. Therefore, the performance can be maintained in the proposed design. The delay of proposed dynamic-static hybrid NTV adder design can be reduced by 28.4% and 33.2% as compared with mirror adder and traditional 28T full adder, respectively. The power consumption of proposed design can decrease 95.4% in average as compared with conventional dynamic-static hybrid adder, and 2.75% saved compared with static mirror adder. In the proposed hybrid NTV circuit, DC power, dynamic power, and leakage power consumption can be significantly lowered. Besides, the dynamic circuit design can enhance the circuit speed, thereby enabling the energy efficiency of the overall circuit increase dramatically. We further evaluate the performance of each design based on the energy efficiency. As shown in Fig. 4, the proposed design achieves maximum energy efficiency at supply voltage of 0.3 V. Under PVT variation, process corner of TT 25°C, FF 0°C and SS 100°C, the energy efficiency can be enhanced by 161.7%, 168.3% and 132.9%, respectively as compared with static mirror adder. Moreover, area of the proposed 32-bit adder is only 93.9% of the static mirror adder owing to hybrid design can omit the PUN of sum generation.

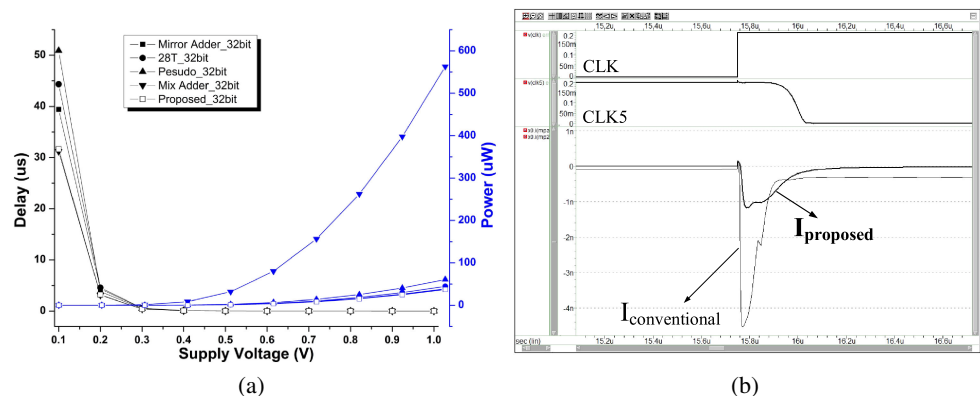


Fig. 3. (a) Performance of various designs with voltage variation.
(b) Comparison of current simulation results.

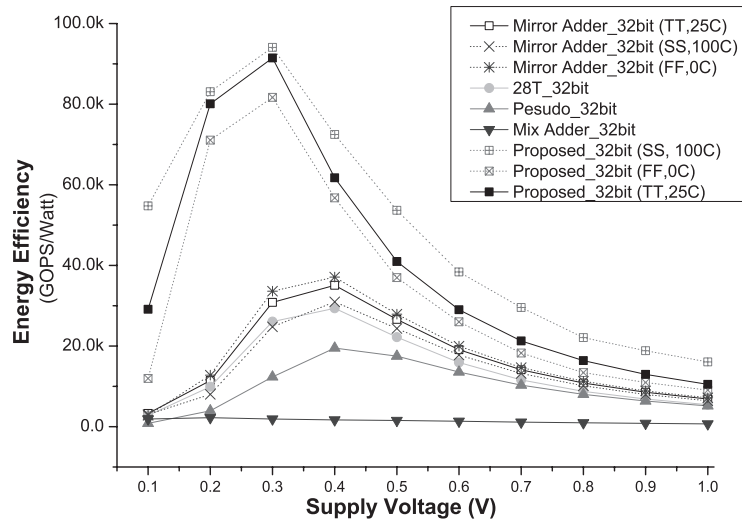


Fig. 4. Comparison of energy efficiency.

4 Conclusion

A dynamic-static hybrid NTV adder design is proposed, a new dynamic CMOS logic control technique is presented to divide the “evaluation phase” in conventional dynamic circuits into the “evaluation phase” and the “isolation phase”. In this way, the power consumption in dynamic CMOS circuit can be lowered significantly and energy efficiency can be greatly enhanced under NTV. As a result, dynamic logic family can be a suitable and attractive candidate under NTV. This work was supported by National Science Council, R.O.C., under Contract MOST-103-2220-E-182-001.