ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.15, 1–7

A 0.5 V 0.18 μm CMOS LC-VCO with a novel switched varactor technique

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Abstract: A 0.5 V LC-VCO implemented in 0.18 μm CMOS with a novel switched varactor technique is described in this paper. This novel switched varactor technique can increase the varactor control voltage variation range and increase Q of LC tank; also it can reduce phase noise and power consumption of VCO. Forward-body bias technique is used to reduce the threshold voltage and improve g_m of transistor. The measured operating current is 4.4 mA and the tuning range is 4.6∼5.2 GHz. The phase noise is −114 dBc/Hz at 1 MHz from carrier frequency 4.8 GHz.

Keywords: low voltage, low power, varactor, forward-body bias

Classification: Integrated circuits

References

[1] S.-A. Yu and P. Kinget: IEEE J. Solid-State Circuits **44** (2009) 2411.

[2] S. Pellerano, S. Levantino, C. Samori and A. L. Lacaita: IEEE J. Solid-State Circuits **39** (2004) 378.

[3] P. Kinget: ISSCC Dig. Tech. Papers (1998) 226.

[4] Y.-K. Chu and H.-R. Chuang: IEEE Microw. Wireless Compon. Lett. **13** (2003) 287.

[5] E. Hegazi, J. Rael and A. Abidi: *The Designer's Guide to High-Purity Oscillators* (Kluwer Academic Publishers, New York, 2005).

[6] A. Lacaita, S. Levantino and C. Samori: *Integrated Frequency Synthesizers for Wireless Systems* (Cambridge University Press, New York, 2007).

[7] M. Marin, M. J. Deen, M. de Murcia, P. Llinares and J. C. Vildeuil: IEE Proc.–Circuits Devices Syst. **151** (2004) 95.

1 Introduction

Low voltage circuit design techniques are widely researched for low power communication systems [1, 2, 3, 4]. VCO is an important building block in the frequency synthesizer. The difficulties of VCO design are the achievable wide-tuning range with low phase noise and low power consumption. Especially for low voltage VCO circuit design, these problems are more

DOI: 10.1587/elex.10.20130535
Received July 09, 2013
Accepted July 11, 2013
Publicized July 23, 2013
Copyedited August 10, 2013

severe. Low power supply voltage leads to narrower tuning voltage range and smaller output amplitude, and consequently decreases output frequency tuning range and degrades phase noise performances of VCO. Traditionally switched MIM capacitor techniques [6] shown in Fig. 1 cannot be used in 0.5 V power supply VCO. Since the threshold voltage of normal NMOS transistors in 0.18 μm CMOS process is about 0.5 V, the normal transistors cannot be turned on. And the size of low-threshold transistor M_0 needs to be larger to decrease the on resistance of transistor, which can lead to large parasitic capacitance when the transistor is off. So the switched MIM capacitor cannot achieve high Q and wide tuning range simultaneously when the power supply voltage is 0.5 V.

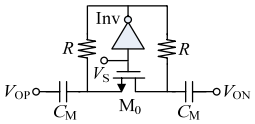

Fig. 1. Schematic of traditional switched MIM capacitor

2 Proposed techniques

To increase the output frequency tuning range in low voltage VCO, switched varactor techniques have been used in Reference [1], but it requires that the gate voltage (V_{OP}, V_{ON}) of varactor is biased at half of the power supply to fully exploit the capacitance variation [2] shown in Fig. 2 (a). So it isn't suitable for low voltage VCO structures whose V_{OP} and V_{ON} are biased at the power supply or ground. The schematic of proposed switched varactor technique is shown in Fig. 2 (b). It consists of a varactor C_0 and a MIM capacitor C_C in series, and the gate voltage V_G of varactor is biased by the output of inverter (Inv) through resistor R_0. The voltage V_{GS} (V_G-V_S) across the varactor used for coarse tuning is $\pm V_{DD}$, which is twice as much as that in Ref. [1]. The total value C_S of C_0 and C_C in series is shown in equation (1) and derivation of C_S is shown in equation (2). When the value of C_C is equal to C_0 at V_{GS}=0 V, dC_S/dV_{GS} is 1/4 of dC_0/dV_{GS} around V_{GS}=0 V. The lower the dC_s/dV_{GS} is, the smaller the varactor nonlinearity [5, 6]. When the ratio of C_C and C_0 at V_{GS}=0 V is smaller than 1, the series capacitance variation range is becoming smaller. When C_S is equal to C_1 (Fig. 2 (a)) at V_{GS}=0 V, to make the C_S capacitance variation range 1/2 times that of C_1, the ratio of C_C and C_0 is selected as 1.

$$C_S = \frac{C_0 \cdot C_C}{C_0 + C_C} \tag{1}$$

$$\frac{dC_S}{dV_{GS}} = \left(\frac{C_C}{C_C + C_0}\right)^2 \frac{dC_0}{dV_{GS}} \tag{2}$$

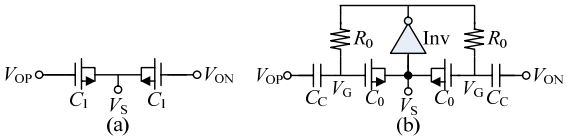

Fig. 2. (a) switched varactor in Ref. [1] (b) proposed switched varactor technique

DOI: 10.1587/elex.10.20130535
Received July 09, 2013
Accepted July 11, 2013
Publicized July 23, 2013
Copyedited August 10, 2013

For comparison of only one varactor in Ref. [1] with the proposed technique using a varactor in seris with a MIM capacitor shown in Figs. 3 (a) and (b), let the value of C_1 (with V_{GS}=0 V) equal to the value of C_0 (with V_{GS}=0 V) in series with C_C. The simulated capacitance value and derivation of these capacitances versus V_{GS} of Fig. 3 are shown in Figs. 4 (a) and (b). Since the power supply is 0.5 V, it can be seen from Fig. 4 (a) that the ratio of C_{max}/C_{min} (the capacitance value at $\pm$0.25 V) is 1.62 in Fig. 3 (a) and the ratio of C_{max}/C_{min} (the capacitance value at $\pm$0.5 V) is 1.52 in Fig. 3 (b). From Fig. 4 (b) the derivation of capacitance is much lower in Fig. 3 (b) than that in Fig. 3 (a), and the maximum dC/dV_{GS} in Fig. 3 (b) is about one half of that in Fig. 3 (a). In an LC oscillator, the approximation of oscillation frequency is given by equation (3) and the gain K_{VCO} is shown in equation (4) [5], where L is the effective inductance and C_{avg} is the effective capacitance at balance. The smaller the capacitance derivation is, the lower the K_{VCO}. Moreover the smaller K_{VCO} leads to lower phase noise and AM-FM conversion noise in VCO [6]. So the proposed techniques can lead to lower nonlinearity and phase noise of VCO than that in Ref. [1]. The Q of MIM capacitor is much higher than that of varactor, so the Q of Fig. 3 (b) is higher than that of Fig. 3 (a). The simulated Q of Fig. 3 shows that the Q of Fig. 3 (b) is about 40% higher than that in Fig. 3 (a) from Fig. 5. The higher Q of varactor leads to higher Q of LC tank, so the proposed techniques can lead to higher output amplitude and lower power consumption of VCO [5, 6] than that in Ref. [1]. As a result, the proposed techniques can be used for coarse tuning of low voltage VCO.

$$\omega_o = \frac{1}{\sqrt{LC_{avg}}} \tag{3}$$

$$K_{VCO} = \frac{\omega_o}{2C_{avg}} \frac{\partial C_{avg}}{\partial V_{GS}} \tag{4}$$

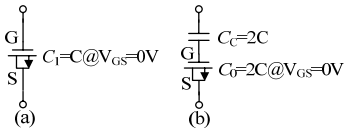

Fig. 3. (a) Only one Varactor in Ref. [1] and (b) Proposed technique

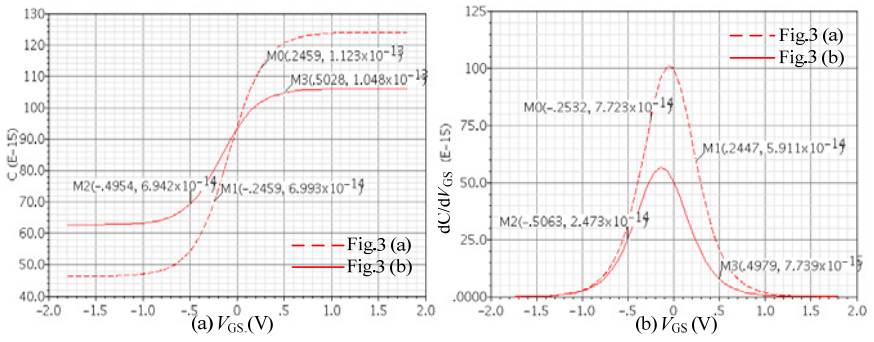

Fig. 4. Simulated (a) capacitances and (b) capacitance derivations of conventional and proposed techniques

DOI: 10.1587/elex.10.20130535
Received July 09, 2013
Accepted July 11, 2013
Publicized July 23, 2013
Copyedited August 10, 2013

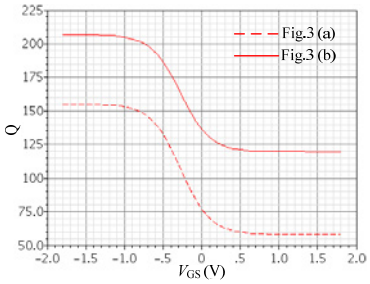

Fig. 5. Simulated Q of conventional and proposed techniques

3 The circuit design

The proposed VCO circuit is shown in Fig. 6 (a). Since the power supply voltage is 0.5 V and the threshold voltage (V_{th}) of RF-NMOS with the body voltage of 0 V in 0.18 μm CMOS process is about 0.5 V, the NMOS transistor can only work in the sub-threshold region and has lower cut-off frequency (f_T). If the transistors operate in the sub-threshold region and its size need to be larger to make VCO start-up, its parasitic capacitance may decrease the tuning range of VCO. Lower cut-off frequency may increase the trans-conductor delay and make oscillation frequency shift back from $(1/LC)^{1/2}$ [6]. The simulated V_{th} and f_T of RF-NMOS transistor as body voltage VB are shown in Figs. 7 (a) and (b) respectively. When the voltage VB is 0.5 V, the V_{th} is 418 mV and the transistor can operate in the saturation region. The f_T increases from 9 GHz to 20.6 GHz when VB varies from 0 to 0.5 V. The turn on voltage of substrate-source (substrate-drain) junction in 0.18 μm CMOS process is about 0.6 V, so the forward-body bias voltage of 0.5 V is adopted in the transistor to reduce the threshold voltage

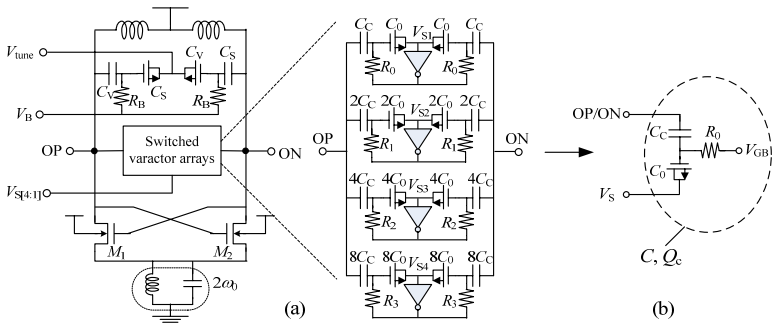

Fig. 6. (a) Proposed VCO circuit (b) single-ended switched varactor with gate bias resistor

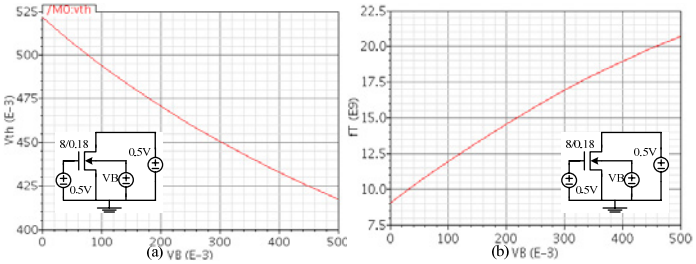

Fig. 7. Simulated (a) V_{th} and (b) f_T as the body voltage VB

DOI: 10.1587/elex.10.20130535
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(V_{th}) and increase the g_m without PN junction turned on. In strong inversion, the noise level was found to be approximately independent of the substrate bias V_{BS} [7].

The NMOS cross-coupled employing a network resonate at $2\omega_0$ without the tail current transistor is used in the VCO circuit. The power supply affects the amplitude of oscillation. Therefore it has to be generated by a low-noise low-drop out regulator. However, a similar problem also arises in the topology with the tail current generator: the amplitude is set by the bias current and by the tank parallel resistance. Even if the former is independent of supply variations, the latter suffers from variations over the tuning range and process spreads. A low-noise amplitude control loop is therefore necessary in that case [6]. To improve the PSRR of the proposed VCO, the de-coupling capacitance between the power supply and ground should be as large as possible.

The fine tuning technique also uses the varactor C_V and MIM capacitor C_S in series and the ratio of them at V_{GS}=0 V is set to 1. To make the varactor C_V operate in the linear region the gate voltage of C_V is biased at 0.15 V through the resistor R_B. The bias resistor R_B has a trade-off between Q of the tank and phase noise of VCO [6]. The equivalent effective capacitance is denoted by C with a quality factor of Q_c shown in Fig. 6 (b), C has a maximum value C_{max} with a quality factor $Q_{c,max}$ and a minimum value C_{min} with a quality factor $Q_{c,min}$, and its difference value (C_{diff}) is given by equation (5), where $C_{0,max}$ and $C_{0,min}$ are the maximum and minimum capacitance of C_0, and Q_c is given by equation (6). Since the ratio of four switched varactor and MIM capacitor in series shown in Fig. 6 (a) is set to 1:2:4:8, when the ratio of resistors $R_0 \sim R_3$ (R_0:R_1:R_2:R_3) used for gate bias of four switched varactors is 8:4:2:1, the $Q_{c,max}$ of four switched varactors would be equal from equation (6), also the $Q_{c,min}$ of four switched varactors would be equal too. Only when the above conditions are satisfied, the ratio of four equivalent effective capacitance differences (C_{diff}) is 1:2:4:8 from equation (5), and consequently the step size of switched varactor arrays capacitances used for coarse tuning is equal.

$$\begin{aligned} C_{diff} &= C_{max} - C_{min} \\ &= \frac{C_{0,max} \cdot C_C}{C_{0,max} + C_C} \cdot \frac{Q_{c,max}^2}{1 + Q_{c,max}^2} - \frac{C_{0,min} \cdot C_C}{C_{0,min} + C_C} \cdot \frac{Q_{c,min}^2}{1 + Q_{c,min}^2} \end{aligned} \tag{5}$$

$$Q_c = \omega_0 C_0 R_0 \left(1 + \frac{C_0}{C_C}\right) \tag{6}$$

4 The measurement results

The die photograph of VCO is shown in Fig. 8 (a) and the area is 900 μm × 850 μm. The power supply of test buffer enclosed by the dashed lines is 1.8 V and its linearity is high. The VCO is tested using on wafer probing and the measured current is 4.4 mA. The measured tuning curves are shown in Fig. 8 (b) and the operating frequency range is 4.6∼5.2 GHz. The unequal intervals between the tuning curves are caused by the rphpoly-rf resistors in series whose value doesn't increase linearly with the number of resistors at high frequency, so the ratio of $R_0 \sim R_3$ is not 8:4:2:1 around

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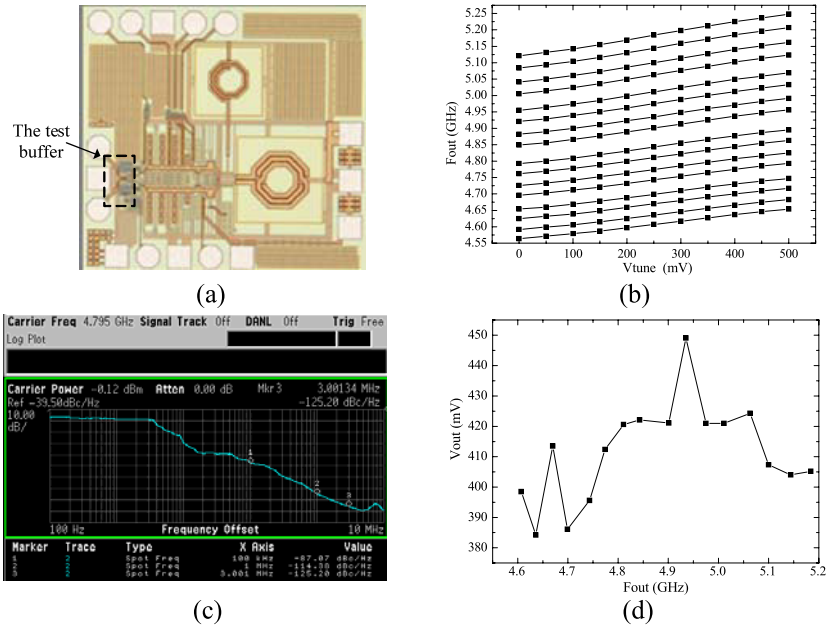

Fig. 8. (a) Chip photograph of VCO (b) Measured tuning curves of VCO (c) Measured phase noise at 4.8 GHz (d) Measured amplitude of single-ended output signal of VCO

5 GHz. The K_{VCO} is 180∼250 MHz/V from Fig. 8 (b). The measured phase noise is −114 dBc/Hz @1 MHz from carrier frequency 4.8 GHz shown in Fig. 8 (c). The measured output amplitude of single-ended signal of VCO excluding the test buffer gain is from 380 mV to 450 mV versus the oscillation frequency shown in Fig. 8 (d). The FoM of VCO is given by equation (7) [6], and the performances compared with other previous works are shown in Table I, which shows that the FoM of proposed VCO is the highest.

$$FoM = \frac{1}{L \cdot P_{\mathrm{d}}} \cdot \left(\frac{\omega_0}{\omega_{\mathrm{m}}}\right)^2 \tag{7}$$

Table I. Performances compared with other papers

Performance parameters	[1]	[2]	[3]	[4]	This paper
Process (μmCMOS)	0.09	0.25	0.35	0.18	0.18
Power supply voltage(V)	0.5	2.5	2.7	1.8	0.5
K_{VCO}(MHz/V)	220	200	100	92	220
Oscillating frequency ω_0(GHz)	2.6	5.44	4.7	5.8	4.8
Phase noise of ω_0@1MHz(dBc/Hz)	-113	-116	-110	-110	-114
Power consumption (mW)	2	6.25	10.8	8.1	2.2
Tuning range (GHz)	2.4~2.6	5.14~5.7	4.45~4.7	5.860~6.026	4.6~5.2
FoM	178.3	182.8	173.1	176.2	184.2

5 Conclusions

The proposed technique is attractive to solve the low voltage VCO coarse tuning problems. Moreover the forward-body bias voltage technique can improve the g_{m} of transistor and be used in the low voltage circuit design. The measured results verified that the proposed technique is robust and feasible for low voltage VCO.

DOI: 10.1587/elex.10.20130535
Received July 09, 2013
Accepted July 11, 2013
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Acknowledgments

This work was supported by the National High Technology Research and Development Program (No.2007AA01Z2A7) and the Special Fund of Jiangsu Province for the Transformation of Scientific and Technological Achievements (No.BA2010073).

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