ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.24, 1–6

# A new $g_m$-boosting current reuse CMOS folded cascode LNA

**Ehsan Kargaran**[1a)], **Yasser Mafinejad**[2], **Khalil Mafinezhad**[1], **and Hooman Nabovati**[1]

[1] *Department of Electrical Engineering Sadjad Institute for Higher Education, Mashhad, Iran*

[2] *School of Engineering, Deakin University, Geelong, Victoria 3216, Australia*

a) *e.kargaran725@sadjad.ac.ir*

**Abstract:** In this paper, a new gain enhancement technique which is recommended for folded cascode LNA structures at low voltage and low power applications is presented. In order to increase power gain, a new modified version of $g_m$-boosting technique is employed which increases the power gain while consuming no extra power. The new topology shares its DC current at the folded stage in order to reduce power dissipation associated with the $g_m$-boosting technique. The proposed technique reduces power dissipation almost 27%, additionally; other parameters such as power gain and noise figure have been slightly improved. In the proposed LNA, power gain and noise figure are15 dB and 3.2 dB respectively. It consumes 1.3 mW under 0.6 supply voltage.

**Keywords:** low noise amplifier (LNA), folded cascode, high gain, low power, low voltage, gm-boosting, current reuse

**Classification:** Integrated circuits

## References

[1] E. Kargaran, G. Nabovati, M. R. Baghbanmanesh, K. Mafinezhad and H. Nabovati: Proc. IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS) (2011) 1.

[2] H.-H. Hsieh and L-H. Lu: IEEE Trans. Microw. Theory Tech. **55** [7] (2007) 1445.

[3] C.-P. Chang, J.-H. Chen and Y.-H. Wang: IEEE Microw. Wireless Compon. Lett. **19** [3] (2009) 176.

[4] H.-H. Hsieh, J.-H. Wang and L.-H. Lu: IEEE Trans. Microw. Theory Tech. **56** [8] (2008) 1807.

[5] E. Kargaran, M. R. Baghbanmanesh, M. M. Ravari, A. Soltani, K. Mafinezhad and H. Nabovati: Proc. IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS) (2012) 701.

[6] B. Razavi: *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001).

[7] X. Li, S. Shekhar and D. J. Allstot: IEEE J. Solid-State Circuits **40** [12] (2005) 2609.

[8] D. Wu, R. Huang, W. Wong and Y. Wang: IEEE Microw. Wirless Compon. Lett. **17** [7] (2007) 543.



DOI: 10.1587/elex.10.20130264
Received April 12, 2013
Accepted May 08, 2013
Publicized July 18, 2013
Copyedited December 25, 2013

## 1 Introduction

The increasing demands upon portable wireless devices have motivated the development of CMOS radio frequency integrated circuits (RFIC). These devices require low power dissipation to maximize battery lifetime. Some low power applications, such as wireless medical telemetry, require the portable devices to operate at low supply voltage with a small battery or environment energy, so the power and supply voltage constriction is a crucial issue for these designs. Being the first stage of the receiver, the design of a low noise amplifier (LNA) involves a trade-off between several goals [1] including providing a stable 50 Ω input impedance, minimizing the noise figure and supplying gain that must be high enough to lower the noise contribution of the following blocks without degrading linearity. Furthermore, in portable systems, the power and supply voltage constraint makes such optimization more complicated.

The input of the LNA needs to be matched to the output of the filter following the antenna to minimize reflections between the antenna and the LNA. Source inductive degeneration has been employed widely in recent years [1, 2, 3, 4]. Although this technique is suitable for LNA input matching in a narrow frequency band, it degrades the power gain of the LNA significantly, and hence the power gain decrement should be compensated with greater DC current. Eliminating source inductor degeneration and using parasitic gate resistance for input impedance matching which results in enhancing LNA gain is reported by the author in [5]. To further enhance LNA gain, $g_m$-boosting technique is one of the most-employed methods to increase LNA gain, but it consumes extra dc power. In order to reduce power dissipation associated with the $g_m$-boosting stage, a new $g_m$-boosting topology which employs current reuse technique is proposed in this paper.

## 2 Input Impedance matching network

Source inductive degeneration (SID) is widely investigated in recent years [1, 2, 3, 4]. Using SID technique for input impedance matching leads to reducing gain of LNA. In order to increase the power gain, a new input impedance matching called Parallel Inductor (PI) is presented by the authors in detail in [5], will not be discussed here. Source inductor has been removed and parasitic gate resistance can be converted to 50 Ω by a simple LC matching circuit network. The aim of this paper is to employ gm-boosting technique with PI matching network at designing low voltage LNA to increase power gain without consuming extra power.

## 3 Proposed gm-boosting technique

### A. Conventional $g_m$-boosting technique

Although conventional NMOS cascode with gm-boosting topology which is represented in Fig. 1 (a) [6] have better performance at amplifier's gain, it is required at least $2(V_{th}+V_{od})$ supply voltage and in 0.18 um CMOS, it is almost 1.2 V and is two times bigger than our proposed supply voltage (0.6 V). This structure cannot be used for low supply voltage. Consequently, folded cascode structure has been chosen for low voltage applications. Based on the circuit topology in Fig. 1 (b), a $g_m$-boosting technique can be


DOI: 10.1587/elex.10.20130264
Received April 12, 2013
Accepted May 08, 2013
Publicized July 18, 2013
Copyedited December 25, 2013

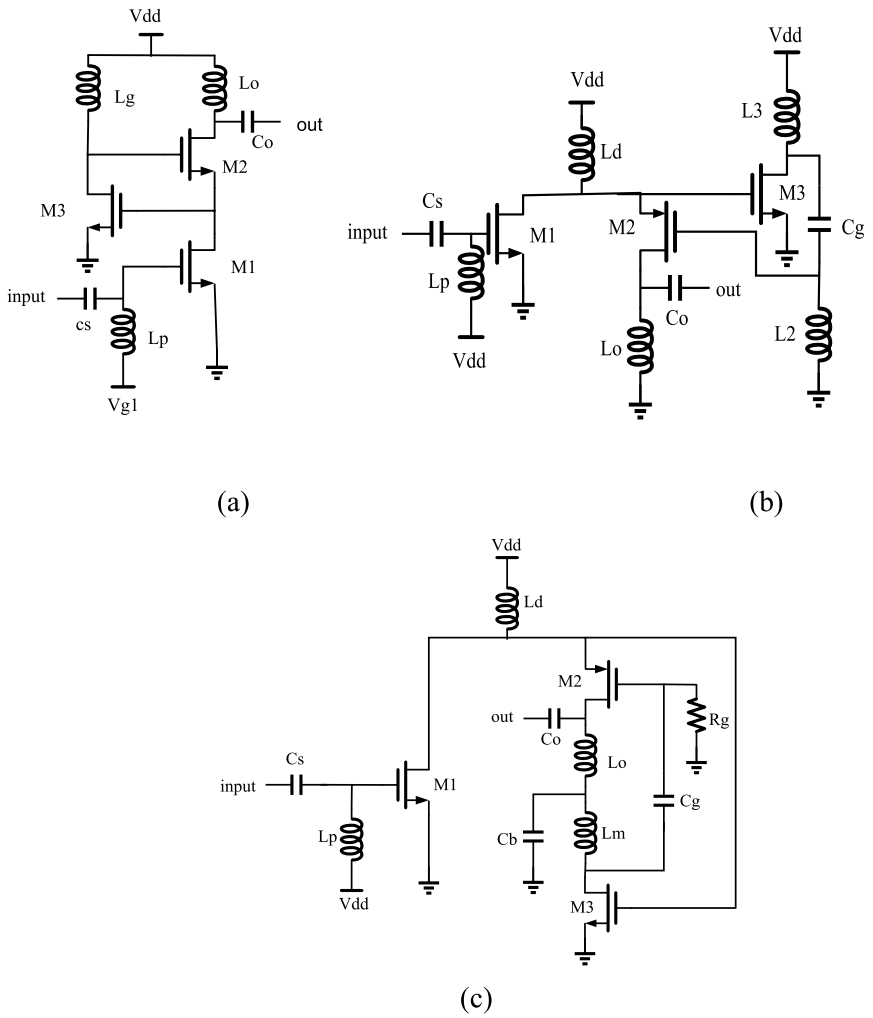



**Fig. 1.** (a) Conventional NMOS cascode with $g_m$-boosting technique, (b) folded cascode $g_m$-boosting technique with PI matching, (c) proposed $g_m$-boosting current reuse folded cascode LNA

employed in the LNA design for increasing the transconductance of the MOSFETs at low bias voltage. A conceptual illustration of the $g_m$-boosting technique is presented in [7]. Fig. 1 (b) shows the circuit schematic of the folded cascode LNA with the $g_m$-boosting technique at the common-gate stage. The signal at the drain $M_1$amplified by $M_3$ is coupled to the gate $M_2$ by common source stage ($M_3$). Thus, the gate-to-source voltage of transistor $M_2$ increases. Consequently, the transconductance is thus boosted for enhanced circuit performance. Assuming the voltage gain provided by the feedback stage $M_3$ is $-A_3$, the effective transconductance of the common-gate stage becomes $g_{m2}(1+A_3)$. For small-signal analysis purposes, the effective voltage gain is given by;

$$A_3 = -g_{m3}\left(r_{o3}||sL_3||sL_2||\frac{1}{sC_{out3}}\right) \quad (1)$$

As shown in [4], using $g_m$-boosting technique results in increasing LNA gain with the cost of consuming more power which could be a big limitation in low power budget systems. Overcoming this problem, a new $g_m$-boosting topology is presented in this paper which is based on current sharing scheme.


DOI: 10.1587/elex.10.20130264
Received April 12, 2013
Accepted May 08, 2013
Publicized July 18, 2013
Copyedited December 25, 2013

### B. Proposed $g_m$-boosting technique

The proposed $g_m$-boosting circuit takes advantage of the current-reuse technique by "stacking" the active nMOS stage which provides the inverting $g_m$-boosting gain between the source and the gate terminals of the folded CG stage on the tail of the CG stage .Thus, the new approach proposed here, is to reduce the power dissipation associated with the $g_m$-boosting, by implementing the "current-reused $g_m$-boosting", where the bias current is shared between the $g_m$-boosting (CS) stage and the folded stage (CG). An appropriate isolation circuit is designed to separate output of the CG and the CS stages at in-band AC-frequencies and for sharing the DC bias current. The isolation circuit also provides the loading at the drain terminals of the CG and the CS stages for adequate gain. In term of biasing, $|V_{gs}|$ in all transistors are $V_{dd}$ and to keep all transistors in saturation region, $|V_{ds}|$ should be higher than $|V_{gs}|-|V_{th}|$. Obviously, M1 is in saturation and the size of M2 and M3 are properly chosen to set $|V_{ds2}|=V_{ds3}=300$ mV and in all corner cases would remain in saturation region. The circuit topology of proposed $g_m$-boosting current reuse folded cascade LNA is shown in Fig. 1 (c). As can be clearly seen from the Fig. 1 (c), the signal at drain of M1 is amplified by M3 then is coupled to the gate of M2 by Cg while the connected node between $L_o$ and $L_m$ is bypassed by Cb. The circuit thus saves power through the reuse of the bias current. Consequently, the gate-to-source voltage of $M_2$ is enhanced which results in increasing transconductance of $M_2$. The key point is that $M_2$ and $M_3$ share their DC current and results in maintaining its previous power budget which is very important for low power applications.

As mentioned earlier, the effective transconductance of the common-gate stage becomes $g_{m2}(1+A_3)$ without dissipating extra power. So the effective voltage gain of $M_3$ is given by;

$$A_3 = -g_{m3}\left(r_{ds3}||sL_m||\frac{1}{sC_{out3}}\right) \tag{2}$$

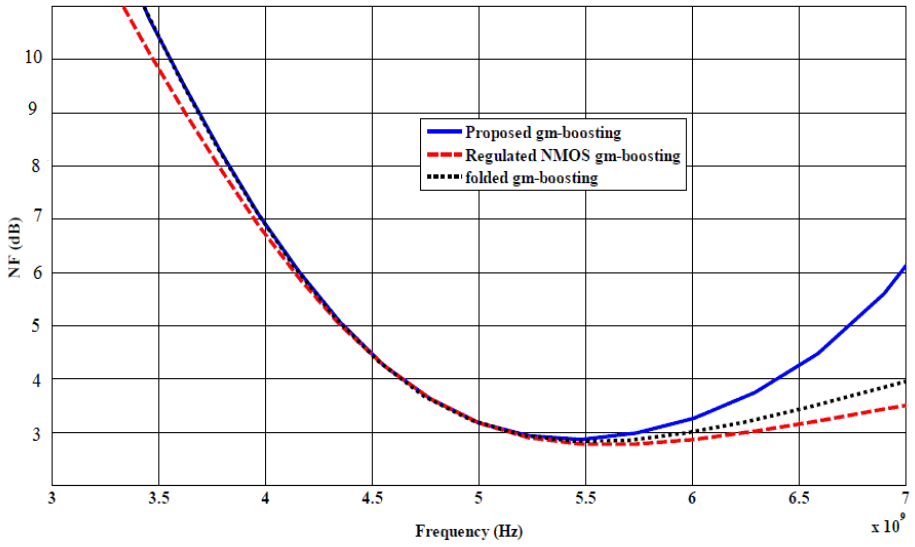
Furthermore, increasing transconductance of $M_2$, also suppresses the noise contribution of the common-gate transistor at the output port.

## 4 Simulation results

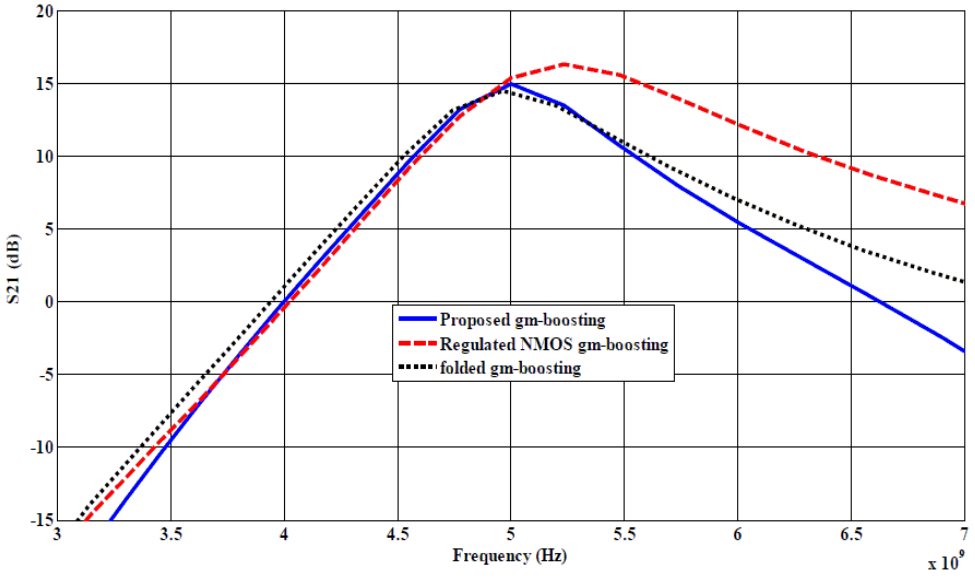
The LNAs circuits have been simulated by HSPICE RF using 0.18-$\mu$m CMOS process BSIM3 model parameters. The LNAs operate with the 0.6 V power supply. The folded cascode structures used in the design of these circuits are studied, with the width of the transistors $M_1$ and $M_2$ equal to 80 $\mu$m and 160 $\mu$m, respectively. To reduce the gate resistance, the multi-finger configuration is used to implement these devices, in which the width and length of each finger are 8 $\mu$m and 0.18 $\mu$m, respectively.

The simulated NF and $S_{21}$ performances of the LNAs are plotted in Fig. 2 (a) and Fig. 2 (b) respectively. For the folded cascode $g_m$-boosting structure shown in Fig. 1 (b), the input and output reflection coefficients are lower then −10 dB and −9.5 dB, respectively. The result shows noise performance of 3.3 dB and its power gain is 14.6 dB while the consumed power is 1.78 mW. This structure has $IIP_3$ of −15 dBm .The performance of proposed $g_m$-boosting current reuse LNA is also presented. Input and output reflection coefficients are lower then −8 dB and −12 dB, respec-


DOI: 10.1587/elex.10.20130264
Received April 12, 2013
Accepted May 08, 2013
Publicized July 18, 2013
Copyedited December 25, 2013




(a)




(b)

**Fig. 2.** (a) simulated Noise figure, (b) Simulated $S_{21}$

tively. The power gain and noise figure of the proposed LNA are 15 dB and 3.2 dB respectively. By introducing this technique, power consumption can be reduced by 27%, furthermore; power gain and noise figure have been slightly improved. The proposed LNA consumes 1.3 mW power. The IM3 of the LNA was simulated by two input tones with 10 MHz offset. The circuit shows $IIP_3$ of $-15.9$ dBm. The return loss, $S_{12}$, is less than $-25$ dB over the bandwidth.

To evaluate the performance of an ultra low voltage LNAs, different figures of merit (FOMs) are commonly used in the literature such as follow;

$$FOM = \frac{gain(abs).IIP_3(mW)}{(NF-1)(abs).power(mw)} \tag{3}$$

Table I represents the summary of the simulation results and comparison with other published papers.


DOI: 10.1587/elex.10.20130264
Received April 12, 2013
Accepted May 08, 2013
Publicized July 18, 2013
Copyedited December 25, 2013

**Table I.** comparison results with other published papers, in $F_0$=5 $GH_z$

| Ref. | **Proposed $g_m$-boosting** | Fig.1 (b) | Fig.1 (a) | [2] | [3] | [4] | [8] |
|---|---|---|---|---|---|---|---|
| Tech (μm) | **0.18** | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 | 0.13 |
| Vdd (V) | **0.6** | 0.6 | 1.2 | 0.6 | 0.6 | 0.6 | 0.4 |
| Power(mw) | **1.3** | 1.78 | 3.4 | 0.9 | 0.8 | 1.68 | 1.03 |
| NF(dB) | **3.2** | 3.3 | 3.3 | 4 | 3.7 | 3.5 | 5.3 |
| $S_{21}$(dB) | **15** | 14.6 | 16 | 9.5 | 11.2 | 14.1 | 10.3 |
| $S_{11}$(dB) | **-8** | -10 | -8 | -15 | -18 | -17 | -17.7 |
| $S_{22}$(dB) | **-12** | -9.5 | -10 | -20 | -21 | -17 | -11.4 |
| FOM | **0.067** | 0.051 | 0.051 | 0.042 | 0.043 | 0.033 | N/A |
| $IIP_3$(dBm) | **-15.9** | -15 | -13 | -16 | -17.5 | -17.1 | N/A |
| Body biasing | **Not used** | Not used | Not used | Not used | Used | Used | Used |
| S/M* | **S** | S | S | S | S | S | M |

* Simulation/Measurement results

## 5 Conclusion

In this paper, design of low voltage low power LNA for WLAN application using 0.18 $\mu$m CMOS technology is presented. $G_m$-boosting technique is one of the most favorite techniques for increasing LNA gain; however this method consumes extra power. This paper presents a new approach to enhance the transcondcutance ($g_m$-boosting) of an LNA by modifying the current-reuse technique to reduce the power dissipation by sharing the bias current between the $g_m$-boosting and the signal amplifying stages. Using this technique saves about 27% of total dissipation power while the other metrics are approximately constant. Employing folded cascode configuration, the fully integrated LNA can operate with small supply voltage of 0.6 V. The simulation results show that the proposed LNA is suitable for ultra low power and ultra low voltage applications.


DOI: 10.1587/elex.10.20130264
Received April 12, 2013
Accepted May 08, 2013
Publicized July 18, 2013
Copyedited December 25, 2013