IEICE Electronics Express, Vol.8, No.21, 1801–1807

An ultra low power and low complexity all digital PLL with a high resolution digitally controlled oscillator

Arash Abadian[1a)], **Mojtaba Lotfizad**[1], **M.B. Ghaznavi-Ghoushchi**[2], **and Nasser Erfani Majd**[1]

[1] *Tarbiat Modares University Faculty of Electrical and Computer Engineering*

[2] *School of Engineering, Shahed University*

a) *abadian@modares.ac.ir*

Abstract: In this letter, a new all digital phase locked loop (ADPLL) is proposed. The proposed ADPLL is introduced a new locking procedure with low complexity which results in an ultra low power design. The design uses only two up-down counters for finding the reference frequency. An efficient glitch removal filter and a new low power DCO are also introduced in this letter. The DCO achieves a reasonably high resolution of 1 ps. The power consumption of the proposed ADPLL at 500 MHz frequency is 820 μW. The proposed ADPLL is simulated in 180 nm CMOS with Hspice and verified by MATLAB.

Keywords: all digital phase locked-loop, digitally controlled oscillator, glitch removal, low power, low complexity

Classification: Integrated circuits

References

[1] I. Hwang, S. Lee, S. Lee, and S. Kim, "A digitally controlled phase locked loop with fast locking scheme for clock synthesis application," *ISSCC Digest of Tech. Papers*, San Francisco, USA, doi: 10.1109/ISSCC.2000.839734, pp. 168–169, Feb. 2000.

[2] J. Zhao and Y. Kim, "A Novel All-Digital Phase-Locked Loop with Ultra Fast Frequency and Phase Acquisition," *52nd IEEE Intl. Midwest Symposium on Circuits and Systems*, Cancun, Mexico, doi: 10.1109/MWSCAS.2009.236048, pp. 487–490, Aug. 2009.

[3] C. Wang, C. Huang, and S. Tseng, "A low-power ADPLL using feedback DCO quarterly disabled in time domain," *Microelectronics J.*, vol. 39, no. 5, pp. 832–840, Feb. 2008.

[4] C. C. Chung and C. Y. Lee, "An all-digital phase-locked loop for high speed clock generation," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 347–351, Feb. 2003.

[5] H. Eisenreich, C. Mayr, S. Henker, M. Wickert, and R. Schüffny, "A novel ADPLL design using successive approximation frequency control," *Microelectronics J.*, vol. 40, no. 11, pp. 1613–1622, Nov. 2009.

[6] C. Wu, W. Shen, W. Wang, and A. Wu, "A two-cycle lock-in time ADPLL design based on a frequency estimation algorithm," *IEEE Trans. Circuits and Syst. II, Exp. Briefs*, vol. 57, no. 6, pp. 430–434, June 2010.

DOI: 10.1587/elex.8.1801
Received September 12, 2011
Accepted October 05, 2011
Published November 10, 2011

[7] A. Abadian, M. Lotfizad, N. E. Majd, M. B. Ghaznavi-Ghoushchi, and H. Mirzaie, "A new low-power and low complexity all digital PLL (AD-PLL) in 180 nm and 32 nm," *ICECS 17th IEEE International Conference*, Athen, Greece, doi: 10.1109/ICECS.2010.5724514, pp. 305–310, Dec. 2010.

1 Introduction

Phase-locked loops (PLL) are extensively used in many communication and electronic systems for clocking or frequency synthesis. Cellular phones, computers, televisions are such examples. Most of the conventional PLL designs are analog based. The analog PLLs have problems such as digital switch noise coupling with power supply, substrate induced noise, sensitivity to process parameters and capacitors and resistors, which are required in the loop filter. On the opposite, All Digital Phase Locked Loop (ADPLL) is composed of all digital components so it has a high resistance to supply noise, temperature variation and process parameters [1, 2, 3].

Some conventional ADPLL designs are introduced in [3, 4, 5, 6]. In these designs generally, a complicated way such as binary searching or time to digital converter (TDC) is used for locking which results in power and area consumption that is not suitable for mobile devices.

In this letter, a new way to lock procedure is proposed. Also a new DCO is introduced and an efficient glitch removal circuit is applied in this circuit. All of the above make this design, ultra low power and low complexity.

2 Proposed ADPLL architecture

The proposed ADPLL block diagram is shown in Fig. 1a. The major blocks of the ADPLL are Phase Frequency Detector (PFD), filter, controller, Digitally Controlled Oscillator (DCO), and Frequency-Divider. The PFD detects the reference clock and the feedback clock phase difference. When feedback clock lags the reference clock, the Up signal would be high and the Down signal would be low and vice versa. When the Up signal is low, the PFD generates some positive impulses which act as glitches. These impulses consume power and disturb the ADPLL function. In this design a filter is used to remove these impulses. The filtered Up signal, Uo, is applied to an up-down counter. The up-down input of the counter is controlled by the Uo signal. The counter generates suitable codes according to the up-down input. By changing the code, the DCO generates a clock proper to the input code. The output of the DCO, Out, is applied to the divider, and the output of the divider is applied to the PFD to compare with the reference clock again. Finally the counter toggles between two codes, which one of these codes is acceptable. In this ADPLL, a circuit, which is described in the section 3, is used to select the best code. This code is the coarse code. So the ADPLL is going to the fine mode and the procedure is repeated to find the suitable fine code. It is a very low complexity way to lock.

DOI: 10.1587/elex.8.1801
Received September 12, 2011
Accepted October 05, 2011
Published November 10, 2011

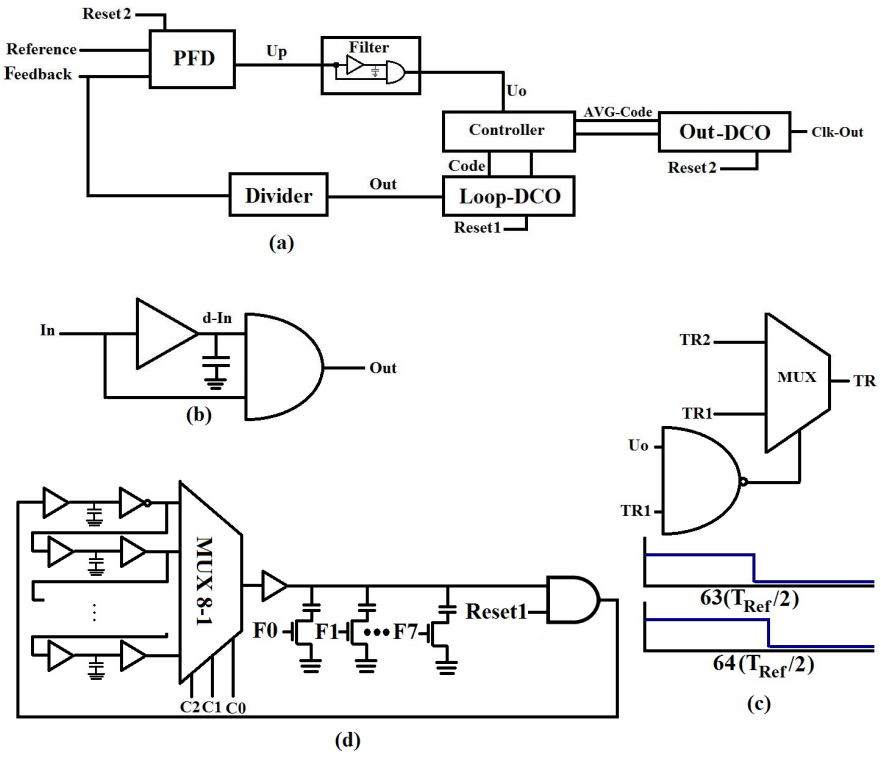

Fig. 1. a) Schematic diagram of the proposed ADPLL, b) Glitch removal filter, c) Fine counter start time circuit, d) The proposed DCO.

3 Circuit description

The PFD is a well-known circuit which is completely described in [4]. The Reset2 input of the PFD enables the ADPLL circuit. The glitch removal filter removes impulses which are produced from PFD. Low power consumption and low-complexity of this filter makes it ideal for glitch removing in this architecture. According to Fig. 1.b which shows this filter, the disturbed signal is applied to a buffer and then delayed with a capacitor, so the logical AND of the delayed signal and the original signal will eliminate the positive glitches as shown in Fig. 2.b. The capacitor value of the glitch removal filter is important to eliminate the glitches. The minimum value of this capacitor is:

$$C_f = \frac{R_1 C_1 \ln 2 + \Delta t/2}{R_2(1+\ln 2)} - C_2 \tag{1}$$

Which R_1 and C_1 are the parasitic resistor and capacitor at the input of the buffer, R_2 and C_2 are the parasitic resistor and capacitor at the output of the buffer and Δt is the maximum glitch duration. The output of the filter is applied to a ud-counter to generate the control codes for the DCO. When the Coarse control code is started to toggle, the Fine Counter should start counting. So, its starting time has to be exactly found. Since after finding the approximated frequency the Coarse code toggles between two codes, the ADPLL has to choose one of them and then start fine tuning. The Coarse Counter clock is the logical AND of the Count-Clk and the TR signal. The

DOI: 10.1587/elex.8.1801
Received September 12, 2011
Accepted October 05, 2011
Published November 10, 2011

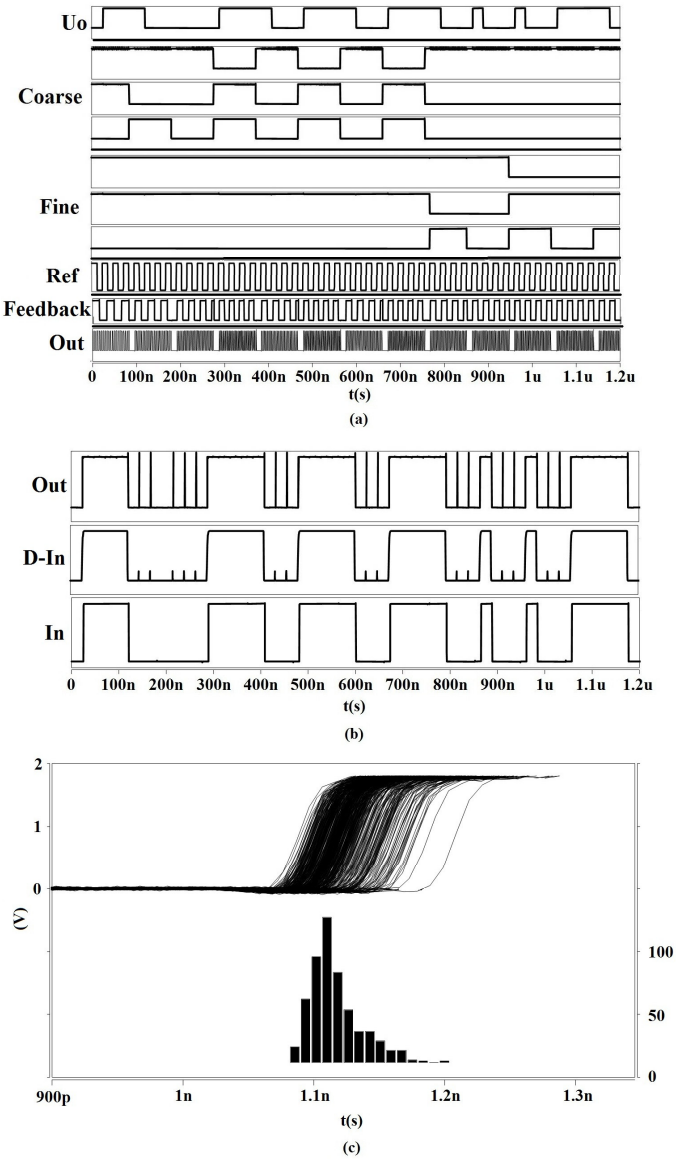

Fig. 2. a) Transient response of the proposed ADPLL, b) Glitch removal filter simulation results, c) Jitter Simulation.

Count-Clk frequency is 1/8 of the reference clock frequency. The TR is a signal which determines when the Fine Counter should start counting. To find the correct Fine Counter starting time, the TR has to be changed to zero at, $t_1 = 63 \times T_{Ref}/2$ or $t_2 = 64 \times T_{Ref}/2$-where T_{Ref} is the reference clock period-. For a proper selection between t_1 and t_2, the Uo signal is applied. If the Uo signal is low at t_1, this time is the proper time for the Fine Counter to start and if it is high at t_1, it means that the Fine Counter has to start counting at t_2. The circuit which is shown in Fig. 1.c realizes these conditions. The ultra low power DCO which is used in this circuit is shown in Fig. 1.d. The coarse code is applied to a multiplexer to select the proper delay line path, and then the fine code selects a capacitor between 8 capacitors which are in the middle of the line path. Each capacitor enables with a transistor and changes the delay time. The code which is applied to the gate

DOI: 10.1587/elex.8.1801
Received September 12, 2011
Accepted October 05, 2011
Published November 10, 2011

of these transistors is one-hot code. The Reset1 input of the DCO disables the loop-DCO quarterly. This results in lower power consumption. Also this signal, Reset1, enables the loop-DCO in the same phase with the reference clock phase. To reduce the output jitter of the circuit, the average of the Coarse and Fine codes are applied to the out-DCO. The Reset2 signal which is applied to Out-DCO and the PFD is used For Synchronization between Out-DCO and Loop-DCO and actually enables the ADPLL. To minimize the device variation between Loop-DCO and Out-DCO layout rules has to be applied precisely. For minimize the capacitor errors, dimensions have to be chosen to minimize the perimeter while keeping the area the same. To estimate the period variation according to device variation, the DCO is simulated with Monte-Carlo approach using Gaussian distribution function with 10% variation in capacitor values, W/L of the buffers, and threshold voltage, so the period variations are 5 ps, 5 ps and 70 ps, respectively. These results show the device variation can't cause a major effect on the system operation. The pk-pk jitter simulation of the DCO is 127 ps and is shown in Fig. 2.c. For jitter calculation a Gaussian random value between 1.6–2 V for supply voltage is used. The random values are not symmetric and this is the reason of larger jitter in the right part. The number of bins in jitter histogram is 500. The RMS Jitter is 21 ps. Since the supply voltage of two DCOs is equal, so the difference of the applied supply voltage of two DCOs is less than the variation which is taking into account. This DCO can achieve 1 ps resolution. The Coarse tuning part of the DCO is based on delay cells and the fine tuning part of the design is based on changing the capacitors. So we can achieve higher resolution in comparison with other delay cell based DCOs. The delay cell based DCOs, have resolution problem so they are designed with multi-stage fine tuning part. With using gated capacitors, this circuit does not suffer from resolution problems. Power consumption of this DCO is 320 μW in 500 MHz frequency. In this structure of the DCO for increasing the frequency, the delay line path has to be reduced, so the power consumption of the DCO is not increased properly with the frequency increasing.

4 Simulation and performance comparison

The proposed ultra low power and low complexity ADPLL is evaluated in TSMC 180 nm and 1.8 V power supply and the golden model of the design is verified by MATLAB. The power consumption of the proposed ADPLL at 500 MHz frequency is 820 μW. The frequency range of the ADPLL is 200 MHz to 780 MHz. Fig. 2.a shows the proposed ADPLL transient response where the reference clock frequency is 41.67 MHz and the division ratio is 8. So the DCO output, Out, frequency is 333 MHz. As seen in Fig. 2.a, the reference clock and the feedback are being matched. Table I summarizes the comparison of the proposed ADPLL with several prior works. By way of comparison, the power consumption, and the power delay product of our design are the best of all listed designs. However the proposed design values are simulated

DOI: 10.1587/elex.8.1801
Received September 12, 2011
Accepted October 05, 2011
Published November 10, 2011

and the other designs are measured, but these results are reasonable according to the design. Of course according to the applied technology we can achieve even better results in smaller technologies.

As it can be seen from Table I, the power consumed by this structure is significantly lower than that by other designs. This significantly lower power consuming is due to the low complexity of the design. In [3] a binary frequency searching method is used to lock. To realize this method, a finite state machine (FSM) is used. The DCO which is used in this design has a very low bandwidth. The work cited in [4] is an earlier ADPLL design. This design is also used the binary frequency searching. This is a highly power consuming design due to the technology, power supply and its design. In [5] also the binary frequency searching is applied. In [6] a TDC is used to lock. This design introduced a new time-domain frequency estimation algorithm and it results in fast lock mechanism but it is much more complicated than the proposed design. So its power consumption is rather high and it is not suitable for mobile devices which are so important nowadays. In [7] which is the previous version of this design, the applied DCO is very power consuming and the frequency range of the DCO is very lower than this proposed deign. As it can be seen all of the attributes of this design is better than the previous version.

Our design has proposed a new way to lock and it is done only with a counter. In comparison with other designs it consumes the lowest power. This is due to the DCO design and low complexity. The functionality of the design is first verified with MATLAB. In the second stage the detailed circuit-level design and simulation is performed. Our simulations confirm that the design is capable of operation in multi-supply voltage level too. This boosts the application of the design for power-efficient multi-VDD designs. The FFT analysis is also verifying the spectrum impurity of the DCO output signal frequency.

Table I. Specification comparison of the proposed ADPLL.

	Proposed	[3]	[6]	[8]	[4]	[5]
Technology(μm)	0.18	0.18	0.18	0.18	0.35	0.13
Power consumption	820μW @500 MHz	1.53mW @133 MHz	14.5mW @446 MHz	2.5mW @403 MHz	100mW @500 MHz	7.4mW @500 MHz
PDP(ns.mW)	1.64	11.48	32.5	6.2	200	14.8
Max. freq. (MHz)	780	158	446	590	510	800
Min. freq. (MHz)	200	70	28	340	45	84
Supply voltage(V)	1.8	1.8	1.8	1.8	3.3	1.5
Output Jitter (ps)	127	162	70	155	70	870
Evaluation Method	Simulated	Measured	Measured	Simulated	Measured	Measured

5 Conclusion

A simple yet efficient ADPLL structure for ultra low power applications is proposed in this letter. Glitches in ADPLL PFD section are power consuming and may alter the reliability of the design. We used an efficient glitch

DOI: 10.1587/elex.8.1801
Received September 12, 2011
Accepted October 05, 2011
Published November 10, 2011

removal filter after PFD circuit which removes glitches with negligible power consumption which is more efficient than a common digital filter and it is easy to design. The proposed design has lower complexity than the other designs in the literature and the circuit level simulation with Hspice at 180 n CMOS with 1.8 V power supply, is also verified against golden model in MATLAB. The frequency range and the DCO resolution and the PDP of the proposed ADPLL circuit bear comparison to the other ADPLLs. Although in comparison with the TDC based designs, this ADPLL needs more cycles to lock, but since in this design the procedure frequency is more than TDC based designs -due to lower division ratio- the lock time is approximately equal to that of these designs.

DOI: 10.1587/elex.8.1801
Received September 12, 2011
Accepted October 05, 2011
Published November 10, 2011