

On the design of low power 1-bit full adder cell

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Abstract: A 1-bit full adder cell based on majority function is designed and simulated. In this design the time consuming XOR gates are eliminated. Low-power consumption is targeted in implementation of our design. The circuit being studied is optimized for energy efficiency at 0.18- μ m CMOS process technology. The new circuit has been compared to the previous work based on power consumption, speed and power delay product (PDP). HSPICE and Cadence simulations show that the proposed adder can work more reliably at different range of supply voltage. The proposed design has the best PDP in comparison with the others.

Keywords: full adder, majority function, low power, VLSI circuit, performance analysis, static CMOS inverter, MOSCAP

Classification: Integrated circuits

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1 Introduction

The addition of two binary numbers is fundamental in various circuits especially circuits used for performing arithmetic operations like multiplication and division, compressors, comparators and parity checkers. There is no ideal adder cell that can be used by all types of applications. Therefore, many different circuits for binary addition have been proposed over the last decades [1, 2, 3, 4], covering a wide range of performance characteristics to satisfy the constraints enforced by different applications.

Design of digital integrated circuits for many applications relies on three major criteria: Low power consumption, small chip area, and high speed. Demand and popularity of portable electronics is driving the designers to strive for smaller silicon area, higher speeds, longer battery life and more reliability [5]. Power is one of the premium resources a designer tries to save when designing a system. The battery technology doesn’t advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems. The goal to extend the battery life span of portable electronics is to reduce the energy consumed per arithmetic operation.

Enhancing the performance of the adder units can significantly improve the system performance. Therefore careful design and analysis is required for these units to obtain optimum performance.

Lowering the supply voltage and reducing the number of transistors of 1-bit adder design is a proper method for lower power consumption. Using lower number of transistors to implement a logic function is beneficial in reducing the device and interconnect parasitic and reducing the chip area, resulting in lower time delay and potentially lower power consumption. However, many low-number-transistor adders do not operate correctly at low supply voltage in 0.18 μm and subsequent CMOS technologies due to V_t loss problem. The goal of this work is to design the low-number-of-transistors full adder that works successfully at ultra low supply voltage, avoids any degradation on the output voltage, has less delay in critical path, and is noise immune even at low supply voltage.

The rest of this paper is organized as follows: in Section II we present and analyze the proposed 1-bit full-adder cell. Simulation setup and results are described in Section III. Finally, Section IV concludes the paper.

2 The proposed adder cell

The full-adder cell in Fig. 1 (a) [1] (Majority Based Design full adder) is based on low power design of majority not function with classical CMOS inverter and capacitors. It has low transistor count results in switch capacitance reduction and the capability of working at ultra low supply voltage. Operating properly at this range of supply voltage without V_t loss problem, having two transistors from V_{dd} to the ground and taking advantage from using four robust CMOS inverters make it a good choice for implementing low power design.

The main drawback of that design is the high short circuit current. This method suffers from an excessive power dissipation caused by the short circuit current in a steady state and also during transient from high to low and vice versa when both transistors are on. The total power dissipated in a generic digital CMOS gate is given by Eq. (1).

$$P_{total} = P_{dynamic} + P_{short-circuit} + P_{static}$$

$$= V_{dd} \cdot F_{clk} \cdot \sum_i V_{i\ swing} \cdot C_{i\ load} \cdot \alpha_i + V_{dd} \cdot \sum_i I_{sc} + V_{dd} \cdot I_l \quad (1)$$

Where F_{clk} denotes the system clock frequency, $V_{i\ swing}$ is the voltage swing at node i (ideally equal to V_{DD}), $C_{i\ load}$ is the load capacitance at node i , α_i is the activity factor at node i , and I_{sc} and I_l are the short circuit and leakage currents, respectively.

Switching power is power consumed in charging and discharging of the circuit node capacitances during transistor switching, short circuit power dissipation occurs because of the short circuit current flowing from power supply to ground during transistor switching and static power is due to leakage and static currents flowing while the circuit is in the stable state. The first two are referred to as dynamic power which constitutes the majority of the power dissipated CMOS VLSI circuits. The third component is negligible if the circuit is designed well [6].

The input voltage of CMOS inverter gate that generates \overline{Cout} in Fig. 1 (a) adder is 0, $1/3 V_{DD}$, $2/3 V_{DD}$ or V_{DD} when 0,1,2 or 3 of inputs are high. Working in high gain part of a CMOS conventional inverter VTC results in both N-MOS and P-MOS transistors being on at the same time which caused to have direct path from V_{DD} to the ground.

In order to eliminate the direct path short circuit current of that design a condition is elected to ban these two transistors being on at the same time. Eq. (2) [7] shows any transition from 0 to V_{dd} or vice versa caused transistors being on and off in a sequential manner without any overlapping.

$$V_{dd} \leq V_{tn} + |V_{tp}| \quad (2)$$

For reducing this short circuit current results in lowering the total power dissipation of that design at $V_{dd} > 1\text{ V}$ the threshold voltage of transistors have to be modified and high- V_t transistors [1, 8] must be used which, is not an easy task.

To solve these problems and achieve a better design than [1], four inverter gates could be substituted by the new style that illustrated in Fig. 1 (b). As we can see with this new structure two cross coupled PMOS eliminate the short circuit current. But as it is clear this circuit does not operate correctly in all zeros input and also in one input being in logic ‘1’. In order to solve this problem, as shown in Fig. 1 (c) two pull-down PMOS transistors are added to the design. By employing this technique a pseudo-DCVSL (Differential Cascade Voltage Switch Logic) structure is designed which has the advantages of real DCVSL circuit. In Fig. 1 (c) to generate Carry when all the inputs or two out of the three inputs being high the pull-down NMOS transistor (N1) turns on and the \overline{Cout} node becomes low. Then the pull-up PMOS transistor (P2) turns on and starts charging $Cout$ to V_{DD} . In addition when all the inputs or two out of the three inputs being low, turning on P3 causes $Cout$ to be pulled down and \overline{Cout} starts to charge up through P1. Eventually, turning on N2 enables $Cout$ to discharge all the way to GND. SUM is also generated with the same way.

It is obvious that with this new design the short circuit current is completely eliminated and there is no necessity to work in Eq. (2) situation. The new design is robust against supply voltage variation without any modifica-

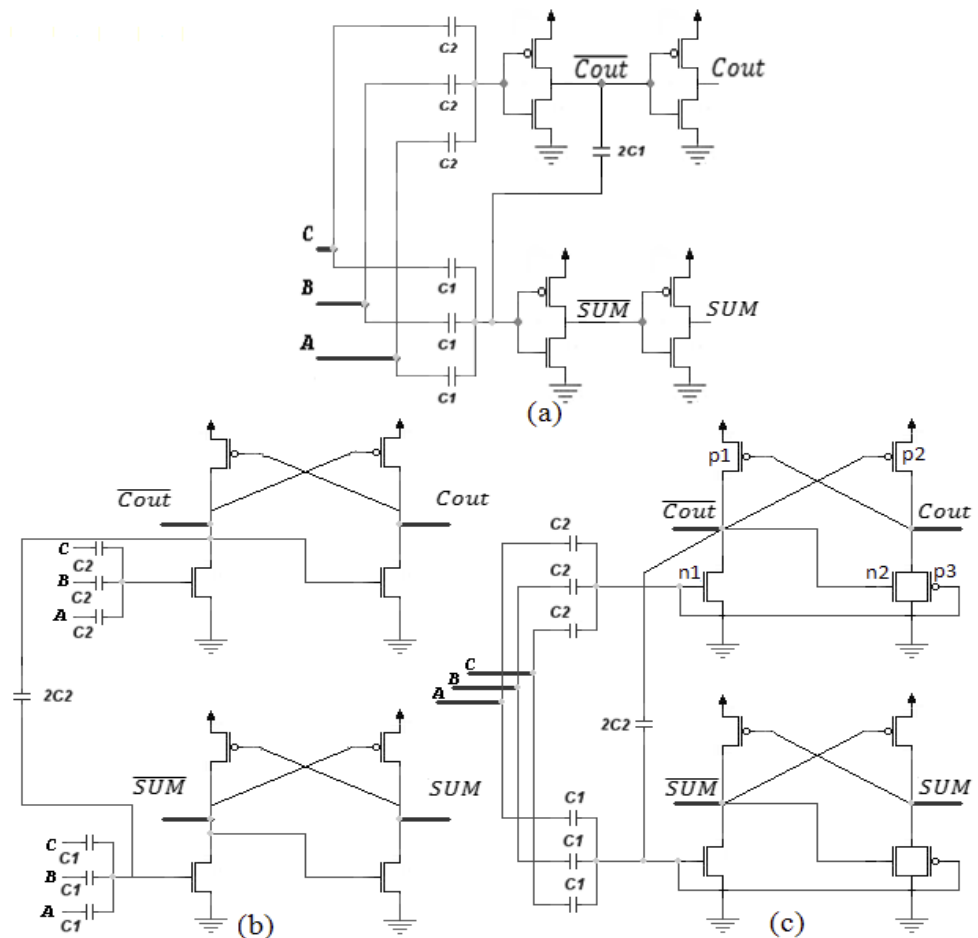


Fig. 1. (a) Majority Based Design (MBD) adder [1].
(b) Full adder cell. (c) Proposed full adder cell.

tion in transistor's threshold voltage at high supply voltage. The circuit also is a ratio less one moreover, the energy consumed per switching activity is better. It benefits from good drivability so it can be cascaded easily whereas the performance of the previous majority function based adder in Fig. 1 (a) degrade when it is cascaded. This new design also generates *Sum* and *Cout* plus invert of them which is so use full in practical environment [6].

3 Simulation

The standards of today's technology require three main parameters to measure performance: Power, Delay, and Size. The power delay product (PDP) is also a quantitative measure of the efficiency and a compromise between power dissipation and speed. So, exhaustive simulations using HSPICE and Cadence have been performed on the Complementary CMOS (C-CMOS) full adder cell [2, 9], Majority Based Design (MBD) full adder of Fig. 1 (a) and the new proposed circuit under different supply voltages (0.4 V, 0.6 V, 0.8 V, 1 V, 1.2 V and 1.4 V) at 100 MHz frequency. The technology being used is 0.18- μm CMOS technology. The threshold voltages of the PMOS and NMOS transistors are around 0.46 and 0.48 V, respectively. Majority Based Design (MBD) adder uses High- V_t transistors. Fig. 2 shows the simulation test-bench. It has been made of three cascaded adder cells. This structure simulates the circuits like regular multipliers and binary adders that use full adder cells as the building block. The inputs are fed from the buffers (two cascaded inverters) to give more realistic input signals and the outputs are loaded with buffers to give proper loading condition. The average power consumption value is measured for the three cascaded adder cells while the delay is measured from the moment the inputs are applied to the second cell, until the *Sum* and *Cout* signals of the second cell is produced. All the 64 possible transitions of input patterns are applied to the test-bench for measuring the average power consumption and worst-case delay. The delay is calculated from 50% of voltage level of input to 50% of voltage level of resulting output for both rise and fall output transitions. For the calculation of the power-delay product, worst-case delay is chosen to be the larger delay amongst the two outputs. By optimizing the transistor sizes of full adders considered, it is possible to reduce the delay of adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum PDP. The Majority Based Design (MBD) full adder of Fig. 1 (a) has already been compared with some conventional adder cell in [1]. Table I shows that the power consumption of the presented full adder increases slower, with the

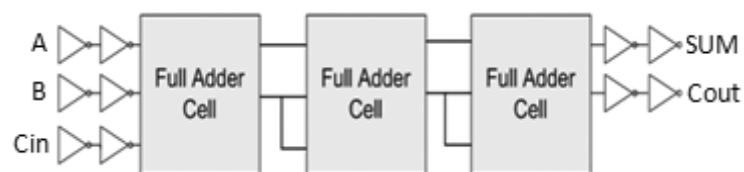


Fig. 2. Simulation test Setup.

supply voltage than the previous work without tuning V_{th} . C-CMOS adder cell fails to function at 0.4 V. The lowest voltage it can operate is 0.6 V which have the worst PDP. This new circuit performs with almost 8%, 22% and 31% improvement in power consumption over the MBD full adder at 0.4 V, 0.6 V and 1 V respectively. Also the proposed design has the best PDP in comparison with the others.

To design the proposed circuit layout [9], various techniques for constructing capacitors have been investigated. This proposed circuit's capacitors have been implemented using the MOS capacitors (MOSCAP) available in the 0.18 μm CMOS process technology [1, 10]. Fig. 3 exhibits the compact layout of the presented adder cell.

Table I. Simulation results.

$V_{DD}(\text{V})$	0.4	0.6	0.8	1	1.2	1.4
Power(μW)						
C-CMOS	-	1.274	1.366	3.109	4.698	6.71
MBD	0.402	0.62	0.937	2.076	3.019	4.601
Proposed	0.368	0.483	0.845	1.44	2.736	3.825
Delay(nS)						
C-CMOS	-	4.917	1.66	0.927	0.643	0.462
MBD	1.868	1.354	0.907	0.649	0.491	0.389
Proposed	1.755	1.36	0.771	0.602	0.47	0.402
PDP (fJ)						
C-CMOS	-	6.264	1.918	2.882	3.021	3.1
MBD	0.751	0.839	0.85	1.347	1.482	1.79
Proposed	0.646	0.657	0.651	0.867	1.286	1.538

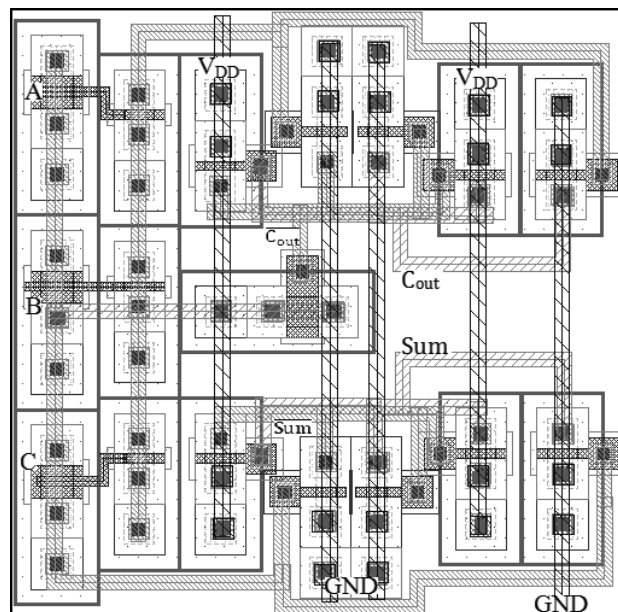


Fig. 3. Compact layout of the proposed full adder.

4 Conclusion

An area efficient and ultra low power 1-bit adder cell, using the low-number-of-transistors was described, designed and simulated. It works based on majority function and MOS capacitors. Lowering transistor counts without using pass transistor logic make this design suitable to operate at low supply voltage. In addition, some techniques to eliminate the direct path power consumption cause this new adder benefits from the lower power dissipation and a better PDP than previous similar designs without any transistor threshold voltage modification. The circuit has high driving capability so it can be cascaded easily in large tree structured arithmetic circuits.