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A 5.4 mW concurrent low noise CMOS LNA for L1/L5 GPS application

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Abstract: In this paper, a concurrent CMOS LNA for GPS application is presented, which supports L1 and L5 only modes as well as L1 and L5 simultaneous mode. To achieve concurrent operation, new cascode configuration employing a single common-source input stage and two common-gate output stages is proposed. And the band-pass matching technique using two capacitor banks is applied to achieve gain and output return loss tunability. It is implemented using 0.13 μm CMOS technology. The LNA achieved low noise figures of 1.68 and 1.67 dB with high gains of 15.7 dB and 16.7 dB at L1 and L5 band, respectively and showed more than 10 dB input and output return losses. The LNA chip consumes low current of 4.5 mA from 1.2 V supply.

Keywords: cascode, concurrent, CMOS, GPS, low noise amplifier (LNA), RF

Classification: Integrated circuits

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1 Introduction

After being equipped in a personal navigation system or mobile devices such as handheld phone, PDA and notebook, the Global Navigation Satellite System (GNSS) has been gaining more popularity. Until now, the global positioning system (GPS) using the frequency of 1,575.42 MHz (L1 band) is commercially available, however, sooner or later another frequency band of 1,176.45 MHz (L5 band) is going to start its service for civilian purpose, which will provide more accurate position information to users when used with L1 band information. Thus it is required to have a system that can support the simultaneous operation of L1 and L5 band.

Conventionally, two single band LNAs in parallel are employed for multi-band or concurrent architectures, however, which result in high implementation cost as well as occupies large system area. Therefore, it is desirable to make compact concurrent RF frontend receiver system. Among them multiband antenna and concurrent LNA are key components to achieve simultaneous operation of L1 and L5 band. Although much work has been done for the multi-band antenna, the multi-band concurrent LNA for GNSS system still remains a challenge [1].

The dual band LNA with a single input and a single output introduced in [2] can be used for the simultaneous operation at two different bands. However, the single output configuration is not preferable for concurrent operation because it lays high linearity burden on the mixer and the broadband output matching circuitry makes it difficult to achieve high gain over wide-band operating frequency range, as a result, increasing the noise figure. Thus, single input and dual output structure are adequate for these applications.

In this paper, a new concurrent LNA configuration with low power of 5.4 mW and low noise figure of less than 1.7 dB is presented, which can cover L1 and L5 band simultaneously. This new concurrent LNA provides very wide input matching flexibility and high gain at both frequency bands, while maintaining low noise figure.

2 L1/L5 Band Low Noise Amplifier

Fig. 1 (a) shows a simplified schematic circuit of the proposed concurrent L1/L5 band LNA. The LNA has been implemented using 0.13 μm RF CMOS

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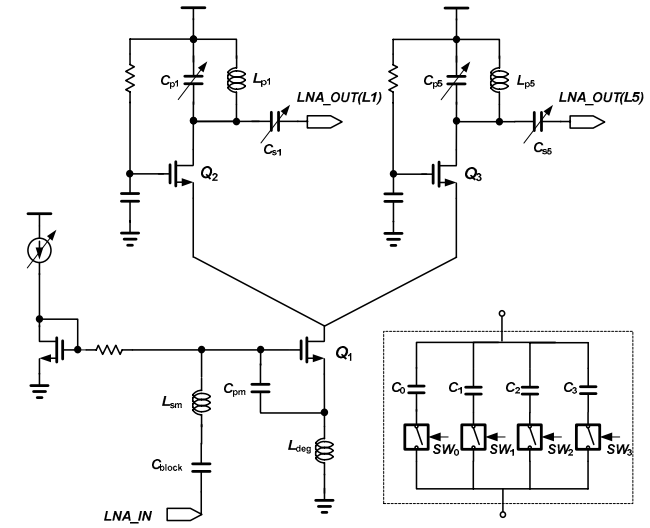
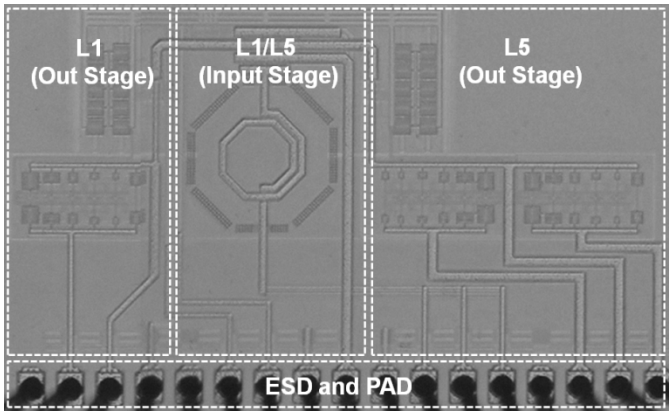


(a)



(b)

Fig. 1. (a) Schematic of the proposed concurrent LNA (b) The fabricated chip photograph (chip size = 820 μm $\times$ 1400 μm).

technology with 6-metal and 1-poly. Fig. 1 (b) shows the photograph of the fabricated LNA, where all pins are the electro-static discharge (ESD) protected.

2.1 Noise matching

Since the LNA comes ahead of any other active components in RF frontend, the noise figure (NF) of LNA is critical on the overall sensitivity of the system. So, it has to be suppressed as low as possible. To minimize the NF, simultaneous noise and input matching technique (SNIM) is used [3]. The series feedback with inductor degeneration, L_{deg} that consists of a spiral inductor on chip and external bondwire inductor is designed to move the input impedance, which is expressed in Eq. (1), to optimum noise impedance, Z_{opt} to achieve minimum noise figure, F_{min}. And also Z_{in} has to be matched to 50 ohm to lower input reflection.

$$Z_{in} = sL_{sm} + \frac{1}{s(C_{gs} + C_{pm})} + \frac{g_m L_{sm}}{C_{gs} + C_{pm}}. \quad (1)$$

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where g_m and C_{gs} is the transconductance and the gate source capacitance of Q_1, L_{sm} and C_{pm} are matching components. Satisfying SNIM conditions at both L1 and L5 band frequencies is difficult without complex matching network, so there need some compromise over optimum noise impedances of L1 and L5 band, while somewhat sacrificing NF.

2.2 Concurrent configuration

The LNA exploits commonly used cascode configuration, which is preferred for LNA architecture because it can give high impedance isolation between the input of common source stage and the output of common gate stage. To accommodate concurrent operation, two common gate output stages are employed. Each stage takes charges of L1 band and L5 band, respectively. Since the common gate output stages share the drain current of Q_1, each path gain will be lower than that of single common gate LNA, but by increasing transconductance, g_m of Q_1, adequate gain can be secured. And since the noise figure is mainly determined by common source transistor, the noise figure is not deteriorated compared to the conventional single band cascode LNA.

The output impedances at drains can be simplified by r_{out} and parallel parasitic capacitance, C_p. To match the output impedance to 50 ohm, the choke inductor and two capacitor banks have been used. The output impedance can be written in

$$Z_{out} = \left\{ r_{out} // \frac{1}{j\omega C_d} \right\} // \left\{ j\omega L_c // \left(\frac{1}{j\omega C_p} \right) \right\} + \left(\frac{1}{j\omega C_s} \right) \tag{2}$$

The parallel capacitor moves the impedance counter-clockwise direction in the admittance circle of smith chart and the series one rotates impedance in clockwise direction, to finally position it to 50 ohm. Even when the value of r_{out} and C_d change on PVT variation, the drain impedance can be easily matched by changing the parallel and series capacitances.

3 Experiment results

The tested chip is packaged in 48 pin MLF and glued on a FR4 PCB board with some discrete matching and bias components. The input impedance is optimized to compromise the noise figures in L1 and L5 band simultaneously. The loss of RF input path in PCB is about 0.35 dB and is compensated in measurement data.

Fig. 2 (a) shows the measured noise figures, gains (S_{21}), input and output return losses (S_{11}, S_{22}) for L1 and L5 band, respectively. The gains can be configured to have maximum value at each operating frequency by controlling the code of output capacitor banks. The results show the optimum gains of more than 15.7 dB and 16.7 dB gains of L1 and L5 band, respectively. And the minimum output return-losses less than 15 dB have been acquired near the frequency S_{11} results show broad matching characteristics with less than 10 dB at each band. The NF at L1 frequency of 1,575.42 MHz is about 1.68 dB and that of L5 frequency of 1,176.45 MHz is 1.67 dB. These

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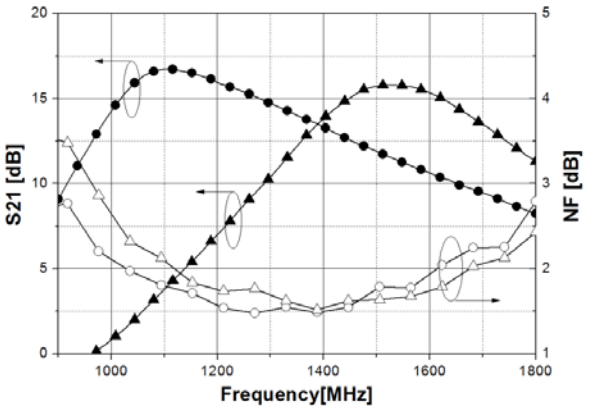
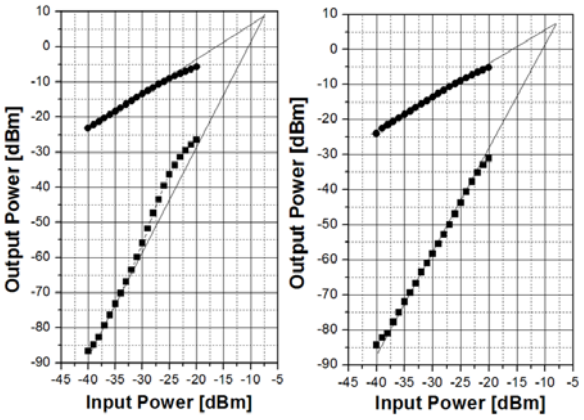


(a)



(b)

Fig. 2. (a) Measured noise figures at L1 (-▲-) and L5 (-●-) bands and insertion gain at L1 (-△-) and L5 (-○-) bands. (b) Measured fundamental output power (-●-) and 3rd order intermodulation power (-■-) versus input power at L1 and L5 band frequencies.

NF characteristics of proposed concurrent LNA are comparable or lower than that of recently published single band LNA [4, 5, 6, 7]. when only at a single frequency, the input impedances of the LNA is optimized for low NF, then the NFs are reduced to 1.4 and 1.17 dB, respectively, more than 0.3 dB compared to those of simultaneous SNIM matched results. Fig. 2 (b) show the measurement results of fundamental and intermodulation output powers versus input power at each band. The 3rd order input intercept points (IIP3) can be inferred by extrapolating measurement data. The values of IIP3s are estimated about −7.5 and −8 dBm for L1 and L5 band respectively. The implemented LNA chip consumes low current of 4.5 mA from 1.2 V supply voltage, while maintaining low noise figure in both band. The Table I. summaries the measurement results and compares recently published LNA performances.

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Table I. Comparison of the published LNA Performances.

	This work	[4][a]	[5][a]	[6]	[7]	Unit
Current	4.5	4	4.2[a]	5	6	[mA]
Supply	1.2	1.8	1.6~1.8	2.8	1.5	[V]
Gain	15.7 / 16.7		34[a]	26	20	[dB]
NF	1.68 / 1.67	5[a]	3.6[a]	3.6	0.8	[dB]
Band	L1 / L5	L1	L1	L1	L5	
Process	0.13	0.18	0.18	0.35	0.25	[μm]

[a]LNA + Mixer

4 Conclusion

A fully integrated concurrent CMOS LNA is presented. The LNA support L1 and L5 only modes as well as L1 and L5 simultaneous mode, which is implemented using 0.13 μm CMOS technology. The LNA is successfully realized employing a proposed cascode configuration with a single common-source input stage and two common-gate output stages. The LNA shows low noise figures of 1.68 and 1.67 dB for L1 and L5 band and also achieves high gain and very low output return loss The LNA chip consumes low current consumption of 4.5 mA from 1.2 V supply voltage.

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